
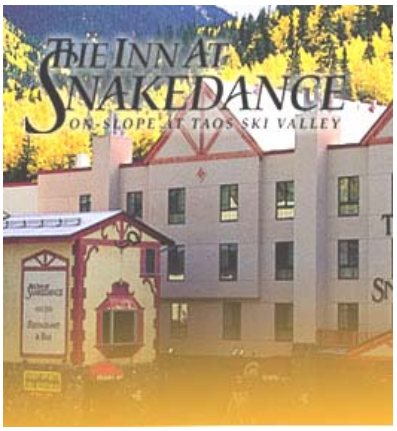



***September 11-13, 2003***

***Taos Ski Valley, New Mexico***

Click here for access to workshop presentations.

***Thursday, September 11***

6:30 – 9:00 PM Reception

***Friday, September 12***

7:30 – 8:30 Breakfast

Impact of EDA on Design/Manufacturing Cost (Organizer: Leon Stok)

**(Session Abstracts Listed on Page 3)**

8:30 – 8:35 *Session Introduction,* **Leon Stok, IBM**

8:35 – 9:20 *Design Cost Trends and their Impact on ROI*
**Juan-Antonio Carballo**, IBM

9:20 – 10:00 *Cost and CAD, changing the Design Portfolio*
**Leon Stok**, IBM

10:00 – 10:30 Break

10:30 – 11:15 *Realities of Design for Manufacturability*
**Riko Radojcic,** PDF Solutions

11:15 – 12:00 *Adding to Your Bottom Line: A New Crop of EDA Tools*
**Eric Nequist,** Cadence Design Systems

12:00 – 1:30 PM Lunch

Programming Paradigms for Reconfigurable Architectures
(Organizer: Patrick Schaumont)

1:30 – 3:00 *Panel Remarks and Discussion*
**Daryl RuDusky**, Celoxica
**Beatrice Fu,** Tensilica
**Andre' DeHon**, Caltech

3:00 – 3:30 Break

3:30 – 6:30 Open discussions and enjoy the area

6:30 – 7:30 Wine and beer social hour

7:30 – 8:30 Dinner

8:30 – 9:30 Very Big Semi, Inc. - A CAD Assessment Report, Sept. 2008
**Steve Schulz**, Si2

### *Saturday, September 13*

7:30-8:30 Breakfast

Analog/Mixed Signal Design Methods (Organizer: Martin Vlach)

8:30 – 9:15 *HDL Based Simulation for AMS*
**Ernst Christen**, Synopsys

9:15 – 10:00 *AMS Modeling*
**David Smith**, Synopsys

10:00 – 10:30 Break

10:30 – 11:15 *Top Down AMS Design Methods*
**Jim Holmes**, Texas Instruments

11:15 – 12:00 *AMS Low Power Microcontrollers*
**Richard Brown**, University of Michigan

12:00-1 PM Lunch

1:00 – 2:00 CANDE Business Meeting

## Session Abstracts:

**Design Cost Trends and their Impact on ROI  Juan-Antonio Carballo, IBM**
Design cost trends in the electronic industry, an increasingly price-sensitive one, don't leave room for inefficiencies. Long-term growth in unit infrastructure costs and labor costs is persistent, with labor expected to stay dominant. Design complexity growth is exponential and software is an increasing portion. Past productivity leaps resulted in over 32% average annual growth, which has hardly kept total design costs under control. Practically any SoC design today requires a design investment in the 10-50-million-dollar range, entered as a fixed cost. Keeping these costs from exploding until 2010 will require at least 2 or three major EDA leaps, especially in software design and design reuse. But while costs matter on their own, their overall impact on return-on-investment (ROI) of an electronic product is the bottom line. Together with cost, revenue, time, and risk are the critical factors affecting ROI. We discuss these ROI related trends for design, and conclude that productivity growth is more than a cost reduction lever -- it is a critical enabler for a positive ROI. We discuss data from a case study in reuse, where we show how investment in design reuse technology results in cost reductions and double-digit ROI improvements. We conclude that (a) substantial growth in reuse granularity and software productivity will be needed in this decade to maintain acceptable return for the industry, and (b) ROI analysis can reveal the true value of key productivity leaps and thus may become a critical tool for justification and evaluation of EDA innovation.

**Cost and CAD: changing the Design Portfolio,  Leon Stok, IBM**
Much discussion has recently been focused on mask costs, even leading to predictions like the death of ASICs. (Will this be a CANDE prediction this year?) However, besides mask costs other manufacturing costs (such as chip, pacakge and test) and design costs (such as designers and design tools)  need to be carefully studied to understand the cost impact and predict changes in the design style landscape. New silicon implementation platforms like various forms of structured ASICs and VPGAs are being proposed to mitigate a portion of the design and/or manufacturing cost at the expense of silicon efficienct in terms of area, power and/or performance.  We will look at these cost factors and describe a framework to compare some of these silicon implementation platforms.

**Realities of Design for Manufacturability, Riko Radojcic,  PDF Solutions**
The bottom line of any semiconductor enterprise is, among other factors, a function of product yield. Simple analyses shows that the product yield is, ultimately, controlled by the design as much as by the manufacturing process. Since the industry experienced surprisingly low yields at 130 nm node, and below, DFM has become an especially ‘hot’ topic. However, the reality is that DFM in nanometer era means a lot more that what it used to be: DRC clean design + high test fault coverage = DFM.  Optical, material, and control factors, associated with the manufacturing processes, have all been pushed to the limit, such that the process ‘window’ is tight, and requires intelligent, process-specific, fine-tuning of various design features. At the same time, the reality is that the DFM considerations must not add to the design cost or schedule, must not be a manual post-process, and must not require a high degree of familiarity with the manufacturing process.  A DFM-for-Design solution must be baked into a design flow and will require modifications in the EDA tools, in the IP, and in design methodologies, but must be based on thorough manufacturing process characterization and modeling.

**Adding to Your Bottom Line: A New Crop of EDA Tools, Eric Nequist, Cadence Design Systems**
Speed, area, and productivity have been used to benchmark EDA tools since the beginning of time. To use a tool simply because it is “5 times faster” does not account for the true cost and impact of the tool. This is becoming readily apparent as designs move to 90nm and 65nm where the classic benchmarks give way to concerns of manufacturability and yield. Closure and performance will be “givens” in tomorrow’s tools. New tools must create designs with the ability to constrain and analyze manufacturability, yield and reliability parameters. By designing for manufacturability and manufacturing with design intent, the resulting yield gains will directly affect the bottom-line. The true impact of these new EDA tools is stunning considering what a single yield point would do for a chip that generates hundreds of millions a year in revenue.