CANDE 2001 5-YEAR PREDICTIONS

1. Power consumption considerations will dominate all parts in high end and portable designs

2. At least 2 of the top 4 EDA companies will not be in the top 4

3. The design culture gap between architects and designers is a major problem

4. Speech recognition will be a major user interface in electronic systems

5. Generic fabrics that allow mask reuse with only a few custom masks will be popular again

6. HW/SW co-design is irrelevant! The real problem is SW/SW co-design - the optimal mapping of system function onto appropriate programmable processing resources and associated communications resources.(Note that programmable processing resources includes programmable processors, reconfigurable logic, and multi-function HW IP blocks)

7. A language question/war will still be unresolved

8. ASIC design styles will be largely replaced by highly programmable platforms

9. Integration of synthesis, placement and route will displace corresponding, independent point tools

10. Signal integrity will displace timing closure as the dominant design implementation problem

The rest of the predictions:

These 3 just missed out:

11. Design-for-cost EDA tools will reach the marketplace
12. Shanghai will be at least as important as Taiwan for fabrication
13. Low power will be the dominant design criteria for SoC – not speed and area

Voters were allowed to give multiple votes to predictions.
Votes marked with an (*) all came from one voter.

14. (5 votes each)
    - Linux is a major OS
    - Unix will still be the dominant OS for EDA development and use
    - (*)There will be viable tools for formal/property verification
15. (4 votes each)
    - Timing is the hardest characteristic to predict/estimate

- Validation/verification will continue to consume the majority of the design cycle
- Silicon will have a second active layer
- (*)The scarcity of design resources will be partially addressed by major changes in the VLSI design curriculum
- (*)Systems will integrate at the package level
- Stacked die in a package will delay the need for stacking transistors on top of each other on the same chip (multiple active layers)
- System design will be increasingly dominated by software
- SoCs won't include analog, digital & RF all together
- Hardware IP will become HW/SW IP
- C programmers will become system level designers
- Modeling will be diagram based

16. (3 votes each)
    - There will be a huge discontinuous breakthrough in verification tools and methodology
    - High level simulation is inadequate for verification
    - Chips implemented in the human body will be a common practice
    - Processor-based Star IP providers will emerge as a new industry segment
    - Open source will not be common in EDA
    - Performance problems! ASIC can't do it. Full custom is needed
    - Reconfigurable fabrics become mainstream
    - Digital & analog automated behavioral model extraction will remain unsolved
17. (2 votes each)
    - (*)The end of the road for optical lithography is in sight
    - 3D chip stack will become popular
    - System design tools will be hot "next year"
    - SystemC C/C++ based methodology will be popular as a platform for system design tools, but not for design entry
    - Reprogrammable engines (processors, ASIPs etc) will be the dominant implementation platform for SoCs
    - Software is so difficult that HS/SW co-design will be necessary
    - Power & performance optimization will come from optimized SW rather than HW
    - BIST will become inevitable for SoC
    - There will be a few dominant leaders for each embedded core segment
    - High levels of integration on processors will mandate design re-use
    - First pass design success remains elusive
    - ASIC hand-off will migrate to be RTL
    - FPGA cores will be in many SoCs
    - With shrinking device sizes, device & technology modeling will become more important again

18. (1 vote each)
    - Dominant CAD platform will be 64 bit
    - GDSII will no longer be the handoff to manufacturing
    - Real-time language translation of conversational speech will become a primary focus of research and some breakthroughs will occur
    - Static power analyses are inadequate for design completion
    - The dominant power source will be ambient energy
    - Look-up-tables will partially displace nands/nors as synthesis primitives
    - Analog & RF synthesis will be in common use
    - Dedicated HW will be profitable (economically viable) for wireless baseband
    - People building big systems with lots of HS & SW re-use will not use system level design tools
    - System level design will remain a private obsession. Real systems will be designed by SW engineers
    - I/O will undergo major increases in bandwidth per pin
    - SystemC will be the dominant system level design language
    - HW-dependent SW becomes a significant focus
    - On-chip parasitic inductance will not be extracted on signal nets (DRC)
    - The cost of test/transistor will start to decrease, tracking with the cost of manufacturing/transistor
    - The recession will last 10 years – the status quo for technology will cause a skip of 2 process generations (3 years)
    - Some progress will be made in the development of a 6th human sense – direct electronic interfacing to the brain
    - IP/Software sold on line via parametric functional and flow (methodology centric search criteria)
    - Virtual components will be integrated using standard APIs
    - Incredible design problems will grow the EDA pie
    - Soft errors will become important for logic design
    - Clockless design will be widely practiced
    - Tall-fat designers are needed for successful design

19. (0 votes)
    - Most CAD applications will run on clusters of computers
    - EDA for system level design will be replaced by domain-specific design services
    - High-Q crystal modeling becomes available for RF design
    - Integral passives will replace discrete passives in RF design
    - The Internet will swallow Telecom companies
    - You can automate cost reduction for highly-programmable platform-based designs
    - Analog designers will learn to use behavioral modeling languages