CANDE'2000

IEEE Circuits and Systems Society

April 2-4, 2000

Granlibakken Resort, Lake Tahoe, California.

Sunday, April 2:

6:30-9:00 PM Reception

Monday, April 3:

7:30-8:30 Breakfast

System-level Specification (Organizer: Rajesh Gupta, UC Irvine)

8:30-9:20 *Embedded & Real Time Systems Engineering with UML*,
Bruce Powell Douglass, Chief Evangelist, iLogix Corporation

9:20-10:10 *Architectural Synthesis and Exploration using Term Rewriting Systems*
Arvind, Professor, Laboratory for Computer Science, MIT

10:10-10:20 Break

10:20-11:10 *Requirements for System Specification Capture*
Mark Birnbaum, Director, Strategic Technology, Fujitsu Microelectronics, Inc.

11:10-12:00 *System Level Modelling - POV from the VSIA System Level Design Development Working Group*
Chris Lennard, Chair, VSIA System Level Design Development Working Group (DWG), and Cadence Design Systems

12:00-1 PM Lunch

Individual Discussions (Organizer: Al Dunlop, Bell Labs)

1 PM-5 PM Discussion topics may include: CANDE initiatives, CANDE projects, CAS, membership and recruiting, open items.

Dinner and Predictions (Organizer: Al Dunlop, Bell Labs)

6 PM-7 PM Wine and beer social hour

7 PM-9 PM Dinner & Predictions

Tuesday, April 4:

7:30-8:30 Breakfast

Designing for ultra low-power (Organizer: Ellen Yoffa, IBM Research)

8:30-9:20 *Microprocessor Thermal Trends and Their Management*
Frank Binns, VLSI Architect, Performance Micro. Div., Intel

9:20-10:10 *Low Energy Wireless System Design*
Jan Rabaey, Professor and Co-Director, Wireless Research Center, UC Berkeley

10:20-11:10 *SOI Challenges at sub 1V (sub 0.1um) Generation: a Circuit and Technology Perspective, and a Short Review of Recent Advances in DTMOS for sub 0.6V CMOS*
Fariborz Assaderaghi, Development Manager, Semiconductor Research & Development Center, IBM

11:10-12:00 *Portable Power Options for Future Applications*
Christina Lampe-Onnerud, Assoc. Dir., Battery Technology, Arthur D. Little

12:00-1 PM Lunch.