



2017 1st Electron Devices Technology and Manufacturing Conference (EDTM)

<http://ewh.ieee.org/conf/edtm/2017>

Extended Abstract Submission deadline: November 4th, 2016

One Page Text and One Page Figure

Notification for Acceptance: December 12th, 2016

Final THREE-Page Manuscript Submission Deadline: January 16th, 2016

Extended abstract could be accepted as final manuscript this year.

Conference Location: Toyama International Conference Center, Toyama, Japan

Date: February 28th to March 2nd, 2017

IEEE Electron Devices Technology and Manufacturing Conference (EDTM): The Inaugural EDTM (Electron Devices Technology and Manufacturing) conference is a full three-day conference to be held at Toyama International Conference Center, Japan from February 28th to March 2nd, 2017, fully sponsored by the IEEE Electron Devices Society (EDS). As semiconductor technology scaling challenges continues to grow, so should the industries collaborative efforts to overcome them must increase. EDTM is intended to serve as a forum for the electron devices community to collaborate on topics ranging from devices, materials, and tools, to create new and innovative technologies. EDTM will provide the following new formats.

1. Technical sessions

EDTM 2017 and beyond will have a strong specific technical focus, and this year's focus being on devices and process technologies for advanced applications, IoE (Internet of Everything) and related low-power devices, advanced memories, sensors, actuators, MEMS, bio.-chips, passive devices, and all types of (exploratory) devices related to advance applications and IoE. Papers/Posters on materials and processes for enabling above-mentioned devices building in heterogeneous integration such as 2.1, 2.5 and 3D structures using wafer-level packaging process (e.g.) are of great focus.

EDTM aims for highest quality, and all papers accepted would be subject to IEEE-EDS standard review processes and conference publishing guidelines. Accepted and presented papers will be published in EDTM proceedings. A selected number of high impact EDTM papers would be invited for the consideration of publication in the *IEEE Journal of Electron Devices Society* (J-EDS) as extended version of EDTM conference papers following the IEEE publication policy and J-EDS author-guidelines.

2. Education

✓ *Tutorials:* We will provide both the basic and advanced programs. Basic program will be presented in local language.

✓ *Poster sessions:* Primarily intended for young engineers and students. The best poster will be awarded in the conference.

✓ *Short courses:* Will bring high level programs.

3. Exhibition

Given the strong semiconductor manufacturing base in Asia, we intend to offer exhibits that will demonstrate products and technology. All of the exhibitors will have an opportunity to offer technical insight and share their knowhow. Moreover, we hope to offer Forum Making Session to engage and allow deeper discussions between device, material, and equipment engineers and technologists.

Steering Committee (EDS):

- Samar K. Saha
- Albert Z.H. Wang
- Paul K.L. Yu
- Fernando Guarin
- Ravi M. Todi (Chair)
- Subramanian Iyer

Local EDTM ExCom (Japan):

- Shuji Ikeda (tei solutions)
- Akira Toriumi (Univ. of Tokyo)
- Kazunari Ishimaru (Toshiba)
- Hitoshi Wakabayashi (Tokyo Tech)
- Seiichiro Kawamura (JST)
- Keiji Ikeda (Toshiba)
- Iriya Muneta (Tokyo Tech.)
- Masaaki Niwa (Tohoku Univ.)
- Hiro Akinaga (AIST)
- Ken Uchida (Keio Univ.)
- Shintaro Yamamichi (IBM Japan)
- Jiro Yumgami (Hitachi-Kokusai)

Secretariat:

- Ms. Mayumi Takita
- (JTB Communication Design, Inc.)
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Papers are solicited in the following areas

Devices and Manufacturing for “Cloud and Edge:” papers in all areas of device and manufacturing enhancing cloud and edge computing; high-performance devices include CMOS technology, platform technologies, stand-alone and embedded memory technologies, interconnects, optical interconnects, compound semiconductors, low-dimensional systems including 2D materials, nanowires, nanotubes, and quantum dots, 3D-IC. The devices for edge computing correspond to ultra-low power devices, energy harvester, RF devices, sensors, sensor networks, display, and actuators, MEMS, power devices, flexible and stretchable electronics, printed electronics, organic and inorganic displays.

Papers are also solicited on the manufacturing issues on process control, manufacturability, yield improvements, and failure analysis and related considerations.

Packaging and Manufacturing for “Cloud and Edge:” papers in all areas of advanced packaging and package-related manufacturing technologies for both cloud and edge applications of IoT, especially, heterogeneous integration technologies such as 2.1D, 2.5D and 3D integrations, wafer-level packaging and panel-level packaging are strongly encouraged; breakthrough technologies in ultra-fine-pitch interconnection, sub-micron package-level wiring, optical/wireless interconnect, power/sensor device packaging, control in thermal-expansion coefficient and thermal management are also recommended; package design methodology and technique for miniaturization of IoT edge sub-systems, and the manufacturability of all the technologies above are of course interested. Emerging topics, such as bio-compatible package, neuromorphic interconnection, and flexible/bendable package are very much welcome.

Process, Tools, and Manufacturing: papers in all areas of process, tools, and manufacturing systems with novel sensing technologies and artificial-intelligence and deep-learning algorithms; process and equipment including process module, process integration and process control, and equipment that improve device performance, reliability, yield or enabling new product are also solicited; the topics are substrates, isolation technologies, integration of heterogeneous channel materials, dielectrics and metal electrodes for gate stacks and MIM capacitors, shallow junctions, and silicides, low dielectric constant materials, contact and via processes, multi-patterning and EUV lithography, self-assembly techniques, deposition techniques include CVD, ALD and PVD, dry and wet etch techniques, cleaning, planarization, integration process for sensors, MEMS, RF devices, and photonics electronics, and process and tool design or process control techniques to reduce variation or improve reliability or yield.

Materials: papers in all areas of materials to achieve the higher performance and manufacturability, including materials for the deposition of films of semiconductor, magnetics, ferroelectrics, insulators, metals, liquid crystals are highly welcome; and to achieve their structures, the resist, organic films, etching gas, and CMP materials and their chemical materials, gas chemistries, wafers, filament, phase change memory materials, cost down, reliability, high yield, manufacturability are also in our scope. Innovative materials for sensor and actuator achieving cloud and edge computing are highly welcome.

Reliability & Modeling: papers in all areas of numerical, analytical (including compact/SPICE) and statistical modeling and simulation of electronic, optical or hybrid devices, their interconnect, and 2D / 3D integration; in context of materials, fabrication processes, and devices, e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport); Mechanical or electro-thermal modeling and simulation; Test structures and methodologies; Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability of materials, processes, and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; defect monitoring and control; manufacturing yield modeling, DFM, analysis, and testing.