EDTM 2018 - Advance Program

As of Mar 12, 2018

Day 2 - March 14, 2018

8:30-9:00 Main Hall (Shinsho-Hall A+B)
Opening

9:00-11:00 Main Hall (Shinsho-Hall A+B)
Plenary Session

9:00	9:40	Logic Technology Scaling to Continue Moore's Law	Mark T Bohr	Intel Corporation
9:40	10:20	2D Materials for Smart Life	Kaustav Banerjee	UCSB
10:20	11:00	Evolution of the GPU Device widely used in AI and Massive Parallel Processing	Toru Baji	NVIDIA

11:00-11:45 Main Hall (Shinsho-Hall A+B)
Exhibition Talks

11:45-13:15 Valencia (2F), Castilla (5F)
Lunch Break

13:15-14:30 Main Hall (Shinsho-Hall A+B)
Session 3M Device: Super Steep Slope Devices 1
Chair: Kejun Xia, NXP Semiconductors

13:15	13:40	Design Considerations of Ferroelectric Properties for Negative Capacitance MOSFETs	Saeidi Ali	Ecole polytechnique federale de Lausanne (EPFL)
13:40	14:05	Analysis of Negative Capacitance UTB SOI MOSFETs considering Line-Edge Roughness and Work Function Variation	Pin-Chieh Chiu	National Central University
14:05	14:30	Investigation of Fin-Width Sensitivity of Threshold Voltage for InGaAs/Si Channel Negative-Capacitance FinFETs	Shih-En Huang	National Chiao Tung University

14:55-15:30 Authors Interview

13:15-14:55 Room C (Conference Room 3)
Session 3C Material: 2D Related Materials
Chair: Iriya Muneta, Tokyo Tech. Co-Chair: Paul Berger, Ohio State Univ.

13:15	13:40	2D Materials for Ubiquitous Electronics (Invited)	Saptarshi Das	Pennsylvania State University
13:40	14:05	Synthesis and Characterization of Novel TMD: Rhenium Disulfide	Michael Daniel Valentin	University of California, Riverside
14:05	14:30	3D foams as a new thermal material for a variety of applications (Invited)	Hang Tong Edwin Teo	Nanyang Technological University
14:30	14:55	Anisotropic thermal conductivity of vertically self-ordered Nanocrystalline Boron Nitride thin films for thermal hotspot mitigation in electronics	Siu Hon Tsang	Temasek Laboratories@NTU

14:55-15:30 Authors Interview

13:15-14:55 Room D (Barcelona)
Session 3D Modeling & Reliability: Modeling for Reliability
Chair: Lining Zhang, Shenzhen Univ. Co-Chair: Xianping Chen, Chongqing Univ.

13:15	13:40	Modeling of Carrier Trapping and Its Impact on Switching Performance (Invited)	Mitiko Miura-Mattausch	Hiroshima University
13:40	14:05	Consistent Predictive Simulation of SRAM-Cell Performance Degradation Including Both MOSFET Fabrication Variation and Aging	Hiroaki Gau	Hiroshima University
14:05	14:30	Non-Universal Temperature Dependence of Hot Carrier Degradation (HCD) in FinFET: New Observations and Physical Understandings	Zhuoqing Yu	Peking University
14:30	14:55	Comprehensive 3D TSV Reliability Study on 14nm FINFET Technology with Thinned wafers	Cimino Salvatore	GLOBALFOUNDRIES

14:55-15:30 Authors Interview

14:55-15:30 Event Hall
Poster Viewing

15:30-16:45 Room C (Conference Room 3)
Session 4C Process: Dry Etching and Ion Implantation
Chair: Kazuo Nojiri, Lam Research Co-Chair: Yoji Kawasaki, Sumitomo Heavy Industries Ion technology Co., Ltd.

15:30	15:55	Atomic Layer Etching: Benefits and Challenges (Invited)	Thorsten Lill Bernd	Lam Research Corporation
15:55	16:20	Withdrawn		
16:20	16:45	Ion Implantation Synthesis of Si-doped HfO2 Ferroelectric Thin Films	Shinji Migita	AIST

16:45-17:00 Authors Interview

15:30-16:45		**Room D (Barcelona)**		
Session 4D		**Device: Advanced CMOS**		
Chair: Naoto Horiguchi, Imec		**Co-Chair: Gong Xiao, National Univ. of Singapore**		
15:30	15:55	Potential Influence of Surface Atomic Disorder on Fermi-level Pinning at Metal/SiGe Interface	Xuan Luo	The University of Tokyo
15:55	16:20	Enhanced Germanium-Tin P-Channel FinFET Performance using Post-Metal Anneal	Dian Lei	National University of Singapore
16:20	16:45	Polarity Control in WSe2 Field-Effect Transistors using Dual Gate Architecture	Hiroyuki Takagi	QNERC and Dept. of EE., Tokyo Tech.
16:45-17:00		**Authors Interview**		
16:45-18:00		**Event Hall**		
Poster Viewing				
18:30-21:00		**Portopia Hotel**		
Banquet				

Day 3 - March 15, 2018

8:30-9:45		**Room A (Shinsho-Hall A)**		
Session 5A		**Featuring: Artificial Intelligence and Enabling Devices 1**		
Chair: Kazunari Ishimaru, Toshiba Memory Corp.		**Co-Chair: Carlo Reita, CEA-LETI**		
8:30	8:55	Steep Slope Transistors for Quantum Computing (Invited)	Teodor Rosca	EPFL
8:55	9:20	Energy and Area Efficient Tunnel FET-based Spiking Neural Networks	Dinesh Rajasekharan	Indian Institute of Technology Kanpur
9:20	9:45	Electrode material dependence of resistive switching behavior in Ta2O5 resistive analog neuromorphic device	Hisashi Shima	AIST
9:45-10:40		**Authors Interview / Break**		
8:30-10:10		**Room B (Shinsho-Hall B)**		
Session 5B		**Package: Photonics Related Technologies**		
Chair: Eric Beyne, imec		**Co-Chair: Yoichiro Kurita, Toshiba**		
8:30	8:55	An Advanced CuCu Hybrid Bonding For Novel Stacked CMOS Image Sensor (Invited)	Yoshihisa Kagawa	Sony Semiconductor Manufacturing
8:55	9:20	Interfacial Failure Characterization of Electronic Packaging Component Using a Multiscale Modelling Approach	Xianping Chen	Chongqing University
9:20	9:45	Heterogeneous Integration of GaN LED on CMOS Driver Circuit for Mobile Phone Applications	Don Disney	GLOBALFOUNDRIES
9:45	10:10	Silicon Photonic Multiport Optical Switch and Its Control Electronics (Invited)	Hitoshi Kawashima	AIST
10:10-10:40		**Authors Interview / Break**		
8:30-10:10		**Room C (Conference Room 3)**		
Session 5C		**Modeling & Reliability: Device Modeling**		
Chair: Dondee Navarro, Hiroshima Univ.		**Co-Chair: Risho Koh, Renesas Electronics**		
8:30	8:55	Ballistic Mobility Model for QDD Simulation of Ultra-short Transistors	Delia Paulina Aguirre Fernandez	Integrated Systems Laboratory, ETH Zurich
8:55	9:20	Study on the Direct Relationship between Macroscopic Electrical Parameters and Microscopic Channel Percolative Properties in Nanoscale MOSFETs	Zhe Zhang	Institute of Microelectronics, Peking University
9:20	9:45	Thin-Film Transistor Compact Model and AMOLED Circuit Design Applications (Invited)	Ling Li	Chinese Academy of Sciences
9:45	10:10	A Smooth and Continuous Phase Change Memory SPICE Model for Improved Convergence	Dayong Liu	The Shenzhen Key Lab of Advanced Electron Device and Integration, ECE,
10:10-10:40		**Authors Interview / Break**		
8:30-10:10		**Room D (Barcelona)**		
Session 5D		**Yield & Manufacturing: DFM and Product Yield**		
Chair: Angelo Pinto, Qualcomm		**Co-Chair: Bill Nehrer, Consultant**		
8:30	8:55	Design and Technology Co-Optimization for exploring Power, Performance, Area and Manufacturability Trade-offs in Advanced FDSOI and FinFET Technologies (Invited)	Mahbub Rashad	Globalfoundries
8:55	9:20	Low Cost and Highly Manufacturable MOL/BEOL Constructs in 22FDSOI Technology for High Performance and Low Power Applications	Navneet Jain	GlobalFoundries Inc.
9:20	9:45	Pre-Tapeout Design for Yield Application: Design based Diffing, Pattern Analytics and Risk Scoring (Invited)	Yoshitaka Horikoshi	Cadence Design Systems, Inc.
9:45	10:10	Process Cost and Time in Minimal Fab to Fabricate Custom-made Microneedle Array with Extraction Tool	Sommawan Khumpuang	AIST
10:10-10:40		**Authors Interview / Break**		

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10:40-12:20		**Room A (Shinsho-Hall A)**		
Session 6A		**Process: Advanced Thin Film Technology**		
Chair: Yasutoshi Okuno, TSMC		**Co-Chair: Makoto Miura, Hitachi High-Technologies Corp.**		
10:40	11:05	Thin Film Process Technologies for Continued Scaling (Invited)	Gerrit Jan Leusink	TEL Technology Center, America, LLC
11:05	11:30	Technology Innovations in Selective ALD for Next-Generation Contacts and Vias (Invited)	Andrew Kummel	Univ. of California, San Diego
11:30	11:55	Chip-Level-Integrated nMISFETs with Sputter-Deposited-MoS2 Thin Channel Passivated by Al2O3 Film and TiN Top Gate	Kentaro Matsuura	Tokyo Institute of Technology
11:55	12:20	Strategies for Growing Perovskite Films on Nanostructured TiO2 for High Performance Solar Cell	Charles Surya	Nazarbayev University
12:20-13:50		**Authors Interview / Lunch Break**		
10:40-12:20		**Room B (Shinsho-Hall B)**		
Session 6B		**Material: Oxide Materials**		
Chair: Hiroyasu Yamahara, The Univ. of Tokyo		**Co-Chair: Pei-Wen Li, National Chiao Tung Univ.**		
10:40	11:05	Functional Oxide Engineering for Solar Energy Harvesting and Neuromorphic Devices based on Spintronics & Magnonics (Invited)	Hitoshi Tabata	The University of Tokyo
11:05	11:30	Superparamagnetic, nanocrystalline cobalt nickel zinc ferrite thin films, deposited at sub-200 oC for RF CMOS applications	Neelima Sangeneni	Indian Institute of Science
11:30	11:55	Nucleation-driven ferroelectric phase formation in ZrO2 thin films -What is different in ZrO2 from HfO2 ?-	Shigehisa Shibayama	The University of Tokyo
11:55	12:20	Direct Observation of Chemical States in ReRAM by Laser-based Photoemission Electron Microscopy	Toshiyuki Taniuchi	ISSP, The university of Tokyo
12:20-13:50		**Authors Interview / Lunch Break**		
10:40-12:20		**Room C (Conference Room 3)**		
Session 6C		**Device: 3D and MEMS**		
Chair: Osbert Cheng, UMC		**Co-Chair: Ken Uchida, Keio Univ.**		
10:40	11:05	Impact of 1um TSV via-last integration on electrical performance of advanced FinFET devices	Gaspard Hiblot	IMEC
11:05	11:30	Monolithic 3D (M3D) Complementary Metal-Oxide-Semiconductor (CMOS)-Nanoelectromechanical (NEM) Hybrid Circuits (Invited)	Woo Young Choi	Sogang University
11:30	11:55	Design Optimization Study of Reconfigurable Interconnects	Urmita Sikder	University of California, Berkeley
11:55	12:20	Fabrication and Characterization of Fully Depleted SOI MOSFETs on Ultrathin Circular Diaphragms Using Cost-Effective Minimal-Fab Process	Yongxun Liu	AIST
12:20-13:50		**Authors Interview / Lunch Break**		
10:40-11:55		**Room D (Barcelona)**		
Session 6D		**Featuring: Heterogeneous Integration**		
Chair: Mukuta Farooq, GlobalFoundries		**Co-Chair: Kamal Shikka, IBM**		
10:40	11:05	Fanout Wafer level Technology - A New Trajectory for Moore's Law Scaling	Rajendra D Pendse	Qualcomm
11:05	11:30	Heterogeneous Integration Using the Silicon Interconnect Fabric	Subramanian S. Iyer	UCLA
11:30	11:55	High-Density Fan-Out Technology for Advanced SiP and Heterogeneous Integration (Invited)	WonChul Do	Amkor Technology Korea
11:55-13:50		**Authors Interview / Lunch Break**		
13:30-14:30		**Event Hall**		
Poster Viewing / Exhibition				

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14:30-16:10		**Room A (Shinsho-Hall A)**		
Session 7A		**Modeling & Reliability: Reliability**		
Chair: Natarajan Mahadeva Iyer, Univ. of California				
14:30	14:55	Soft Error Rate from Planar to FinFETs On Bulk Vs SOI Processes (Invited)	Mahadeva Iyer Natarajan	Univ. of California, Los Angeles
14:55	15:20	Defect spectroscopy from electrical measurements: a simulation based technique	Luca Larcher	University of Modena and Reggio Emilia
15:20	15:45	A Novel Approach to Localize the Channel Temperature Induced by the Self-heating Effect in 14nm High-k Metal-gate FinFET	E. R. Hsieh	National Chiao Tung University
15:45	16:10	Understanding the impact of High-k Post Deposition Anneal Temperature on FinFET Reliability -Trade-offs, optimization and mitigation	Purushothaman Srinivasan	GLOBALFOUNDRIES
16:10-16:30		**Authors Interview**		
14:30-15:45		**Room B (Shinsho-Hall B)**		
Session 7B		**Featuring: Artificial Intelligence and Enabling Devices 2**		
Chair: Kazunari Ishimaru, Toshiba Memory Corp.		**Co-Chair: Carlo Reita, LETI**		
14:30	14:55	Deep Neural Network for Device Modeling	Yuan LEI	Hong Kong Applied Science and Technology Research Institute
14:55	15:20	A Two-terminal Electric-double-layer Synaptic Device with Short-term Plasticity	Jiabin Wang	Tsinghua University
15:20	15:45	Emulating the Short-Term Plasticity and Filtering of Biological Synapses with IZO-based Electric-Double-Layer Transistors	Xiang Wan	Nanjing University Of Posts And Telecommunications
15:45-16:30		**Authors Interview**		
14:30-15:45		**Room C (Conference Room 3)**		
Session 7C		**Material: Advanced Material Processes**		
Chair: Gil Nonato Santos, De La Salle Univ.		**Co-Chair: Ng Geok Ing, Nanyang Technological Univ.**		
14:30	14:55	Suppressing Oxidation-Enhanced Diffusion of Boron via Buried Epitaxial Oxygen-Inserted Layers in Silicon	Daniel Connelly	Atomera, Inc.
14:55	15:20	Gettering Mechanism in Carbon-cluster-ion-implanted Epitaxial Silicon Wafers using Atom Probe Tomography	Ayumi Onaka-Masada	Okayama Prefectural University
15:20	15:45	New Contact Metallization Scheme for FinFET and Beyond (Invited)	Junichi Koike	Tohoku University
15:45-16:30		**Authors Interview**		
14:30-16:10		**Room D (Barcelona)**		
Session 7D		**Device: Thin Film Devices**		
Chair: Yukinori Morita, AIST		**Co-Chair: Yi Yang, Tsinghua Univ.**		
14:30	14:55	Origin of High Mobility in InSnZnO MOSFETs	Nobuyoshi Saito	Toshiba Memory Corporation
14:55	15:20	Suppression of channel shortening effect for InGaZnO Thin-Film-Transistor	Junji Kataoka	Toshiba Memory Corporation
15:20	15:45	Radio-frequency Superiority of Poly-Si TFTs with T-Shaped Gate and Air Spacers for IoT Applications	Yu-An Huang	National Chiao Tung University
15:45	16:10	The Analysis for OLED property of the devices with various aperture ratio by Impedance Spectroscopy	Tomohiko Naganuma	Japan Display Inc.
16:10-16:30		**Authors Interview**		
16:30-17:30		**Event Hall**		
Poster Viewing with Refreshment				
17:30-19:00		**Room E (Valencia)**		
Women in Engineering / Young Professional Event				

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Day 4 - March 16, 2018

8:30-10:10 Room A (Shinsho-Hall A)
Session 8A Device: Super Steep Slope Devices 2
Chair: Yukinori Morita, AIST Co-Chair: Ken Uchida, Keio Univ.

8:30	8:55	On the dynamic characteristics of ferroelectric and paraelectric FETs	Ashwani Kumar	The University of Sheffield
8:55	9:20	Impact of Contact Resistance on 2D Negative-Capacitance FETs	Lu Po-Sheng	National Chiao Tung University
9:20	9:45	P-channel Super Steep Subthreshold Slope PN-Body Tied SOI FET: Possibility of CMOS	Takayuki Mori	Kanazawa Institute of Technology
9:45	10:10	Device Designs of III-V Tunnel FETs for Performance Enhancements through Line Tunneling	Chiu-Ting Wang	National Central University

10:10-10:40 Authors Interview

8:30-10:10 Room B (Shinsho-Hall B)
Session 8B Process: Ge Surface Process Control
Chair: Osamu Nakatsuka, Nagoya Univ. Co-Chair: Jiro Yugami, Hitachi Kokusai Electric Inc.

8:30	8:55	Rigidity enhancement of GeO2 by Y doping for reliable Ge gate stack	Tomonori Nishimura	The University of Tokyo
8:55	9:20	Anomalous Spectral Shape Evolution of Ge Raman Shift in Oxidation of SiGe	Yusuke Noma	The University of Tokyo
9:20	9:45	Interface Engineering of Ge-based Nanoelectronics Using Fluorinated Graphene (Invited)	Zengfeng Di	Chinese Academy of Sciences
9:45	10:10	Ge FinFET CMOS Inverters with Improved Channel Surface Roughness by Using In-situ ALD Digital O3 Treatment	G.-L. Luo	National Nano Device Laboratories

10:10-10:40 Authors Interview

8:30-9:20 Room C (Conference Room 3)
Session 8C Featuring: Featuring: Nanotechnology Featuring the 2D Materials 1
Chair: Iriya Muneta, Tokyo Tech. Co-Chair: Navakanta Bhatt, Indian Institute of Science

8:30	8:55	The Auger FET: a Novel Device Concept for Subthermal Switching (Invited)	James T Teherani	Columbia University
8:55	9:20	A graphene platform on silicon for the Internet of Everything	Francesca Iacopi	University of Technology Sydney

9:20-10:40 Authors Interview

10:40-11:55 Room A (Shinsho-Hall A)
Session 9A Device: Advanced Memory
Chair: Jae-Kyu Lee, Samsung Co-Chair: Jong-Ho Lee, Seoul National Univ.

10:40	11:05	Ultra-high-efficient Writing in Voltage-Control Spintronics Memory(VoCSM); the Most Promising Embedded Memory for Deep Learning	Yuichi Ohsawa	Toshiba Corp.
11:05	11:30	Experimental and Simulation Study of Resistive Switching Properties in Novel Cu/Poly-Si/TiN CBRAM Crossbar Device	Chand Umesh	King Abdullah University of Science and Technology
11:30	11:55	Reconfigurable Cell String Having FET and Super-Steep Switching Diode Operation in 3D NAND Flash Memory	Nagyong Choi	Seoul National University

11:55-12:10 Authors Interview

10:40-11:55 Room B (Shinsho-Hall B)
Session 9B Package: Fan-Out Technology
Chair: Yoichiro Kurita, Toshiba Co-Chair: Piyush Gupta, Qualcomm

10:40	11:05	The Evolution of Panel Level Packaging (Invited)	Rolf Aschenbrenner	Fraunhofer IZM
11:05	11:30	Development of Semiconductor Manufacturing System Integrating Wafer Process and Packaging Process Using a Half-Inch Sized Package	Fumito Imura	AIST
11:30	11:55	A Novel System-in-Package using High-Density Fan-out Technology for Heterogeneous Integration	SeungNam Son	Amkor Technology Korea

11:55-12:10 Authors Interview

10:40-11:55 Room C (Conference Room 3)
Session 9C Featuring: Nanotechnology Featuring the 2D Materials 2
Chair: Iriya Muneta, Tokyo Tech. Co-Chair: Navakanta Bhatt, Indian Institute of Science

10:40	11:05	2D Electronics – A Promising Option or a Type C Hype Cycle? (Invited)	Frank habil. Schwierz	TU Ilmenau
11:05	11:30	New device concepts, transistor architectures and materials for high performance and energy efficient CMOS circuits in the forthcoming era of 3D integrated circuits (Invited)	David Esseni	University of Udine
11:30	11:55	Device Performance of 2D Layered Material Transistors and Their Challenges: A Theoretical Study (Invited)	Geng-Chiau Liang	National University of Singapore

11:55-12:10 Authors Interview

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10:00-12:20 Room D (Barcelona)
Symposium on Frontier Researches of Functional Oxide Devices and Materials

12:10-13:30 *No lunch is served on 16. Please see the map in the congress bag for nearby restaurants.
Lunch Break

13:30-13:40 Room A (Shinsho-Hall A)
Poster Award Ceremony

13:40-15:20 Room A (Shinsho-Hall A)
Session 10A Yield & Manufacturing: Yield Analysis and Improvement
Chair: Bill Nehrer, Consultant Co-Chair: Angelo Pinto, Qualcomm

13:40	14:05	Short Flow Characterization Vehicle (Test Chip) Usage in Advanced Technology Development and Yield Improvement (Invited)	Tomasz Brozek	PDF Solutions
14:05	14:30	Fast Defect Reduction to Enable Customer Yield Ramp (Invited)	Roman M Mostovoy	Applied Materials
14:30	14:55	Particle removal characteristics in liquid flow during wafer rotation	Naoyuki Handa	EBARA Corporation
14:55	15:20	Trends in Manufacturing Productivity and Yield for Interconnected Devices and Industries (Invited)	Rebecca Mih	Lam Research

15:20-15:40 Authors Interview

13:40-15:20 Room B (Shinsho-Hall B)
Session 10B Material: Materials Transistors
Chair: Paul Berger, Ohio State Univ. Co-Chair: Yang Xu, Zhejiang Univ.

13:40	14:05	Single-fabrication-step Ge Nanosphere/SiO2/SiGe heterostructures: A key enabler for realizing Ge MOS devices	Po-Hsiang Liao	National Central University
14:05	14:30	Withdrawn		
14:30	14:55	The Sub-micron GaN HEMT Device on 200mm Si(111) Wafer with Low Wafer Bow	Chieh-Chih Huang	LEES, Singapore-MIT Alliance for Research and Technology
14:55	15:20	Flexible Printed Organic Thin-Film Transistor Devices and IoT Sensor Applications (Invited)	Shizuo Tokito	Yamagata University

15:20-15:40 Authors Interview

13:50-16:55 Room D (Barcelona)
Symposium on Frontier Researches of Functional Oxide Devices and Materials

13:40-17:00 Room E (Valencia)
JST / CREST / 2D Workshop in Kobe

Poster Presentations

P-1	Thermal-Performance Improvement of Collector-Up Heterojunction Bipolar Transistors by Graphene Packaging	H. C. Tseng	Kun Shan University
P-2	Analysis of Temperature Distribution in Stacked IC with Three Tier Structure	Satoshi Ushida	Toyama Prefectural University
P-3	Device Design Parameter for Desired DC Gain and Hysteresis-Free FDSOI NCFETs	Shruti Mehrotra	Indian Institute of Technology Kanpur
P-4	Ferroelectric Characteristics of Ultra-thin Hf1-xZrxO2 Gate Stack and 1T Memory Operation Applications	M. H. Lee	National Taiwan Normal University
P-5	Embedded Tunable Near Infrared Sensor with Programmable Potential Barrier on Nano-meter CMOS Platforms	Zih-Hong Chen	National Tsing Hua University
P-6	Potential and Limitations of HfZrO2-based Ferroelectric MOSFET For Low Power Applications	Yang Li	National University of Singapore
P-7	Paraelectric-Ferroelectric Transition in Hafnium-Oxide-Based Ferroelectric Memory	Chia-Chi Fan	National Chiao-Tung University
P-8	Thermoelectric Characteristics of Rapid-Melting-Grown SiGe Wires Measured by Peltier Cooling Experiment	Shuichiro Hashimoto	Waseda University
P-9	Cryogenic Characteristics of Ge channel Junctionless Nanowire Transistors	Chuanchuan Sun	Tsinghua University
P-10	1.0 THz detection by InAs quantum-well MOSHEMT using GSG THz probe	Eiji Kume	IRspec Corporation
P-11	DESIGN AND PERFORMANCE OF pi-TYPE THIN-FILM NANO-TEG USING VACUUM/SiO2-HYBRID INSULATION MODULE STRUCTURE	Toshimasa Seino	Tokyo Institute of Technology
P-12	Dynamic Thermal Characterization of Microheater in Semiconductor Metal Oxide based Gas Sensor	Ravi Shankar	STMicroelectronics Pte Ltd
P-13	Multibit Memory Cells Based on Spin-Orbit Torque Driven Magnetization Switching of Nanomagnets with Configurational Anisotropy	Wasef Shaik	King Abdullah University of Science and Tehnology
P-14	Implications of 3-Dimensional Scaling Rules on a 1.2 kV Trench Clustered IGBT	Peng Luo	The University of Sheffield
P-15	MEMS FLUXGATE MAGNETOMETER WHOSE SOLENOID COIL ARE WINDED BY A NOVEL WAFER-LEVEL LIQUID ALLOY FILLING METHOD	Jiebin Gu	State Key Laboratory of Transducer Technology
P-16	Quadrupole-electrode-integrated micropores for selective single-particle detections	Tomoki Hayashida	ISIR
P-17	Domain size effects on thermoelectric properties of p-type Ge0.95Sn0.05 layers grown on GaAs and Si substrates	Yukihiro Imai	Nagoya University
P-18	Low thermal budget fabrication of poly-Ge1-xSnx thin film thermoelectric generator	Kouta Takahashi	Nagoya University
P-19	HAXPES evaluation of ferroelectric HfSiO MIM capacitor	Koji Usuda	TOSHIBA CORPORATION
P-20	Cu cone inserted CBRAM device fabrication and its improved switching reliability induced by field concentration effect	Hae Jin Kim	Seoul National University
P-21	Study on the Effect of Hf Oxide Film Sputtering Condition on Resistive Random Access Memory Properties	Atsushi Azuma	Kansai University
P-22	Novel Technique for Production-Yield Enhancement of Semiconductor Devices	Shiro Ninomiya	Sumitomo Heavy Industries Ion Technology Co., Ltd.
P-23	High Aspect Ratio InAs fins Fabrication with sub-30nm fin width for FinFETs	Maneesha Rupakula	Ecole Polytechnique Federale de Lausanne
P-24	Position Control and Gas Source CVD Growth Technologies of 2D MX2 Materials for Real LSI Applications	Toshifumi Irisawa	AIST
P-25	Annealing Effect on Amorphous Indium-Zinc-Tungsten-Oxide Thin-Film Transistors	Qun Zhang	Fudan University
P-26	Atomic layer deposition(ALD) of Ru thin film on Ta2O5/Si substrate using RuO4 precursor and H2 gas	Cheol Hyun An	Seoul National University
P-27	Effect of Activation and Stress Conservation in Si0.7Ge0.3:B after Two-step Microwave Annealing	Tai Chen Kuo	National Cheng Kung University
P-28	Analysis of DC Self Heating Effect in Stacked Nanosheet Gate-All-Around Transistor	Min Jae Kang	Imperial College London
P-29	Self-Heating-Effect-Free p/n-Stacked-NW on Bulk-FinFETs and 6T-SRAM Layout	Eisuke Anju	Tokyo Institute of Technology
P-30	Physics-based Compact Modeling of MSM-2DEG GaN-based Varactors for THz Applications	Ahtisham Ul Haq Pampori	Indian Institute of Technology Kanpur
P-31	Body Bias Dependence of Hot Carrier Degradation (HCD) in Advanced FinFET Technology	Jiayang Zhang	Peking University