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High-speed, mixed-signal emulation for power system dynamic analysis

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Abstract: **This paper presents two different demonstrators of electronic hardware platforms, dedicated to power system emulation. They use DC emulation approaches of an AC power system. Both demonstrators focus on the speeding-up of the temporal analysis of a power system. The first demonstrator proves the feasibility of such programmable hardware. Moreover, comparison with a reference numerical simulator is used to confirm the accuracy of obtained results. The effect of analog-to-digital (A/D) and digital-to-analog (D/A) electronic conversion on the accuracy is also analyzed. The second hardware platform aims to improve generator and load models. At the same time, it also increases the flexibility of the hardware demonstrator platform.**

Index Terms: **analog emulation, mixed-signal emulation, power system computation, microelectronics, VLSI technology**

I. Introduction

The constantly increasing power consumption combined with the rising complexity of power systems clearly highlights the need for a much faster than real-time power system simulator, dedicated to temporal analysis (transient analysis, voltage regulation and frequency regulation). Such a tool is needed to anticipate the behavior of the power system, using the current steady state as its starting point and then applying typical scenarios. Through this process, it becomes possible to determine the weaknesses of the power system. The faster this power system simulator operates, the bigger is the number of scenarios that can be simulated in a given time-span. Thus, the most important characteristic of the simulator is the time scaling factor ψ. It is defined as the ratio between real time and simulation time.

Existing simulation methods are based on numerical algorithms solved with conventional computers. Their time scaling factors ψ are too small (i.e. simulators are too slow) to be used for real time exploitation of the power system. Moreover, their computation speed is related to the size of the grid. This is problematic because of the set of differential equations that need to be solved on each generator/load node at each computation step. All differential equations are linked together through the power grid. Thus, a dedicated architecture, which is especially developed for this problem, is much more appropriate than a conventional, pipelined architecture.

In the past, research was mainly focused on parallelizing the computation in order to accelerate simulation speed. But it has been shown that massive parallel digital computation is not a convenient solution to increase the speed of temporal analysis [5]. Indeed, when matrix resolution of the Kirchhoff network equations is separated for parallel computing, the communication time between computers becomes an important limitation. Rather than solving the Kirchhoff network equation using heavy numerical matrix algorithms, we can use an instantaneous analog Kirchhoff network equation-solver to accelerate simulation time. This latter is then connected to separate generator/load equation solvers in order to increase the speed even more. Generator/load equation solvers can be implemented by means of analog or digital electronic functions. An analog-to-digital A/D and digital to analog D/A conversions circuitries helps to create the interface between the analog world and the digital processing. This proposed architecture is shown in *Figure 1*.

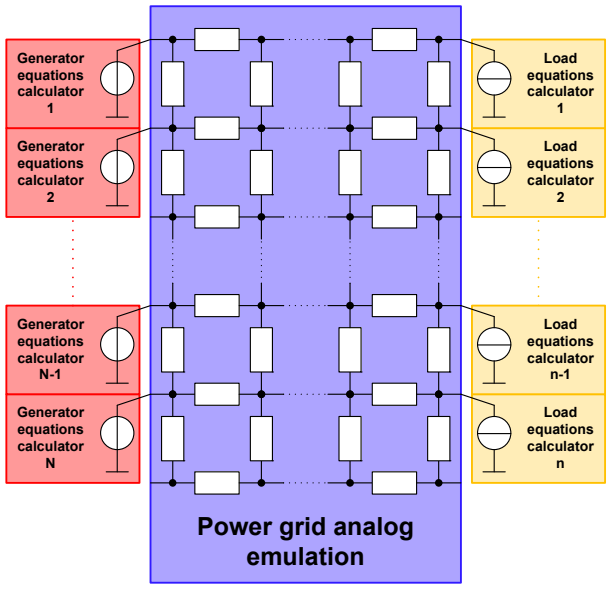

Figure-1 : *Analog Kirchhoff network equation-solver connected to separate generator/load equation-solvers*

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On-chip integration is essential for emulating a real power system (miniaturization and signal-to-noise ratio reduction). Thus, the final objective of this field is the realization of a fully integrated programmable power system on-chip, containing between hundreds and thousands of nodes.
The above-described computation tool (*Figure 1*) has already been developed using fully analog emulation [1]. Current research is focused on two different approaches: DC [1] [2] [3] and AC [4] emulation. Both approaches preserve the grid topology.
The emulation approach consists of a mapping between the real grid and its analog emulation scheme. It allows the computation of the power that is flowing through the grid branches. At the same time each node of the grid is connected to an electronic solver, which models the generator/load in order to compute dynamic phenomena (i.e. through swing equation resolution).
The AC emulation [4] can be seen as the downscaled model of the real power system. Hence, voltage and current are downscaled and the operating frequency is increased to 5 MHz. Thus, the system can operate up to 100 000 times faster than real time. Shrink factors link the values between real components and the emulated ones, such as resistances, inductances and capacitances.
DC emulation [1] [2] [3] is a mathematical representation of the real power system solved by analog computation. It provides the envelope of power system signals. This implies that real and imaginary parts of voltage and current vectors can be directly measured on chip.
This paper is organized as follows: we first present the DC model of the power network and explain how speed enhancement is possible by means of analog emulation (Section II). We then present two mixed-signal implementations (analog components combined with numerical components) of the DC emulation approach.

- The first implementation validates the concept of mixed signal DC emulation using a power system topology with classical model generators and constant current loads (Section III). Comparisons with a numerical reference simulator are provided. A/D and D/A converter choices are then discussed.

- The second implementation aims to enhance generator and load model, increasing at the same time the flexibility of the hardware demonstrator platform (Section IV).
Both approaches have been realized and tested.

II. Speed enhancement by emulation: Mathematical background

A. DC model of the grid

The DC model [1] [3] that is considered here takes the transmission line inductances into account but neglects the resistive parts. The relation linking the real and imaginary part of the node voltages with the real and imaginary part of the current injected in node i is given by (i):

$$\underline{I_i} = \underbrace{-\sum_{j=1}^{n}\left(\frac{1}{X_{ij}}\cdot\Im m\{U_j\}\right)}_{Network\ A} + \underbrace{j\cdot\sum_{j=1}^{n}\left(-\frac{1}{X_{ij}}\cdot\Re e\{U_j\}\right)}_{Network\ B} \quad (i)$$

Equation-1 : *Mathematical representation of the grid*

Hence, the analog Kirchhoff network equation-solver can be implemented by two equally resistive networks.

B. Classical model of the generator

The analog emulated generator circuitry solves the well known swing equation (ii) using two programmable gm-C filters [7] mounted in series (iii). The analogy of the electrical angle δ is a voltage V_2, the electrical power becomes a current and the inertia of the synchronous machine is given by both gm-C_1 and gm-C_2 filter products (*Equation 2*).

$$\underset{(a)}{\left(\frac{2\cdot H_i}{\omega_0}\right)}\cdot\underset{(b)}{\left(\frac{d^2\delta_i}{dt^2_{powerworld}}\right)} = \underset{(c)}{\left(P_{m_i} - P_{e_i}\right)} \quad (ii)$$

$$\underset{(a')}{\left(\frac{C_1}{g_{m1}}\cdot\frac{C_2}{g_{m2}}\cdot\frac{1}{R}\right)}\cdot\underset{(b')}{\left(\frac{d^2V_2}{dt^2_{emulator}}\right)} = \underset{(c')}{\left(i_{m,emulator} - i_{e,emulator}\right)} \quad (iii)$$

Equation-2 : *Analogy between the swing equation and its analog emulation (a ≡ a', b ≡ b' & c ≡ c')*

The voltage input of the first integrator is proportional to the difference between the mechanical power and the electrical power. The electrical power itself is provided by the generator to the network and computed using the measured currents (real and imaginary) flowing to the analog network.
It becomes possible to link the real power world and the analog emulation using the scaling factors ψ and Λ (iv). Where ψ is the ratio between the real and the emulated time and Λ is the ratio between the real and the emulated voltage [V/pu].

$$\frac{g_{m1}}{C_1}\cdot\frac{g_{m2}}{C_2}\cdot R\cdot\left(i_{m,emulator} - i_{e,emulator}\right) = \dots$$

$$\dots = \frac{f_0}{H_i}\cdot\left(P_{m,power\ wold} - P_{e,power\ world}\right)\cdot\Psi^2\cdot\Lambda \quad (iv)$$

Equation-3 : *Link between power world and analog emulation*

Increased speed is due to the much smaller time constants in analog emulation implementation compared to the real-world power time constants. Nevertheless, speed is limited by parasitic effects, the signal-to-noise ratio and also by the time delay of analog to digital (A/D) and digital to analog (D/A) conversion. As shown in Equation 4, time scaling factors from 100 to 100 000 can reasonably be achieved.
.

$$\Psi = \frac{dt_{powerworld}}{dt_{emulator}} = 100...100'000 \quad (v)$$

Equation-4 : *Time scaling factor definition* ψ

III. First Prototype Implementation and Results

As described in [3], a fully programmable demonstrator has been realized on printed circuit boards (PCBs). A simple reference topology has been used with three generators connected to one load (*Figure 2*).

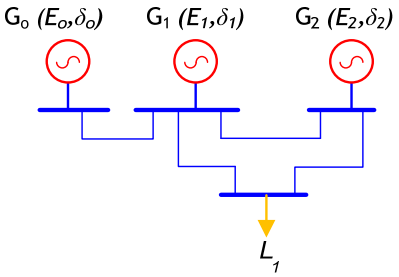

Figure-2 : *Simple reference topology*

The overall system is composed of four PCBs, including two programmable generator boards and one board containing the emulated grid and load. As already mentioned, the grid is emulated by two purely resistive and equal networks, whereas the load is emulated as a constant current source. All components are reprogrammable. The fourth board is used for interconnecting purposes and power supply. The suitable parameters and scenarios can be set through a graphical computer interface and the hardware can then be programmed via USB.

A microcontroller is used for sine and cosine computation as well as for calibration of the components and dynamic compensation of the loop offset. The speed of the chosen A/D and D/A converters connected to the microcontrollers determines the limitation of the time scaling factor ψ. For this implementation the time scaling factor is equal to ψ=100.

A. Scenario for measures and comparisons

We decided to use the same reference scenario and the same topology for measures and comparisons. The characteristics of the power system components are shown in Table 1.

	Parameter	Value	Unit
Generator 1	Active power	0.7	[pu]
	Reactive power	0.25	[pu]
	Inertia	4.2	[s]
	Transient reactance	0.35	[pu]
Generator 2	Active power	1.1	[pu]
	Reactive power	0.4	[pu]
	Inertia	2.1	[s]
	Transient reactance	0.3	[pu]
Load	Active power	1.85	[pu]
	Complex power	-0.4	[pu]
Line G_B-G_1	Line reactance	0.1	[pu]
Line G_1-G_2	Line reactance	0.18	[pu]
Line L-G_1	Line reactance	0.2	[pu]
Line L-G_2	Line reactance	0.1	[pu]

Table-1 : *Characteristics of the emulated and simulated power system*

The applied scenario is as follows (*Figure 3*):

(a) Emulation of the steady-state conditions using the values computed through load flow.
(b) Three-phase short-circuit between G2 and L1 in the middle of this transmission line.
(c) Disconnection of the short-circuited transmission line after a certain time.

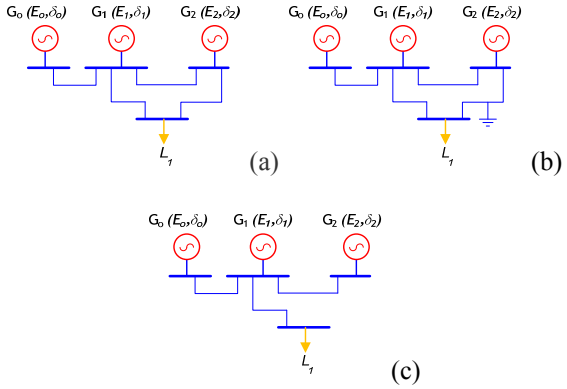

Figure-3 : *Scenario applied on reference topology*

B. A/D and D/A converters sizing technique

The accuracy of the mixed signal implementation results is dependant on the A/D and D/A converter characteristics. Simulation has been realized in order to meet the accuracy of the system. Two simulations have been done for sizing the A/D and D/A converters of each swing equation circuit. The scenario proposed in *Figure 3* is applied and the short circuit time is set to 700us (emulated time) or 3.5 oscillations of 50Hz in order to compare the results. The simulations results are compared with the results obtained by a pure analog swing equation circuit. First simulations aim to highlight the frequency results' dependency on the converters. *Figure 4* and *Figure 5* show the generator's electrical angle δ for different converter frequencies. Curves show that a conversion frequency that is too low (related to ψ=100) overevaluates the oscillation amplitude after the fault. An acquisition frequency

between 100kHz and 200kHz is sufficient in order to meet with less than 2 degrees error in the numerical simulation results over a period of 50ms (emulated time) after the fault.

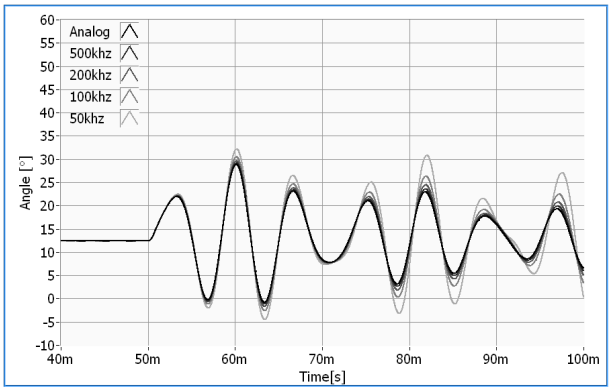

Figure-4 : *Electrical angle of generator 1 for different acquisition frequencies*

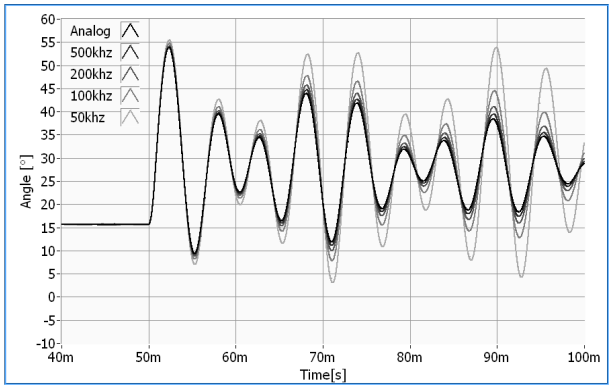

Figure-5 : *Electrical angle of generator 2 for different acquisition frequencies*

The second simulation emphasizes the dependency of the converter resolution. As seen in the first simulations, *Figure 6* and *Figure 7* show that a converter resolution that is too low overevaluates the oscillation amplitude. Simulations highlight that a resolution of 6 bits is not sufficient to meet with less than 2 degrees of error in the numerical simulation results. A resolution of 8 bits is shown to be sufficient to obtain less than 2 degrees of error during the 50ms (emulated time) after the fault.

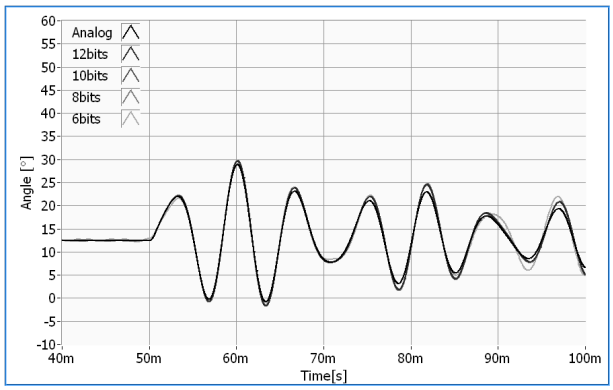

Figure-6 : *Electrical angle of generator 1 for different converter resolutions*

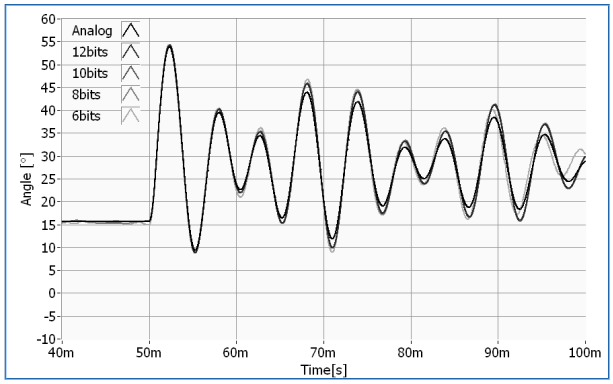

Figure-7 : *Electrical angle of generator 2 for different converter resolutions*

Finally, a frequency acquisition of 120kHz has been implemented in order to fulfill the discussed specifications. Converter resolution of 10bits A/D and 12bits D/A have been choosen.

C. Comparison - simulation vs. emulation results

In order to validate the emulation approach, a reference simulator based on numerical algorithms was realized using Labview. Numerical simulations and measured mixed-signal emulation results were then compared using the reference topology with a typical scenario (*Figure 3*).

Two different comparisons (qualitative and quantitative comparisons) have been carry out in order to validate the DC emulation approach. The qualitative comparison consists of validating the behavior of the electrical angle δ of the emulated generators (*Figure 8*). Emulated results are compared to the numerical reference simulator. The scenario used for this validation is the same as in *Figure 3*. Scales highlight that the obtained speed improvement is ψ=100.

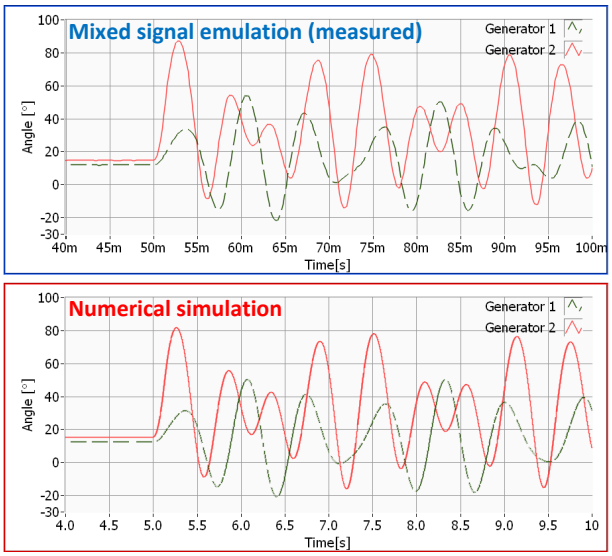

Figure-8 : *Results comparison for a short-circuit time of 120ms (real time) after 5s steady state. ψ=100*

The quantitative comparison plainly shows that the critical short-circuit clearing time is viable. Consequently, the software of the programmable demonstrator has been modified. A searching algorithm tests the same scenario as in *Figure 3* while increasing the clearing time until one of the two generators desynchronises with the power system. It is possible to limit the range of simulation time to the first oscillations because the classical generator model is used and thus the decision about stability can be made after the first oscillation. In order to put the emulator back into its steady state after a simulation is launched, a high damping is applied on both generators after few oscillations.
Figure 9 and *Figure 10* show the measured electrical angle. In this example the clearing time for the first simulation is 100us (emulated time) and is increased by 100us (emulated time) between each simulation. The emulation stops when one of the generators desynchronyses with the power network (critical clearing time is reached).

Figure-10

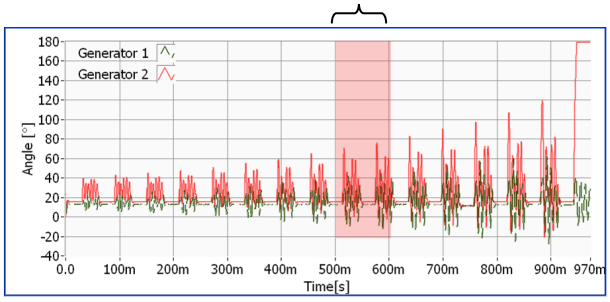

Figure-9 : *Generator's angle measurements during crtitical clearing time searching (measured)*

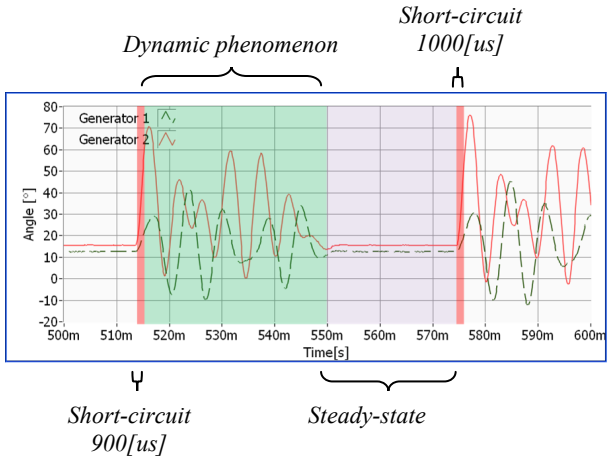

Figure-10 : *Zoom on Figure 9*

A measurement of the circuit resolution has been taken by reducing the step of the clearing time algorithm to 10us between two scenarios (emulated time). A set of a hundred measurements of the critical clearing time has also been taken and the results are presented in *Figure 11* and *Table 2*.

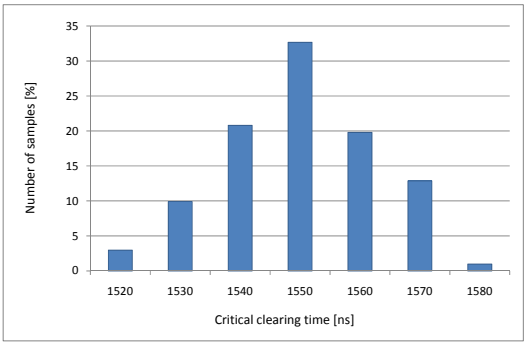

Figure-11 : *Results of searching the critical clearing time (100 simulations)*

Mixed signal emulation critical clearing time@ψ=100. *Measured*	*Numerical simulation critical clearing time*
Mean value: $T_{critical\ clearing\ time} = 1550[us]$ *Standard deviation:* $\sigma_{T\ critical\ clearing\ time} = 12.8[us]$	$t_{critical\ clearing\ time} = 169[ms]$

Table-2 : *Results of searching the critical clearing time comparison*

Before starting the emulation process, the generator and load model circuits need to be accurately calibrated [8]. DC offset errors also need to be cancelled [9] in order to meet the precision of numerical simulation. A manual trimming on gm-C filters is added. Nevertheless, the emulation underevaluates the critical clearing time of 13ms (real time) or 8%. An automatic procedural calibration [10] should, in future implementations, solve this issue by using more precise analog components as a reference [11] [12]. However, both comparisons show that mixed signal emulation is an excellent trade-off in terms of speed, precision and facility of calibration for transient stability computation.

IV. Model Enhancement

The above presented hardware is based on the classical model of the generator. Hence, the validity of its results is limited to a short time (~5s) after a sudden topology change. This drawback can be eliminated using Park equations instead (Equation 5), which consists of solving the excitation winding equation in the direct axis (viii), the damper winding equation in the quadrature axis (ix) and the algebraic stator equation (x & xi) at the same time as the swing equation (vii). By adding regulators (i.e. voltage and mechanical power regulators), the generator model could be enhanced even further. The first hardware does not allow the implementation of enhanced models; therefore a new hardware platform is necessary.

$$\frac{2\cdot H_i}{\omega_0}\cdot\frac{d^2\delta}{dt^2} = P_m - P_e \quad (vi)$$

$$P_e = U_q\cdot I_q + U_d\cdot I_d \quad (vii)$$

$$\frac{dE'_d}{dt} = \frac{1}{T'_{q0}}\left[-E'_d - \left(x_q - x'_q\right)\cdot I_q\right] (viii)$$

$$\frac{dE'_q}{dt} = \frac{1}{T'_{d0}}\left[E_{fd} - E'_q + \left(x_d - x'_d\right)\cdot I_d\right] (ix)$$

$$E'_d = U_d + R_s\cdot I_d + x'_q\cdot I_q \quad (x)$$

$$E'_q = U_q + R_s\cdot I_q - x'_d\cdot I_d \quad (xi)$$

Equation-5 : *Park equations [6]*

The fundamental difference between the classical model implementation and the enhanced model implementation is the connection between the generator and the analog grid. The synchronous transient reactance x'_d of the classical generator is contained in the analog grid. As a consequence, a programmable resistance needs to be added between the voltage output and the analog grid (*Figure 12*). The synchronous reactance of the enhanced model is directly computed through the model equations. Therefore, no resistance is added between the generator and the analog grid (*Figure 13*).

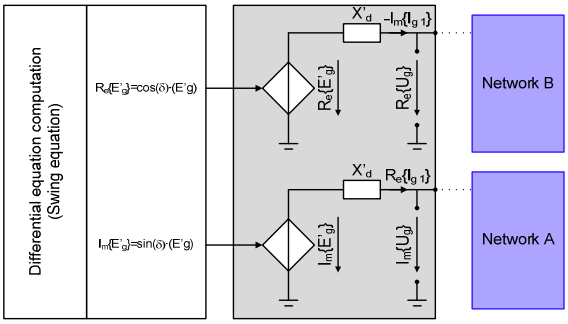

Figure-12 : *Electronic implementation of the classical generator*

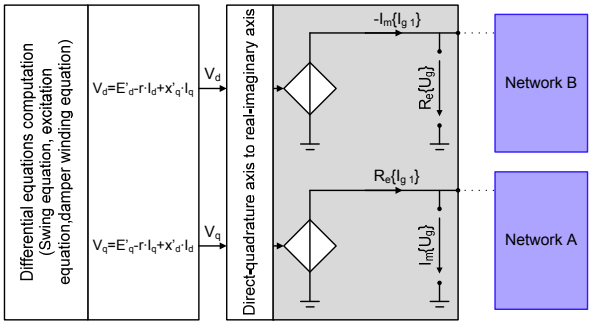

Figure-13 : *Electronic implementation of the enhanced generator*

Enhanced models for the load (constant impedance load and constant power load) can also be implemented by means of a controlled curent or a controlled voltage source. They can be implemented with the DC model of the grid.

V. Hardware Platform for Model Development and Evaluation

The first hardware presented in paragraph II is a fixed implementation of a given model suitable for integrated circuit implementation. In order to easily handle any model improvement or modification, a new flexible hardware platform has been developed and implemented. It contains embedded processors on generic boards connected with analog buses in an array (*Figure 14* and *Figure 15*). It uses purely numerical algorithms to compute, on separated hardware, the generator/load model equations. The mathematical grid model is emulated in the same way as the first presented prototype was. The generator and the load model are implemented using powerful 32 bit microcontrollers connected to appropriate analog interfaces. Therefore, it is possible to speed-up prototyping by implementing different generator and load models by means of software codes.

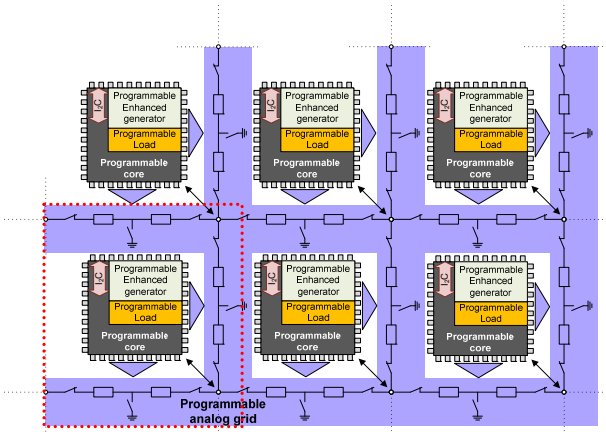

Figure-14 : *Architecture of the new programmable hardware platform*

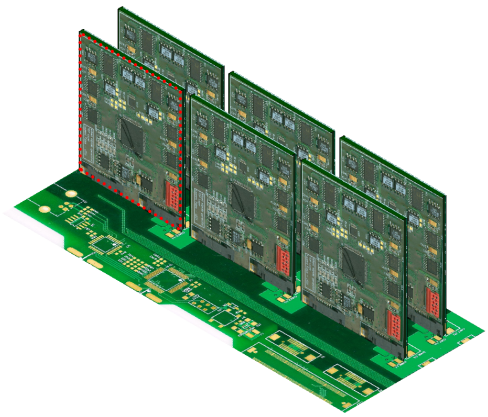

Figure-15 : *Realization of the new programmable hardware platform*

Fully reprogrammable boards have been realized. Each board can be programmed as a transmission line and/or a generator and/or a load using an I2C bus interface (*Figure 16*). Both current and voltage can be measured at the connection between the board and the analog grid.

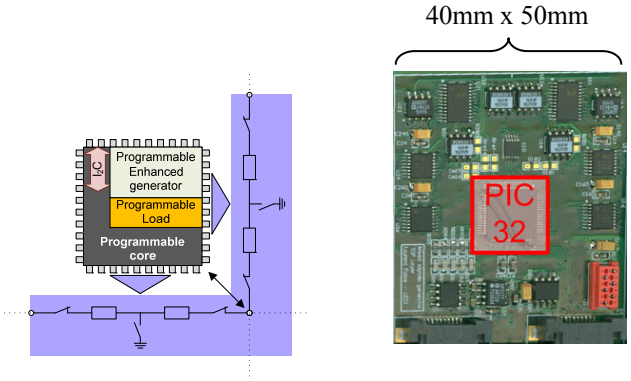

Figure-16 : *Programmable board*

Each board includes both configurable resistive analog networks A and B. As seen in Equation 1, network A contains the imaginary part of the voltage related to the real part of the current. Network B contains the real part of the voltage related to the imaginary part of the current. The model of each generator/load can be configured as a controlled current-source or a controlled voltage-source by means of analog switches mastered by the microcontroller. The overall architecture of the module is shown in *Figure 17*.

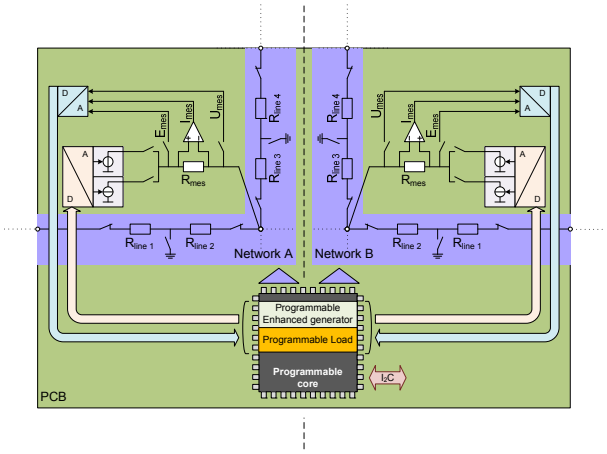

Figure-17 : *Architecture of the board (schematic)*

Figure 18 shows the placement of both network A and network B as well as the analog interfaces of the board. High precision analog circuits allow the accurate calibration of the circuit.

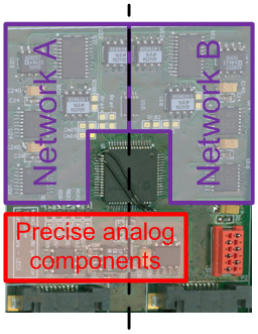

Figure-18 : *Architecture of the board (realization)*

VI. Conclusion

This paper focuses on increasing the speed of power system simulation, using an electronic emulation approach. The DC emulation approach of AC power system is presented and validated, by means of a mixed-signal demonstrator based on the classical model of the generator, and with the constant current load model.

Using a reference topology and a reference scenario, results of the mixed-signal demonstrator have been compared to numeric simulation results. Dynamic behavior and critical short-circuit time simulations were performed. This paper has shown that mixed signal emulation is an excellent trade-off in terms of speed and precision. Electronic calibration of the circuit is an important factor to consider in achieving accuracy.

In this paper, we also presented and implemented a second flexible demonstrator. Its aim is to create a new development platform for generator/load model enhancements. This flexible approach is not restricted to DC model implementation. It could be used as a development platform for other possible power system electronic emulation approaches. In order to miniaturize the mixed-signal emulator, a programmable power system on-chip is currently being designed. This integrated circuit is functionally equivalent to the programmable board and uses CMOS AMS 0.35µm technology.

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