美洲中國工程師學會
Chinese Institute of Engineers/USA
San Francisco Bay Area Chapter

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CIE/USA-SF EPMC Workshop

2.5D/3D Solution Workshop

Information technology has experienced revolutionary progress over the past several decades. Escalating demand for electronic devices with improved performance, functionality and mobility has compelled innovative enabling technologies in packaging technology, thus evolving from conventional board level assembly to two types of system-level integration: System on Chip (SoC) and System in Packaging (SiP). However, both integration technologies are already fast approaching their physical limits in addressing contemporary and future demands due to their limited interconnect bandwidth.

Through Silicon Via (TSV) technology holds the key to eliminating chip-to-chip interconnect constraints and the potential to enable new disruptive architectural solutions.
This half-day workshop will cover recent developments in enabling technologies for 2.5D/3D solutions based on TSVs, and design processes of 2.5D/3D technology including electrical, mechanical and thermal issues.

Date: March 7, 2015 (Saturday) 13:00 – 17:00 pm

Venue: Cadence Auditorium, Building 10, Cadence, 2665 Seely Avenue, San Jose, CA 95134

Direction: The easiest way is to enter from the Montague Expwy/Trimble Rd traffic light. Building 10 is the tallest 5-story building in the Cadence campus.

Admission: Free admission for all the attendance.

Co-Sponsor: IEEE CPMT

Agenda:

13:00 -13:30 Sign in
13:30 - 14:10 Recent Developments for Enabling 2.5D Solutions, Dr Dongkai Shangguan
14.10 - 14.50 FPGA SSI Technology Design and Verification, Mr Yong Wang
14.50 - 15.30 Thermal Analysis for 2.5D/3D IC Designs, Mrs Yun Dai
15.30 - 15.40 Coffee Break
15.40 - 16.20 The Adoption of 2.5D and 3D Packaging Technology, Dr Larry Zu
16:20 - 17:00 TCAD Solution for Managing Mechanical Stress in 3D IC structures, Dr Xiaopeng Xu

Talk 1

Recent Developments for Enabling 2.5D Solutions

This presentation will review recent developments that can be used to enable 2.5D solutions, including IC/packaging co-design, process technologies, and supply chain. Applications for IoT will also be discussed.

Dr. Dongkai Shangguan

is currently the Founding CEO of the National Center for Advanced Packaging (NCAP China), focusing on developing and commercializing advanced microelectronics packaging technologies for the industry. Concurrently, he also serves as an Executive Advisor at the Institute of Microelectronics, Chinese Academy of Sciences. Through his 20+ years with the industry, Dr. Shangguan worked at the Electronics Operations with Ford Motor Co. / Visteon Corporation in various technical and management function, and at Flextronics as Corporate Vice President of Advanced Technology & Engineering Leadership. Dr. Shangguan received his BS degree in Mechanical Engineering from Tsinghua University, China, Ph.D. degree in Materials from the University of Oxford, U.K., and MBA degree from the San Jose State University.

Talk 2

FPGA SSI Technology Design and Verification

This presentation gives tutorial on FPGA SSI technology design and verification. It shares the economic drivers and technical challenges for SSI technology and introduces Xilinx 3DIC FPGA technology, power and performance optimization. Then it goes through different perspectives of design process, verification, CAD flow and interaction with package design/manufacturing. The combined SSI product clearly shows the benefit of SSI technology to fill the gap between monolithic silicon and 3D IC to continue performance improve curve.

Mr. Yong Wang

is currently a Director of Engineering at Xilinx leading Device Power and Signal Integrity team since 2011. His team owns Xilinx product families' SI/PI methodology development, noise/timing/jitter analysis, interface timing such as DDR4/3, and corresponding verification/characterization. Prior to joining Xilinx, Mr. Yong Wang has been system design and SI/PI lead of several companies such as NVIDIA, MetaRAM, and HP/Intel. He led the world first 16GB and 32GB R-DIMM design, validation and production with patented memory buffer ASIC design when he was system lead with MetaRAM. In NVIDIA/HP/Intel, he provided technical leadership in the areas such as but not limited to, IA-64 system front-side parallel bus channel timing, serial link channel analysis, system level power modeling, on-die power grid noise/timing analysis and timing/noise validation in the lab. Mr. Yong Wang received his M.S. degree in Electrical Engineering from Colorado State University and B.S. degree in Electrical Engineering from Peking University. Mr. Yong Wang has 21 US patents issued and several publications including best paper rewards in IEEE transactions and conferences like MTT, EPEP and ECTC.

Talk 3

Thermal Analysis for 2.5D/3D IC Designs

While 2.5D/3D IC technology provides a great deal of advantages of cost, performance, lower power, etc, thermal issues become evitable important in 2.5D/3D IC designs. This speech introduces Cadence thermal analysis solution for 2.5D/3DIC reference flow.

Yun Dai

is Staff Product Engineer at Cadence System Design Inc. She received a B.S. degree in Electrical Engineering and a M.S. degree in System Engineering from Shanghai Jiao Tong University. She also received a M.S. degree in Computer Engineering from San Jose State University. She has more than 20 year experiences of EDA R&D development, management and customer engagements in the area of power integrity and signal integrity

Talk 4

The Adoption of 2.5D and 3D Packaging Technology

Over the past 68 years the semiconductor packaging industry adopted several technologies: wirebond, flip-chip, MCM, and SiP. In recent years 2.5D and 3D packaging has become a hot topic. IDMs, wafer foundries and assembly houses poured tremendous resources into developing the technology. Today some leading wafer foundries and assembly houses state that their technologies are ready to take customers. Is now the time for our industry to adopt the 2.5D and 3D packaging technology for consumer applications? How about its competing technology? And what are the roadblocks preventing the rapid acceptance of this technology?

Dr. Larry Zu

is the founder and President of Sarcina Technology LLC. Sarcina provides leading U.S. companies with semiconductor package design and power/signal integrity simulation. In addition, Sarcina offers final test hardware design and program development, as well as one-stop turnkey service. The company has strong expertise in package design, from the simplest to the most complex. Since its formation, Sarcina's package tapeouts have all been first-time successes.

Larry Zu is an industrial veteran who has previously worked at AT&T Bell Labs, DEC, Intel, TSMC, and GUC with a proven track record to deliver successful products. At Bell Labs he worked on multichip module (MCM) technology and RF device integration. At DEC he was an Alpha 21264 microprocessor package designer. At Intel he was the lead package design engineer for the Itanium 2 microprocessor. He then managed the microprocessor package design team for the Pentium 4 server, desktop, and laptop. Afterwards, he moved on to manage the optical transponder product engineering group. During his last 2 years at Intel, he focused on RF front-end module design by integrating all active and passive components on Si or laminate substrate. At TSMC he managed the XBOX 360 package design team.

At GUC Larry led a cross functional team in wafer processing, packaging, testing, and Q&R to bring Cisco's networking chips from preproduction to production. He then helped GUC to build from scratch a packaging team with expertise in package design, layout, and chip-package-board co-simulation in power integrity and signal integrity, thermal modeling, and assembly process engineering. In the subsequent 3 years his team taped out 500 packages with a 99.6% first-tape-out success rate.

Larry received his B.S. in physics from Peking University and his Ph.D. in electrical engineering from Rutgers University. He has multiple IEEE journal papers and US patents.

Talk 5

TCAD Solution for Managing Mechanical Stress in 3D IC structures

Mechanical stresses are generated and redistributed in 3D IC structures during fabrication and package assembly process. The stress distribution depends on constituent materials and feature layouts. The residual stresses modulate carrier mobility in the active silicon regions, affect structure integrity, and impose performance and reliability concerns. To manage stress in 3D IC structures, a process orientated technology computer-aided design (TCAD) methodology has been developed to analyze stress accumulation and evolution. A 3D multi-physics simulator is employed to model the entire fabrication and assembly process, which includes silicon and BEOL process, TSV fabrication, micro-bumping, die stacking, flip chip bumping and packaging. Stress simulations are carried out with various constitutive relations to characterize material anisotropy, elasticity, creep, viscosity, plasticity effects. Multilevel sub-modeling technique is utilized to study chip package interaction. Stress induced performance and reliability effects are evaluated for important design parameters. Strategies to minimize performance variation and improve structural reliability are discussed.

Dr. Xiaopeng Xu

is a senior R&D manager at Synopsys, Inc. Before joining Synopsys, he held positions at Avanti, Hyundai Electronics of America, and IBM, and conducted research at University of California and Stanford University. He received his engineering Ph.D. degree from Brown University in 1994.