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Infrastructure for Rapid Assessment of Reliability

Infrastructure and process improvements in the reliability testing of a high density microelectronic packaging technology

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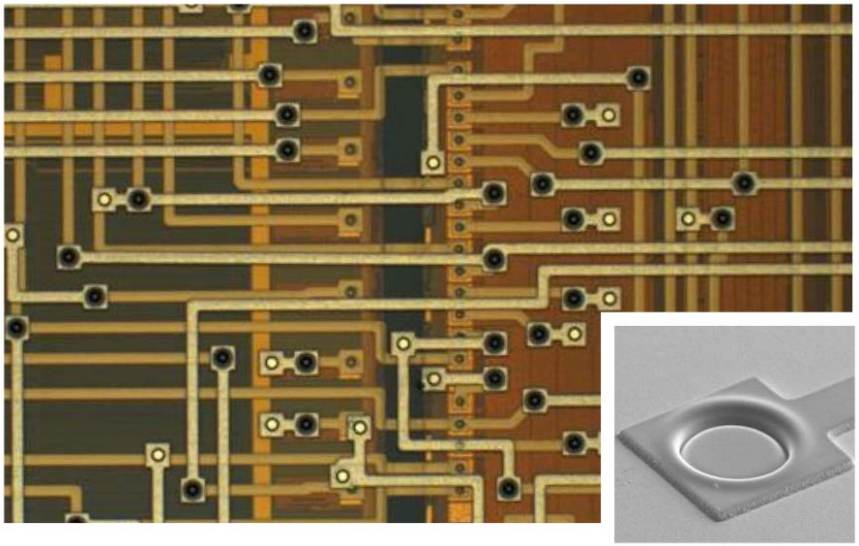
Draper

Outline

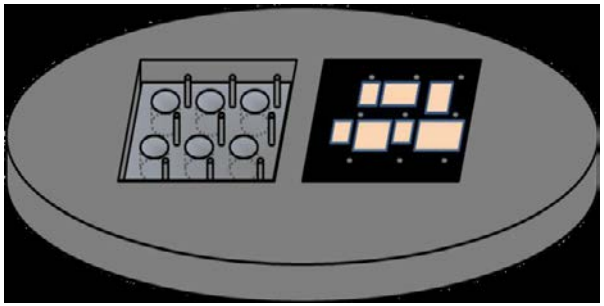
1. What is iUHD?
2. Motivation for early reliability assessment
3. Physical infrastructure
4. Design and Process infrastructure
5. Preliminary outcomes

Integrated Ultra High Density Packaging (iUHD)

- Technology for fabricating multi-chip modules
- Modified Si wafer fabrication techniques
  - Reconstructed wafer process
  - Double sided around polymer core
  - Up to 7 metal layers on a side
- 1 µm thick metal with 12 µm lines and space
  - Ti-Cu-Ti metal layering
- Photoimageable spin-on polymer dielectric
  - 25 µm diameter vias



iUHD module

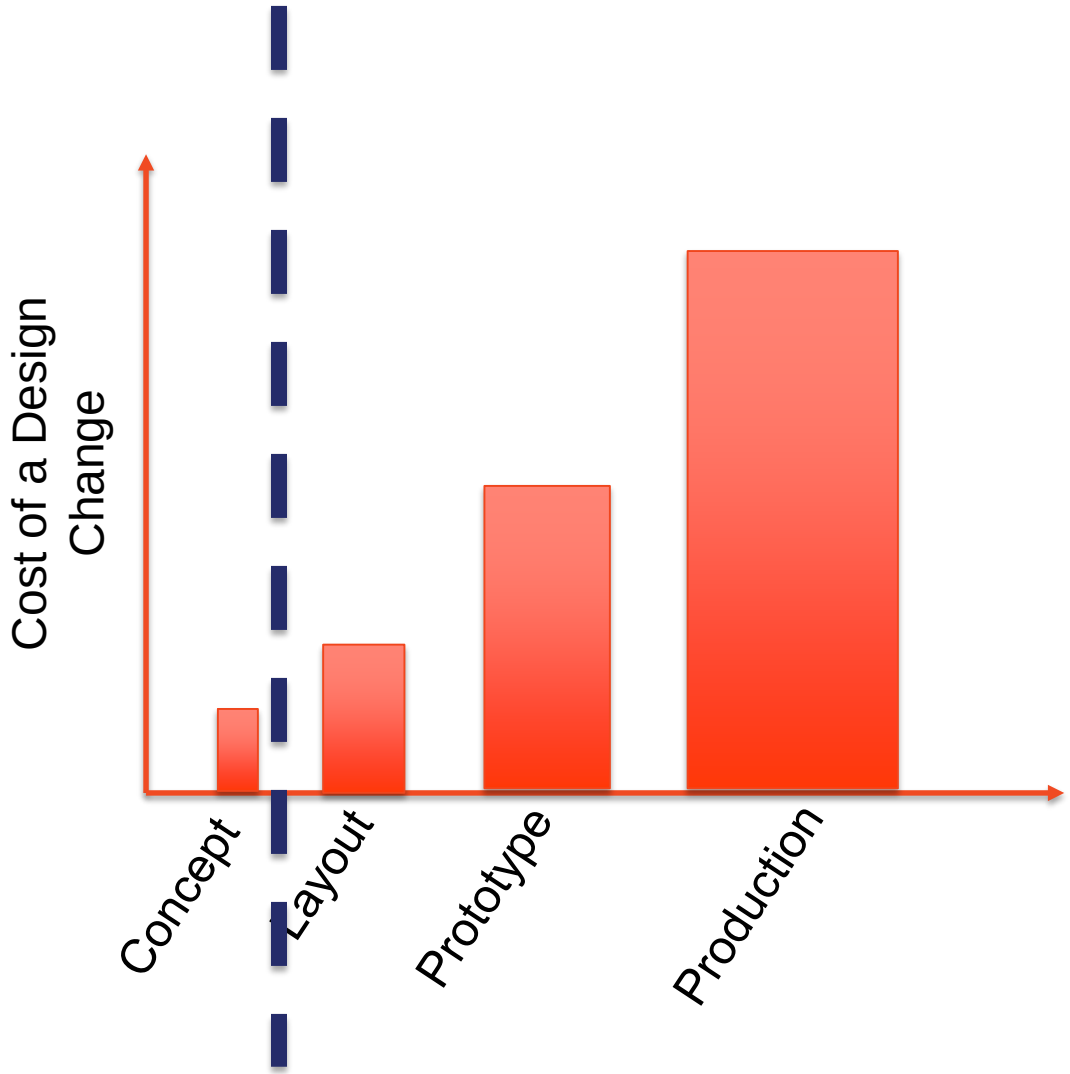


Reconstructed wafer diagram[1]

Motivation

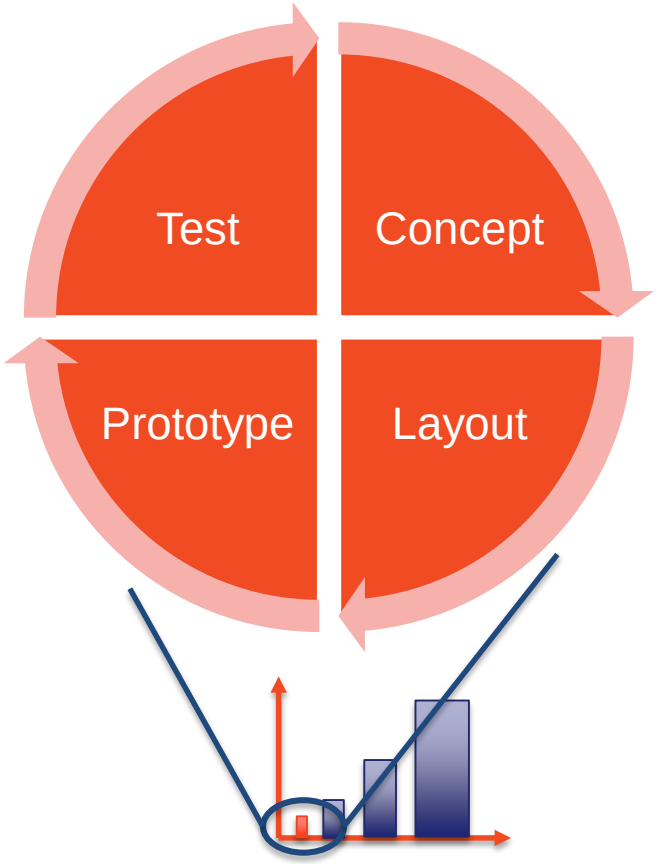
- **Best Practice Reliability Engineering - Quality Ninja**
  - *Early design cycle assessment*
- **Process Development - Characterization of unit processes**
  - *Process change characterization*
  - *Reliability monitoring*
- **Infrastructure - Minimize cost and resource needs**
  - *Common test die design to streamline process*
  - *Common packaging*

Why we need Best Practices



Low Risk, Low Cost

- Goal: Iterate reliability testing as many times as possible before the program schedule pushes to layout and prototype
- A platform for design engineers' *creativity*



Initial Goals

- Data driven test selection with physics of failure intuition
  - *Low hanging fruit*
- Standardized test die design
  - *Simplify data analysis*
  - *Simplify packaging*
  - *Minimize design overhead*
- Standardized Packaging
  - *Consistent method*
- Standardized Test Interface Board
  - *Reusable*
  - *Can accommodate multiple test die designs*

Test Selection Process

FMEA

Four characteristics identified to test:

- Via connection robustness
- Time dependent dielectric breakdown
- In plane leakage
- Trace current carrying capacity

RPN 100 - 199

RPN 1-99

Process step or element	FUNCTION	POTENTIAL FAILURE MODE	POTENTIAL EFFECTS	POTENTIAL CAUSES	DETECTION METHOD	SEV	OCC	DET	RPN
upper layer via	**electrically connect circuit elements**	electrical open	yield loss	via pad contamination	visual inspection, electrical test	4	2	2	**16**
				missing or incomplete via	visual inspection, electrical test	4	2	2	**16**
				missing metal (sputter or plate)	visual inspection, electrical test	4	3	2	**24**
				etch defect	visual inspection, electrical test	4	3	2	**24**
		weak connection opens with time/stress	field failure	via pad contamination	visual inspection, electrical test	9	2	5	**90**
				incomplete via (scumming)	visual inspection, electrical test	9	2	5	**90**
				missing metal (sputter or plate)	visual inspection, electrical test	9	3	5	**135**
				etch defect	visual inspection, electrical test	9	3	5	**135**
				reduced diameter from focus impact of in module bow	visual inspection, electrical test	9	4	5	**180**

Test Conditions

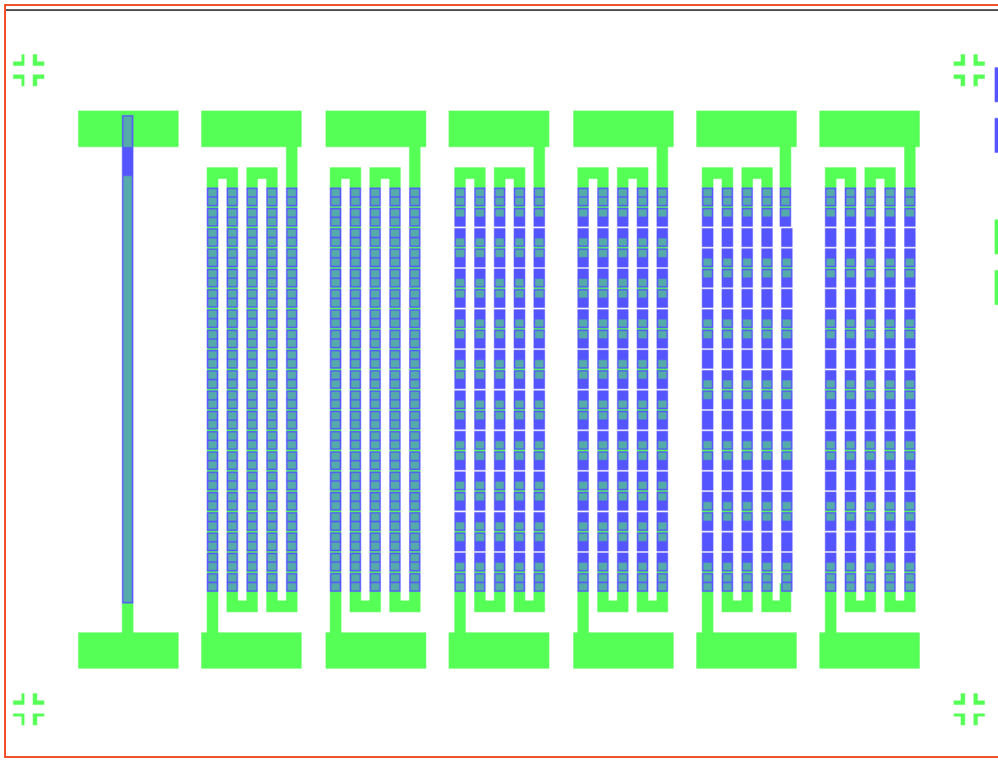
- High Temperature Bias Life
  - *JESD22-A108 (1000 hours at 125C with bias)*
- Temperature Cycling
  - *JESD22-A104 (1000 cycles with Condition B, -55 to 125C, 2 cycles per hour)*
- Temperature-Humidity Bias
  - *JESD22-A101 (1000 hours at 85C, 85% RH with bias)*

Test Die Design Framework

Simple, with minimal variables

Extensible, representing process extremes

- Die size: 6.3 mm x 9.5 mm
  - 48 modules per 100 mm wafer
- 1 control and 6 test structures per die
  - Positive control, 40 vias
  - Up to 6 unique test structures
- Sized to accommodate the identified test features



Test Die Design showing 1 control and 3 pairs of test structures

Packaging Infrastructure

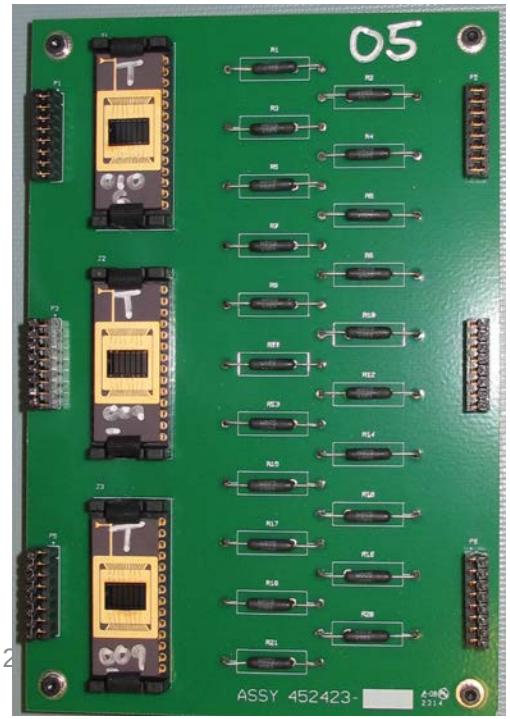
Ceramic package with Au wirebonds to the test die

Socket connector for package to test board (no soldering)

Test board accommodating 3 packaged modules

Current limiting resistors in series

Header pins for resistance measurement



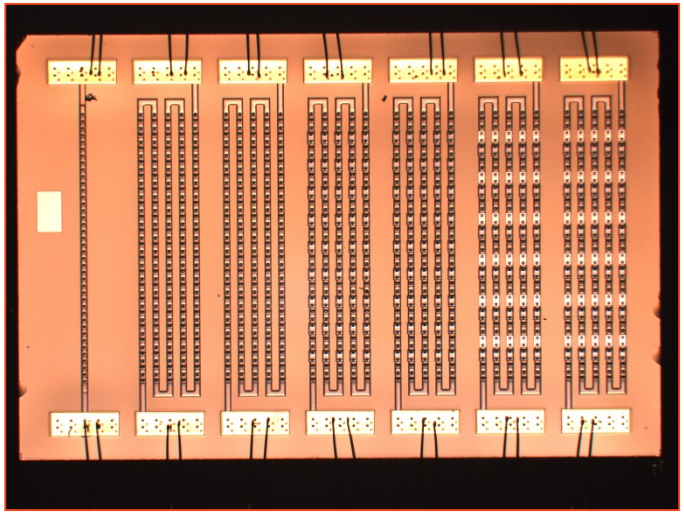
Testing Plan

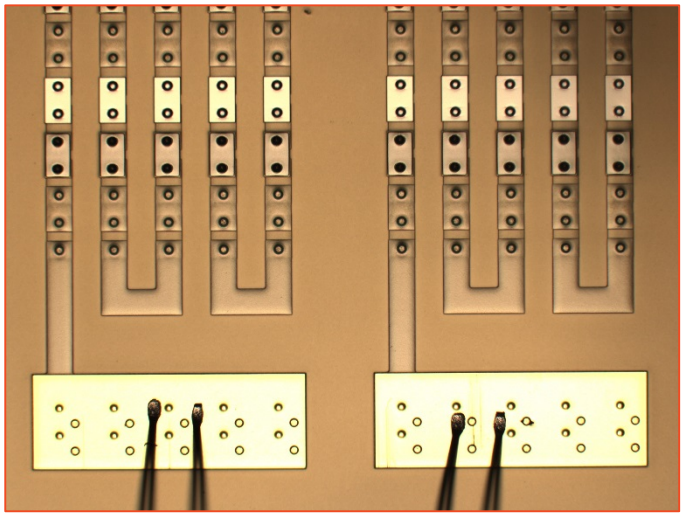
- Test plan for each feature was determined by an analysis of the **failure mechanisms** for each and the **physics of failure**

Feature to Test	Structure Used	Temperature Cycling	High Temperature Bias Life	Temperature Humidity Bias
Via connection robustness	Via chain (THV)	**Yes**	No	No
Time dependent dielectric breakdown	Overlapping Plane Structure (OPS)	**Yes**	**Yes**	**Yes**
In plane leakage	Comb Test Structure (CTS)	No	**Yes**	**Yes**
Trace current carrying capacity	Snake Test Structure (Snake)	No	**Yes**	No

Via Chain Structure

Via Connection Robustness

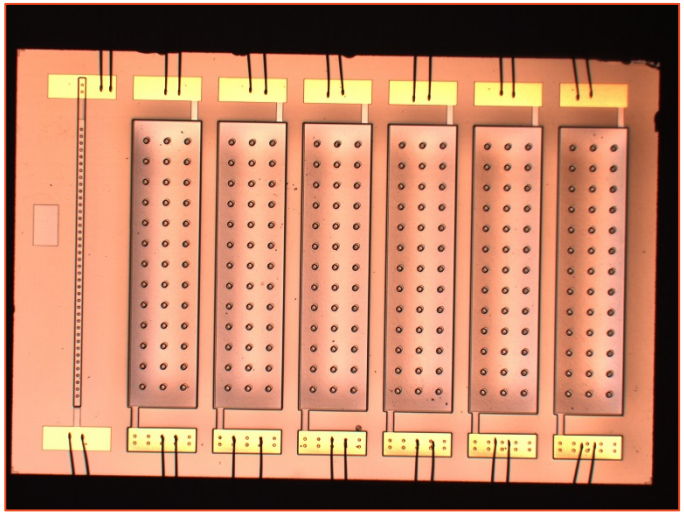


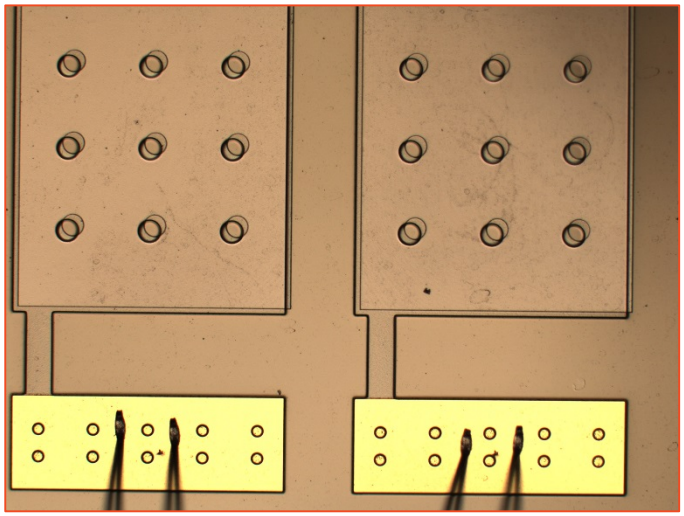


- Via chains through varying dielectric thicknesses
  - 200 vias per structure
  - 3 different structures each test die
    - Single layer via chain (standard process)
    - Double layer via chain
      - Standard and 1.5x Nominal Diameter vias
    - Triple layer via chain
      - Standard and 1.5x Nominal Diameter vias
- Pass/Fail Criteria
  - Less than 10% increase in resistance after environmental test
- Extensibility
  - Wider Via Diameter
  - Increased Via Depth
  - Metal Thickness

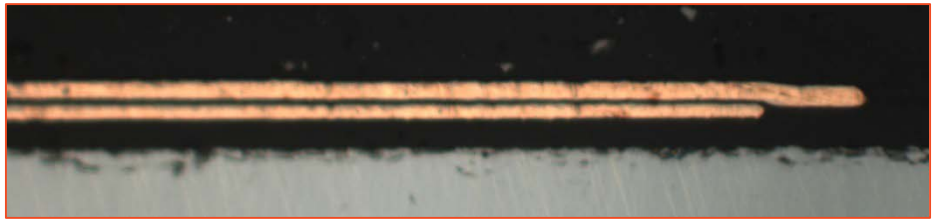
Overlapping Plane Structure

Time Dependent Dielectric Breakdown



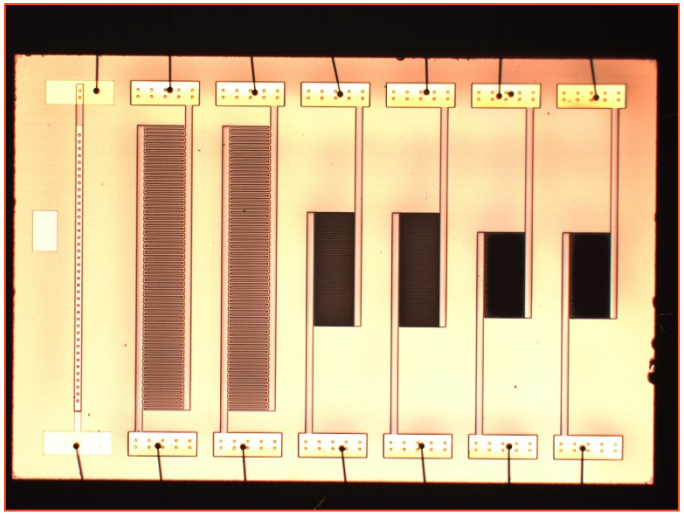


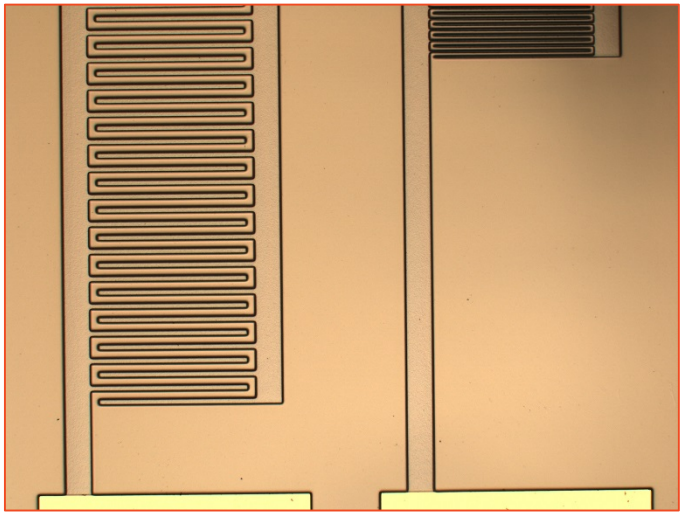
- Stacked metal planes separated by dielectric
  - 6 identical structures on each die
    - 4 mm² area per structure
    - Varied plane separation by increasing metal 1 thickness
    - Stacked perforations and overlap representing product topography
- Pass/Fail Criteria
  - No shorts after environmental test
- Extensibility
  - Dielectric thickness



Comb Test Structure

In Plane Leakage

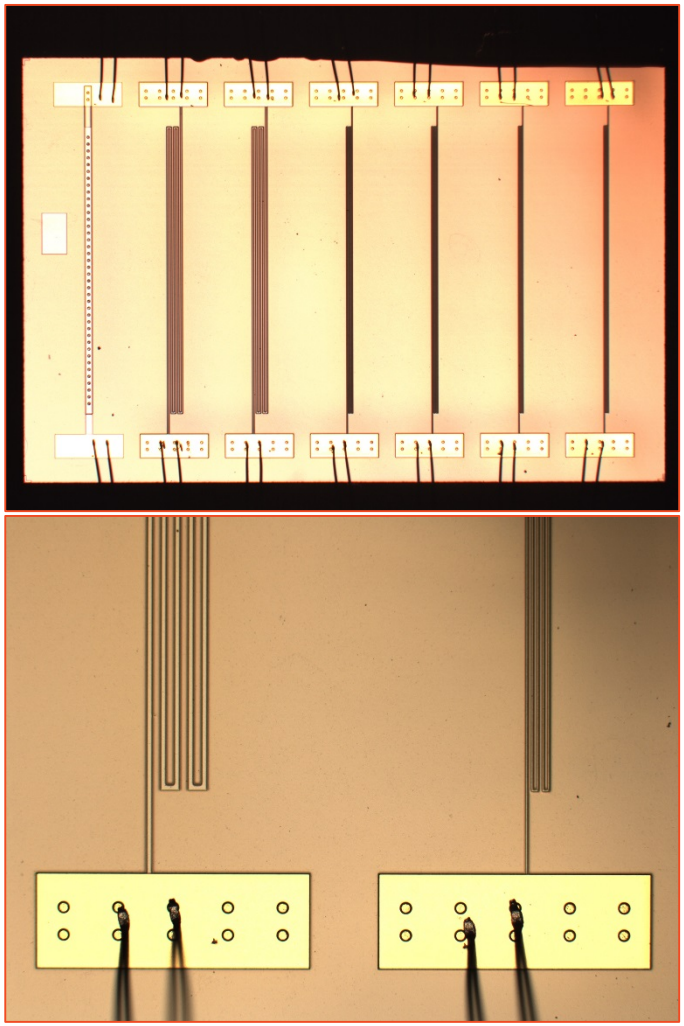




- Interdigitated conductors separated by dielectric (in plane)
  - 84 tooth comb, ~100 mm perimeter
  - 3 test structures per die with varied line width and spacing
    - Nominal
    - 40% nominal
    - 30% nominal
  - 1 µm and 5 µm metal
- Pass/Fail Criteria
  - No shorts after environmental test
- Extensibility
  - Metal thickness (increase in sidewall copper area)
  - Line to line spacing

Snake Test Structure

Trace Current Carrying Capacity



- Single layer trace under dielectric
  - 20 mm long trace
  - 3 test structures per die with varied line width
    - Nominal
    - 40% nominal
    - 30% nominal
  - Current density varied by test structure
- Pass/Fail Criteria
  - Less than 10% increase in resistance after environmental test
- Extensibility
  - Line width
  - Current density

Preliminary results

Feature to Test	Structure Used	Temperature Cycling	High Temperature Bias Life	Temperature Humidity Bias
Via connection robustness	Via chain structure (THV)	**Pass**	NA	NA
Time dependent dielectric breakdown	Overlapping Plane Structure (OPS)	**Pass**	**Pass**	**Pass***
In plane leakage	Comb Test Structure (CTS)	NA	**Pass**	**Pass***
Trace current carrying capacity	Snake Test Structure (Snake)	NA	**Pass**	NA

* Temperature Humidity Bias stopped at 709 hours for equipment maintenance

Rapid Characterization – New Via Type

Laser drilled 2 Layers
Standard diameter

Laser drilled 3 Layers
Standard diameter

Laser drilled 4 layer
Wide diameter

- Demonstrated multi-layer vias could be fabricated with comparable reliability to standard process
  - *Standard vias are photo defined*
  - *Multi-layer vias are laser drilled*
- Characterized on the same test die as standard process vias for a robust comparison

Lessons Learned – In Process Modifications

- The Temperature Humidity Bias Life test exposed two areas for improvement
  - *Implemented use of **soldermask** on all test die after Cu dendrite formation was observed between probe pads*
  - ***Gold** wirebond wires were used on all test die for characterization in humidity after Al wires corroded during test*

Limitations

- The infrastructure is designed to **rapidly characterize unit processes**. It is intended as a pre-screening for features but does not encompass all the **nuances** that may be seen in a design
- Fabrication over smooth silicon is not representative of the **topography present** in an iUHD module (which includes die, encapsulant and through substrate connections)
- Number of **layers** not equivalent to full process capability
- **Internal** features only analyzed

Future Directions

- Use infrastructure to characterize:
  - *Standard **Through Substrate Connections***
  - *Experimental **stacked via** configuration*
- Build test die on **molded wafer** (representative of iUHD core)
  - *To better model the core topography*
- Reliability and Process **monitoring** program
  - *Easily baselined*
  - *Characterization of the process at regular time intervals*
  - *Able to build on product wafers to validate robustness of in-line fabricated material*
  - *Designed into 2 upcoming prorgrams*

Acknowledgments

Maurice Karpman – Reliability engineering guru and mentor

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Carol Toth – For extensive processing support and troubleshooting

References

[1] J. Thompson, G. Tepolt, L. Racz. A. Mueller, T. Langdo, D. Gauthier, B. Smith; “Embedded Package Wafer Bow Elimination Techniques,” *61st Electronic Components and Technology Conference*, (Jun.) 2011.

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Questions

Bios

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Hannah Varner is a Member of Technical Staff at CS Draper Laboratory in the Production Quality and Analysis division. Hannah has worked in reliability engineering and accelerated life testing activities on the micro-electronics and inertial instrument areas of the company. She has an SB in Mechanical Engineering from Brown University where she managed the production of and quality systems for Brown's first satellite (EQUiSat).

Maurice Karpman

Maurice Karpman is a Principal Member of the Technical Staff at CS Draper Laboratory where he has led Accelerated Life Test, FMEA, Reliability Engineering and Risk Management activities. Prior to Draper, he spent 10 years in reliability engineering and failure analysis of MEMS at Analog Devices, including group leader and lab manager positions. He has also worked in electronic package development and optical device engineering at Polaroid, Reflection Technology, Prime Computer and Motorola. He has an SB and MS in Material Science from MIT.