Microwave and Millimeter Wave Power Amplifiers: Technology, Applications, Benchmarks, and Future Trends

Dr. James J. Komiak (Jim)
BAE Systems Electronic Systems
james.j.komiak@baesystems.com
Why Are Power Transistors So Important?

Power amplifiers typically *dominate* transmitter/system characteristics:

- DC power consumption
- Power dissipation (heat) ➔ thermal load
- Reliability ➔ stressful operating conditions
  - High junction/channel temperature
  - High DC operating voltage (relative to other functions)
  - Large AC signals
- Cost
  - Power MMICs typically have largest chip area, highest chip count
  - Power MMICs typically are lowest yield, highest cost ($/chip, $/mm²) of MMIC types due to large size, high periphery
Current Generation Silicon LDMOS

- Based on MOSFET technology
- Low cost, proven performance, reliability
- Low source inductance using p-type sinker
- Field plate for increased gain
- Multi-generation performance improvement continuously has increased frequency of operation
GaAs Pseudomorphic HEMT (PHEMT)

- First demonstrated for microwave power in 1986
- $\text{In}_x \text{Ga}_{1-x} \text{As}$ channel, with $0.15 \leq x \leq 0.30$
  - Enhanced electron transport
  - Increased conduction band discontinuity, allowing higher channel current
  - Quantum well channel provides improved carrier confinement
- Power devices typically use “double heterojunction” layer structure
- Material grown by MBE or MOCVD
- Used for power amplifiers from 0.9 to 80 GHz
- Enhancement mode (E-mode) PHEMT for cell-phone PAs -- single supply voltage
InP HEMT

- Millimeter-wave operation first demonstrated in 1988 (low noise)

- Based on InGaAs/InAlAs material system on InP substrate
  - InGaAs channel with 53% In (lattice-matched), 80% In (pseudomorphic), 100% In (strained pseudomorphic)
  - Enhanced transport, large conduction band discontinuity

- High current (1A/mm), very high transconductance (3000 mS/mm) demonstrated

- Sub-Millimeter Wave frequency response $f_{\text{max}} = 1500$ GHz, $f_t = 610$ GHz

- Low breakdown for single recess (low bandgap of InAlAs gate layer)

- Double-recess devices have been reported

- Metamorphic HEMT (MHEMT) – InP HEMT on GaAs Substrate

- Superior PAE and power gain demonstrated at 20-1000 GHz
GaN HEMT

- Grown on SiC substrates
- Heterojunction with undoped channel
- Electron mobility $\mu = 1500 \text{ cm}^2/\text{V-sec}$
- High surface defect density ($10^7$-$10^8$/cm$^2$)
- First GaN HEMT MMIC reported in 2000
- Millimeter Wave frequency response $f_{\text{max}}$ of 230 GHz, $f_t$ of 97 GHz
- Very high power density demonstrated $>10\text{W/mm}$
- Thermally limited device
Best Reported Microwave Transistor Efficiencies

High Gain Enables High Efficiency Modes of Operation: Class AB2, Class B, Class C, Class F
Integration to Higher Power Levels

- Small periphery (gate/emitter)
- Short gate/emitter fingers
- Low parasitics

- “Building block” for higher power
- Longer fingers
- Characterized for power amplifier design

- Power amplifier or T/R module
- MIC power combining (typ. 2 to 8-way)
- Each MMIC feeds separate radiating element (typ. 100s-1000s of elements)

- Full MMIC: all matching on-chip

Intrinsic Device (single finger)

Power Transistor “Cell”

Hybrid Power Amplifier

Power MMIC

Module

- Discrete device: all matching off-chip
- Waveguide/Radial Combiners
  - W/G: 2 to 32-way
  - Radial: to 128-way
- Constrained Combining (Plumbing)
- Spatial Combining (Phased Array/Quasioptics)

BAE SYSTEMS
Pre-history of Circuit Design

- **Characterization:**
  Simple analytical models derived from DC I-V measurements

- **Simulation:**
  Hand calculation of model parameters

- **Models:**
  Ebers-Moll....
1970s Circuit Design

- **Characterization:**
  - I-V & C-V measurement;
  - S-parameters - HP8410

- **Simulation:**
  - …increasing sophistication!

- **Models:**
  - … “hybrid-π”
1980s Circuit Design

- Characterization:
  S-parameters over bias
  - HP8510

- Simulation Tools:
  Touchstone, Compact

- Models appear in the simulators:

Small-signal bias-dependent equivalent-circuit FET model
1990s Circuit Design

- **Characterization:**
  Pulsed I-V and S-parameters

- **Simulation Tools:**
  *Harmonic Balance* enables large-signal simulation in HP ‘MDS’, EEsof ‘Libra’

- **Models:**
  Large-signal models: ‘Root’ FET model
2000s to now Circuit Design

- Characterization: X-Parameters – PNAX
- Simulation Tools: HB, Circuit Envelope
  Agilent ‘ADS’
  AWR ‘Microwave Office’

Vector Signal Analysis
1990 State of the Art Amplifier

- Two stage MMIC Amplifier, 3 to 6 GHz, off-chip matching network
  - Output Power 11 W ± 1 dB
  - Large signal gain of 10 to 13 dB
  - PAE in the range of ~10 to 17%
  - 43% to 57% dc / visual yield
  - Extensive discussion on thermal performance

- Output stage design methodology
  - Comprehensive device characterization including both measurements and linear/nonlinear modeling
    - Measured small-signal S parameters, equivalent circuit models fitted to the data
    - $I/V$ measurements augmented with optimum load/contour data obtained via load pull, are used to derive a consistent linear/nonlinear model
  - Network synthesis techniques consisting of transforming the 50Ω load to the required optimum large-signal load impedance
    - Cripps technique, a value of $R_{opt}$ derived from $I_{dss}$ and the $V_{ds}$, and the small-signal model parameters $C_{ds}$ and $L_{dr}$ determines an approximation to the optimum class A load.
    - An enhanced version of the Cripps technique takes into account the effect of the full-channel current $I_{max}$ and the nonunilateral nature of the device by large-signal conductance substitution of the load line into the complete small-signal model
    - The use of the load-pull measurements with variable tuners, automated to search for optimum conditions

1995 State of the Art Amplifier

- A fully monolithic HBT power amplifier
  - 2400 µm consisting of 8 - 300 µm unit cells in a cascode configuration
  - Power-added efficiencies of 56% max / 38% min, 44.4% average across 7 to 11 GHz band
  - Output power levels of up to 7.3 Watts with a gain of 11 to 14.1 dB
    - Under long pulse (500 usec) and high duty cycle (25%) conditions.

2011 State of the Art Amplifier

- Decade Bandwidth 2 to 20 GHz GaN HEMT Power Amplifier MMICs in DFP and No FP Technology
  - With Dual Field Plate [DFP] Technology
    - $P_{3db}$ of 26.3 Watts max, 15.4 Watts average, 7.1 Watts min.
    - PAE of 38.3 % max, 19.8 % average, 5.9 % min.
    - Power gain of 11.2 dB max, 8.6 dB average, 5.0 dB
  - No Field Plate [FP] Technology
    - $P_{3db}$ of 21.6 Watts max, 16.0 Watts average, 9.9 Watts min.
    - PAE of 35.7 % max, 25.9 % average, 15.3 % min.
    - Power Gain of 11.1 dB max, 9.7 dB average, 8.0 dB min.

Komiak, J.J.; Kanin Chu; Chao, P.C.; , "Decade bandwidth 2 to 20 GHz GaN HEMT power amplifier MMICs in DFP and No FP technology,” Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International, vol., no., pp.1-4, 5-10 June 2011
Power Amplifier Advance Architectures

- **Stage Bypassing and Gate Switching**
- **Kahn Envelope Elimination and Restoration Technique**
  - Combines a highly efficient, but nonlinear RF Power Amplifier with a highly efficient envelope amplifier to implement a high-efficiency linear RF Amplifier
- **Envelope Tracking**
  - The supply voltage is varied dynamically to conserve power, but with sufficient excess (“headroom”) to allow the RF PA to operate near saturation at high efficiency.
- **Outphasing**
  - Produces an amplitude-modulated signals that combine the outputs of two amplifier driven with signals of different time-varying phases. The resulting output is the instantaneous vector sum of the two amplifier outputs to follow the desired signal amplitude. In a modern implementation, a DSP and synthesizer produce the inverse-sine modulations of the driving signals.
- **Doherty Technique**
  - This architecture combines two amplifiers of equal capacity through quarter-wavelength lines or networks. The “carrier” (main) amplifier is biased in class B, while the “peaking” (auxiliary) amplifier is biased in class C. Only the carrier PA is active when the lower signal amplitudes. Both amplifiers contribute output power when the input signal amplitude is approaching levels to saturate the main amplifier.

150 Watt 110-450 MHz Si LDMOS Power Amplifier

Push-Pull with Ferrite Loaded Coax Baluns

Power Gain at 150 Watts ~ 12.5 dB
S-Band GaN HEMT High Power Amplifier

**GaN Chip : 4 x 36mm**

**Package size : 36.4 mm x 17.4 mm**

**Evaluation Board**

- **Frequency** = 2.9 GHz
- **Pout ~ 800 Watts**
- **Bandwidth > 2.9 to 3.3 GHz**
- **Vds = 65 V**
- **Idsq = 2 A**
- **PW = 200 usec**
- **Duty Cycle = 10 %**

**Graph:**
- **Output Power [dBm]**
- **Gain [dB]**
- **Input Power [dBm]**
- **59.3 dBm**
- **57.4%**
- **14.5 dB**
Ka-Band 0.2 μm NFP GaN HEMT MMIC HPA

- **Process:** 0.2 um NFP GaN HEMT
- **Frequency Range:** 34 to 36 GHz
  - 14.8 - 15.8 Watts Pout
  - 21% PAE
- **Design Details**
  - Quadrature Balanced
  - Fast gate switching FRAP bias network
  - Vds = 20 to 34 Volts
  - 5.4 mm periphery, Idsq = 200 mA/mm
- **Chip Size:** 4.568 mm x 4.025 mm x 55 um

Highest MMIC CW Power Reported at Ka-Band
W-Band 0.15 μm GaN HEMT MMIC HPA

- Process: 0.15 μm GaN HEMT
- Frequency Range: 84 to 95 GHz
  - 0.5 to 0.8 W @ 10-15 % PAE (2010)
  - 1.5 to 1.8 W @ 17.8 % PAE (2012 8-way)

0.15 mm – 0.3 mm – 0.6 mm
1 THz InP HEMT MMIC

- **Process:** 25 nm InP HEMT
- **Application:** THz
- **Frequency Range:** 0.95 to 1.05 THz
  - Pout 0.25 mW (estimated)
- **Chip Size:**
  - 550 um x 350 um x 18 um (WR-1.0 version)

- 8 um transistor cell
- 2 fingers x 4 um
- CPW MMIC
Coaxial Waveguide Spatial Power Combiner

Input Transition  Input Antenna  MMICs  Output Antenna  Output Transition

Waveguide Tray

Packaged MMIC

Microstrip to Antipodal Finline Antenna Transition

(a)  (b)  (c)

Section 1  Section 2  Section 3
**W-Band SSPA**

Two-chip module binary WG septum combiner, transitions, bias networks. Module dimensions are 2.05 x 0.57 x 0.19 inches.

SSPA with the air-cooling fins attached. Mass of this unit is 0.47 kg and its dimensions are 2.4 inches dia x 2.5 inches.

Phased Array

An array of antennas in which the relative phases of the respective signals feeding the antennas are varied in such a way that the effective radiation pattern of the array is reinforced in a desired direction and suppressed in undesired directions.

$$\text{EIRP} = G_e \times P_e \times N^2$$
High Power Solid State Transmit Technologies
(not including Phased Arrays)

GaN potential -- 10X increase in MMIC and SSPA power, 1-100 GHz
Future Trends

• Circuit Technique Development & Implementation
  • Multi-tone with controlled distortion
  • STAR: Simultaneous Transmit and Receive

• Sub-Millimeter Wave Applications

• Thermal
  • Near Junction Thermal Transport (NJTT) – GaN on Diamond
  • Thermal Ground Plane (TGP) -- alloy heat spreader
  • IntraChip/InterChip Enhanced Cooling (ICECOOL) -- convective or evaporative microfluidic cooling built directly into devices or packaging
  • Microtechnologies for Air Cooled Exchangers (MACE) – enhanced heatsinks
  • Active Cooling Module (ACM) – miniature refrigeration systems based on thermoelectric or vapor-compression technologies

• Semiconductor Devices
  • Evolutionary
  • Diamond
  • Graphene, Carbon Nanotube
  • Boron Nitride
  • ?? ??