Class 0 – Who’s at Risk & How to Avoid Quality and Reliability Failures

Professional Services Only
No Product Sales!

Client Locations

Ted Dangelmayer
www.dangelmayer.com
Agenda

- Preliminaries
- Class 0 Definition
- Brief Review: CDM & CBE
- Who’s At Risk
  - Class 0 Technologies
- Class 0 Failure Mitigation
ESD Acronyms

- **EPM:**
  - ESD Program Management: A Total EPM Quality System

- **Best Practices Benchmarking™**
  - Relative Compliance to Best Practices
  - Quantifies Yield Improvement Opportunity

- **EOS** – Electrical Overstress
  - IC Damage due to Electrical Over Voltage or Current

- **HBM** – Human Body Model
- **CDM** – Charged Device Model
- **CBE** – Charged Board Event
- **CDE** – Cable Discharge Event
DA ESD Class 0 Definition

• Class 0
  • Withstand Voltages Less than 250 volts HBM or CDM

• Class 00
  • Withstand Voltages Less than 125 volts HBM or CDM

• Class 000
  • Withstand Voltages Less than 50 volts HBM or CDM

Note: Class 0 Devices Prone To Higher Levels of Test Failures, Test Escapes and Latent Failures
### ESDA Technology Roadmap

**Device Thresholds Are Declining**

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<tbody>
<tr>
<td>HBM</td>
<td>3800V</td>
<td>3000V</td>
<td>2200V</td>
<td>1500V</td>
<td>1000V</td>
<td>750V</td>
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<tr>
<td>CDM</td>
<td>800V</td>
<td>700V</td>
<td>675V</td>
<td>625V</td>
<td>325V</td>
<td>240V</td>
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### IC Design Target Levels

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<th>Model</th>
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<tbody>
<tr>
<td>HBM</td>
<td>2000V</td>
<td>500V</td>
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<tr>
<td>CDM</td>
<td>500V</td>
<td>250V</td>
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ESD Damage
A Quality & Reliability Issue

- **Catastrophic**
  - Device failure that is both sudden and complete. It involves complete loss of the required function

- **Cumulative**
  - Device failure resulting from multiple sub-threshold exposures to ESD

- **Latent**
  - Device failure over time due to prior ESD damage
Brief Review: CDM – CBE
Charged Device Model

“99.9% of ESD Failures are CDM/CBE/CDE!”

Andrew Olney, Analog Devices, Quality Director & Industry Council, TI, Intel, etc.
S20.20 - Class 0 and CDM/CBE Limitations
Yield Improvements by Adding CDM & CBE Best Practices

Note: Courtesy Herald Datanetics Ltd. - 1st Class 0 Certified Manufacturing Operation
http://www.dangelmayer.com/class-0-certification.php  Each data point is confirmed ESD damage during production (typically 65 volt CDM/HBM ESD sensitivity) and different colors represent different products.
CBE (Charged Board Event) Test Set-Up

Sensitive Device Pin

Thin Dielectric Film

Field Plate

Olney et al (Analog Devices)
Charged Board Event ESD Damage
Most FA Experts Misdiagnose as EOS!!!!

Up to 50% of EOS Failures are CBE ESD! (2008)

Peak Currents of 25 amps Have Been Measured!

Courtesy: Andrew Olney, Quality Director, Analog Devices
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How to Classify Circuit Boards

• Based on Most Sensitive Component
  • Class I, 0, 00, 000
  • Must Have Both HBM & CDM Thresholds
  • Estimates Are Not Sufficient
    • W/O Data You are At Risk

• Consider Class 0 For Boards Due to CBE
  • Based on Criticality of Application
  • 25 Amp Discharge Currents Possible
Are You On A Collision Course Too?

“The Perfect Storm”
Entire East Coast of USA
October 1991

- Without Typical “Hurricane Warnings”!
  - Fishermen At Sea Caught Off-guard
  - 2000 Miles of Hurricane Like Conditions
- **ESD Analogy:**
  - CDM Generally Not Understood
  - Class 0 Trend Approaching Now
- **A Very ESD Real Threat!**
  - More Dangerous than Individually
Class 0 - Who’s At Risk
None of the Sites Assessed Since 2001 had adequate CDM/CBE Controls in place initially!
Class 0 - CDM Threshold Dependencies

Larger Device Package Size

Higher Operating Speeds
Class 0 Technologies

- ICs
  - Nanoscale CMOS
  - RF
  - GaAs
- Optoelectronics
  - Lasers
  - LEDs
  - Detectors (PIN, APD)
- MEMS
- MR Heads
Class 0: Who’s At Risk

- Semiconductor Backend
- Automation
- HBM Programs
  - S20.20 Programs
  - Manufacturing w/o
    - HBM & CDM Thresholds
    - CDM Best Practices
    - CBE Best Practices
- Circuit Board Manufacturing & Integration
- Contract Manufacturing
- Defense Manufacturing
- Aerospace Manufacturing
  - NASA
- Consumer Electronics Manufacturing
- Medical Manufacturing
- Automotive Manufacturing
- Wafer Fabrication & Wafer Saw
- New Construction & Outfitting New Lines
Circuit Board Manufacturing & Integration

• Myth:
  Circuit Boards are Less Sensitive to ESD than Devices
  • Widely Assumed True - False Sense of Security
  • Boards Are More Sensitive than Components
    • Up To 25 Amp Discharge Currents
  • Nokia Asserts All ESD Failures Happen at Board Level
  • Rapidly Escalating Probability of at least One Class 0 Component per Board
  • 50% of EOS Board Failures are ESD (CBE/CDE)
Variation in CBE Waveforms

A - High L, C
B - Lower L, C; higher R
C - Faster discharge (small C)
D - Slower discharge (large C)
E - Two RLC sources
F - High L, R

Data Courtesy Nokia
At Risk - Contract Manufacturing (CM)

- CM Programs are HBM – S20.20
- On a Collision Course
  - Customer Generally Do Not Specify Class 0 Requirements
    - Customers Leave CDM & Class 0 Mitigation to CMs
    - CMs Require Customers Requirements to Take Action
  - Therefore – a Collision Course
At Risk - Defense & Aerospace Manufacturing

- CDM & CBE Mitigation Not Required
  - Generally Not Well Understood at Factories
- Mil Standards 30 Years Outdated
  - S20.20 an HBM Standard
- Resistant To Change
At Risk - Consumer Electronics Manufacturing

- Often Performance & Cost Driven
  - High Speed
  - Technology Node Feature Sizes
  - Circuit Functionality
  - I/O Density
- Combination Prone to Class 0 Thresholds
At Risk - Medical Manufacturing

- FDA Recognizes S20.20
  - CDM & CBE Not Recognized
- Failures Life Threatening
At Risk - Automotive Manufacturing

• Expanding Application of Electronics
  • Less Experience with Electronics Manufacturing
    • Transitions from Mechanical to Electronic Difficult
• ESD Controls New to Automotive Repair Operations
  • Often Insufficient Controls
At Risk - New Construction & Outfitting New Lines

- Class 0 Often Overlooked for New Construction
  - ESD Engineers Often not Involved Early
  - Architects & Facility Engineers Make Decisions without ESD Input
    - Can Result in Significant Cost Penalties to Correct Errors
    - e.g. - Segregation of Class 0 Lines May be Necessary
- Class 0 Material Properties Generally Not Considered
  - Flooring
    - High vs. Low Charging Selection
  - Conveyors, Material Transports, Automation & Workstations etc.
- Can Result in Replacement of Costly Items for Class 0 Applications
At Risk - Wafer Fabrication & Wafer Saw Operations
Are ESD failures happening at wafer level?

Arc model, I(t) - Includes inductance

Field plate at V

V(t)

Small features

neglected

Small cap

large cap

Large bus

Bulk resistance

surface resistance

neglected

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Typical Wafer Potential Difference Distributions

**Difference in potential from zap point**

5000 volt zap

<table>
<thead>
<tr>
<th>V (V)</th>
<th>Position (mm)</th>
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<tbody>
<tr>
<td>-250</td>
<td>0</td>
</tr>
<tr>
<td>-200</td>
<td>0.001</td>
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<tr>
<td>-150</td>
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<tr>
<td>-50</td>
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<tr>
<td>0</td>
<td>0.005</td>
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**Potential differences between neighboring points**

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<th>V (V)</th>
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<tr>
<td>-80</td>
<td>0</td>
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<tr>
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<tr>
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<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
</tr>
<tr>
<td>80</td>
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</table>
Class 000 – Wafer Saw Example
Unexpected Results!

• CDM Threshold – 35 Volts
• 92.2% Defective at Wafer Saw
• Failure Analysis
  • CDM Damage
Class 0 Failure Mitigation
Class 0 Mitigation Considerations

- Industry Standards Do Not Include CDM For Class 0!
  - Unlikely They Will in Foreseeable Future
    - Not Conducive to Standardization
    - Customization Essential
  - CDM Mitigation Techniques Not Well Known
  - Not Planned for 2014 Issue of S20.20
- 99.9% of ESD Component Failures are CDM/CBE/CDE
  - CDM & CBE Techniques Virtually the Same
  - Therefore:
    - Class 0 Controls ~ CDM Controls
    - CDM Mitigation Techniques Must Be Fully Understood
- Proven CDM Best Practices Requirements
  - In Private Sector – Limited Access by Public
  - Class 0, 00, 000 Requirements
    - Escalate at 250 V, 125 V, 50 V
**Best Industry**

**Manufacturing Standard**

ANSI/ESDA S20.20

Scope: HBM >100V

Industry Standards

Lag Technology

10 to 15 years

Thus:

*S20.20 Customization is Essential for:*  
Class 0, CBE, CDE & CDM
CDM Mitigation

Two Strategies – Which One is S20.20?

Lower device voltage or higher surface resistance in the discharge path can reduce discharge current.
S20.20 - Class 0 and CDM/CBE Limitations
Yield Improvements by Adding CDM & CBE Best Practices

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Questions?

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