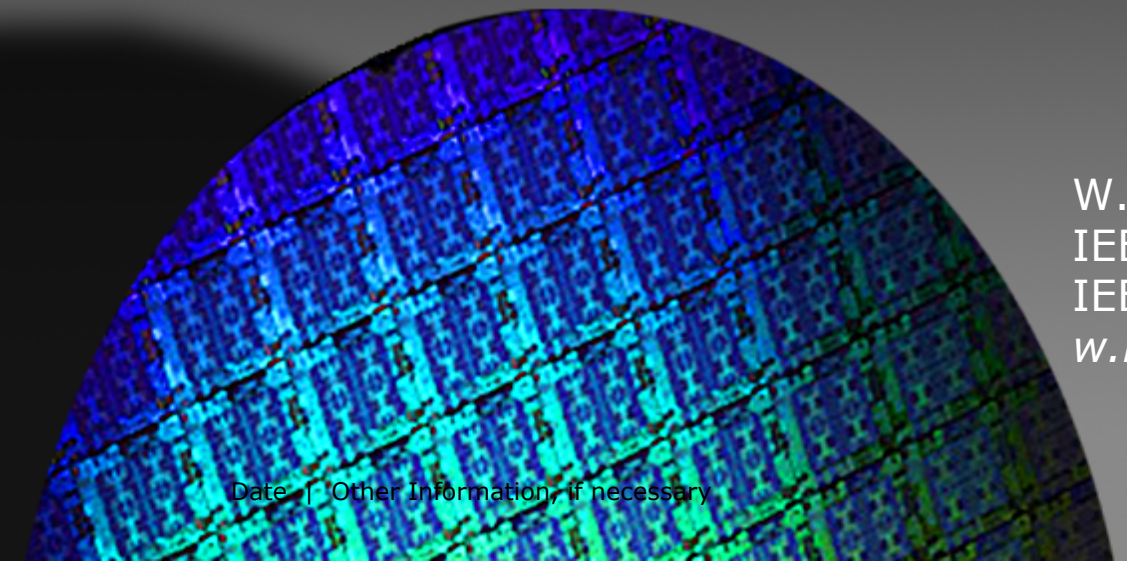
Intellectual Property Key Ingredients…..



W. Tonti
IEEE Sr. Director
IEEE Future Directions
w.r.tonti@ieee.org

A TUTORIAL WALK THROUGH A PATENT

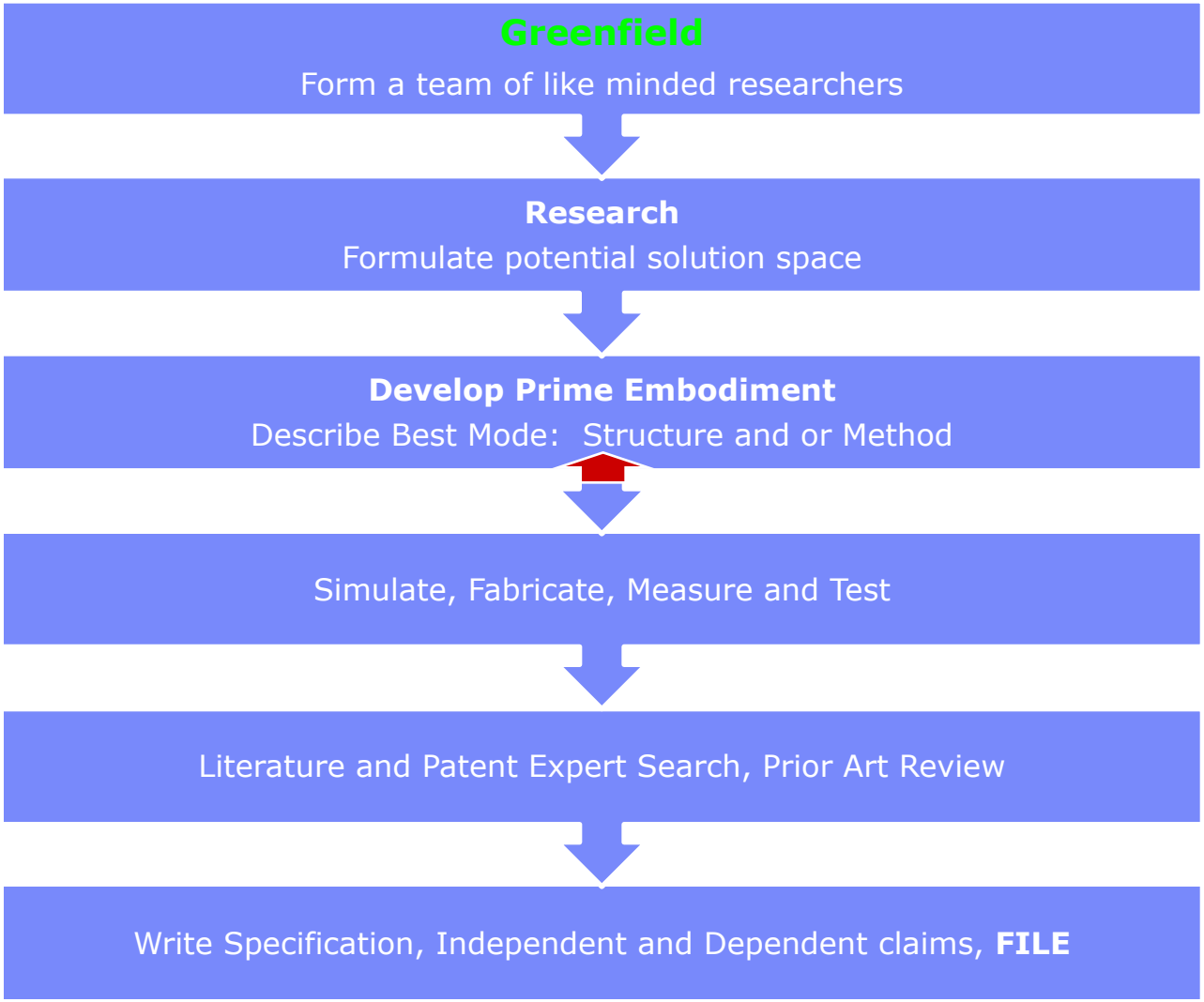
US 5,798,553
Issue Date: 8/25/1998
TRENCH ISOLATED FET DEVICES, AND METHOD FOR THEIR MANUFACTURE

A TUTORIAL WALK THROUGH A PATENT

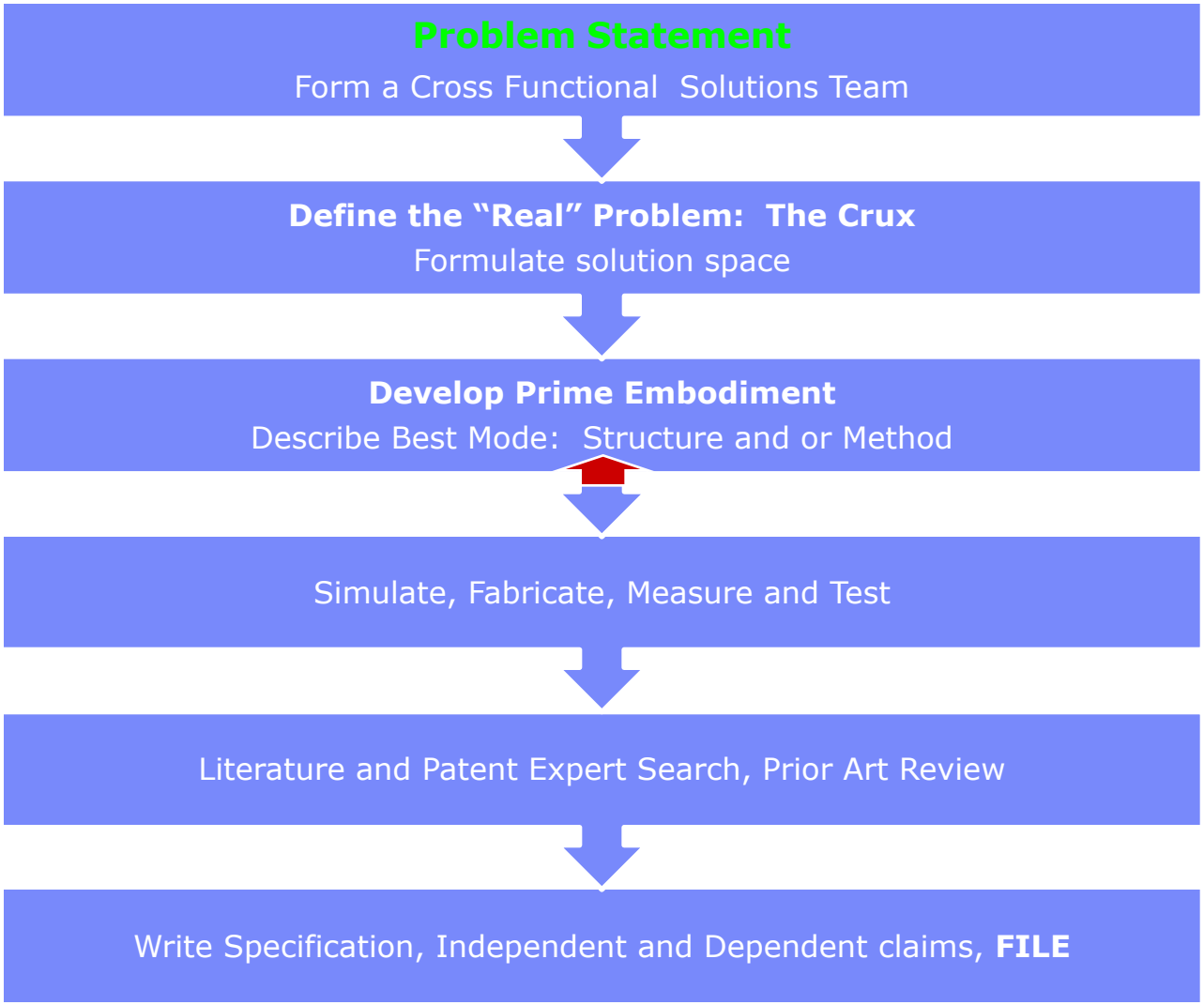
OUTLINE OF PRESENTATION:

- POTENTIAL PATENTS
- REQUIREMENTS FOR OBTAINING A PATENT
- EXEMPLARY PATENT – US 5,798,553
  - OVERVIEW OF PROBLEM TO BE SOLVED
  - THE SOLUTION
  - COMMENTS ON PATENT
- MY PERSPECTIVE OF FACTORS CONDUCIVE TO SUCCESSFUL INVENTING

The Process of Inventing: New Space, Base Tech – Think Tank



The Process of Inventing: Solving a Problem, Cross Functional Team



A SOLUTION TO A PROBLEM IS A POTENTIAL PATENT

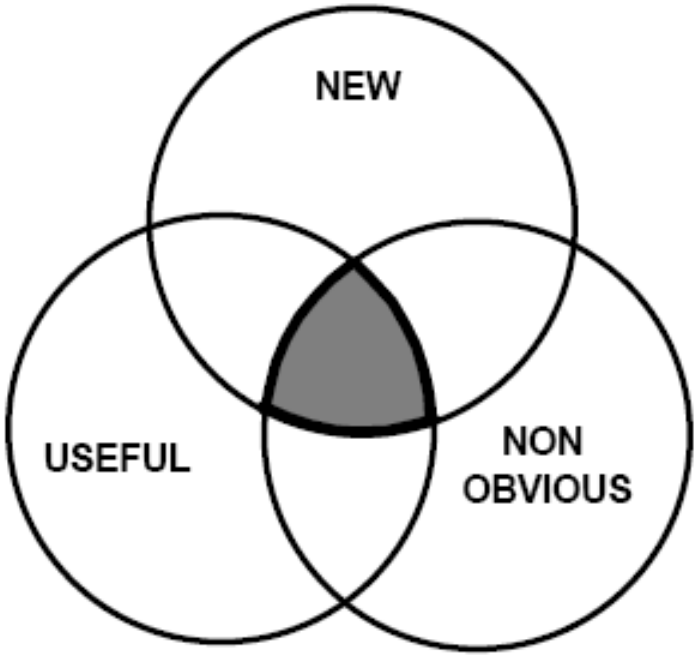
- PROGRESS IN TECHNOLOGY DEVELOPMENT IS IMPEDED BY PROBLEMS ENCOUNTERED ALONG THE WAY

  - UNANTICIPATED APRIORI

  - SOLUTIONS ARE REQUIRED TO ACHIEVE THE GOALS OF A PROJECT

→ FERTILE GROUND FOR INVENTING

REQUIREMENTS FOR OBTAINING A PATENT



TO OBTAIN A PATENT, AN INVENTION MUST BE:

- NEW
- USEFUL
- NON OBVIOUS

The Patent Process

- Solution of an existing problem
- Identifying elements for a future roadmap
- Leverage your strengths
- Form a team
- Everyone is a contributor, no idea is bad
- Write it down……
  - For me ideas come at night. Have a pad nearby.
  - A picture really is worth 1000 words

Where do you search for Prior Art ?

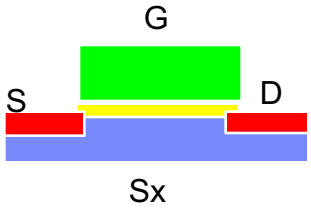
- Two main sources of IP
  - IEEE Xplore
  - US patent database
- Why bother searching?
  - It is required.
  - Your claims will be modified based on what you uncover.
  - More often than not prior art will sharpen your own submission.

Transistor

Four Terminal Switch, A Field Effect Device
Minority Carrier Current flows from (Source to Drain)
Requires a potential to invert the surface (Gate)
Common Substrate Connection

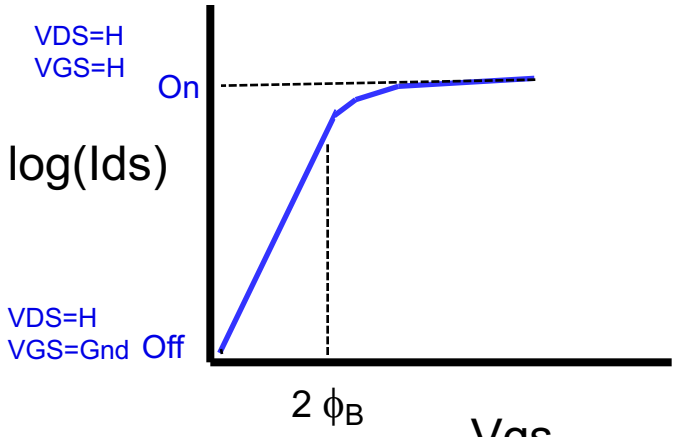
Fundamental design criterion: Built in potential $\phi_B=[kT/q]\ Ln(N/N_s)$

A Transistor switches from the off to on state at ~2 ϕ_B



Bias Configuration
S= Gnd
Sx= Gnd
D=High(+)
G= Swept, Gnd to D

Layout

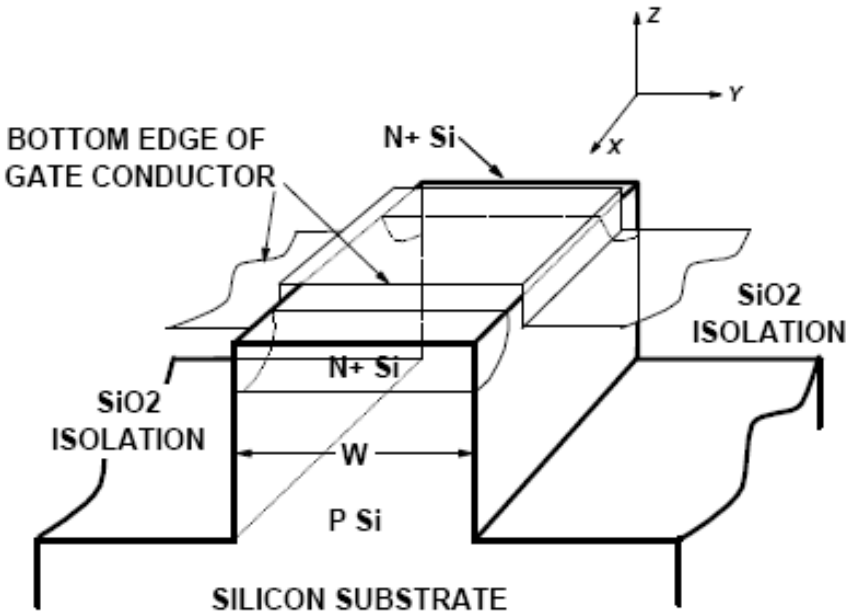


OVERVIEW OF PROBLEM TO BE SOLVED

US 5,798,553

PROBLEM STATEMENT:

- HOW CAN THE CHANNEL CURRENT CONTRIBUTED BY THE SILICON CORNER OF MOSFETs BOUNDED BY SHALLOW TRENCH ISOLATION (STI) BE MINIMIZED?



CHANNEL CURRENT IS IN THE "*x*" DIRECTION

OVERVIEW OF PROBLEM TO BE SOLVED

US 5,798,553

CROSS-SECTION NORMAL TO CHANNEL CURRENT:

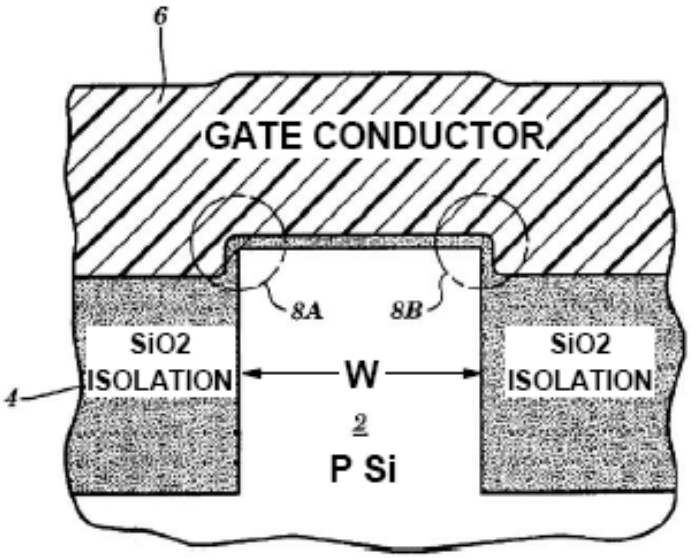


FIG. 1

- FOR EQUAL DOPING CONCENTRATION, THE THRESHOLD VOLTAGE (Vt) AT THE SILICON CORNERS (8A, 8B) IS LOWER THAN AT THE MIDDLE PLANAR REGION

  - WHY?

INSIGHT·

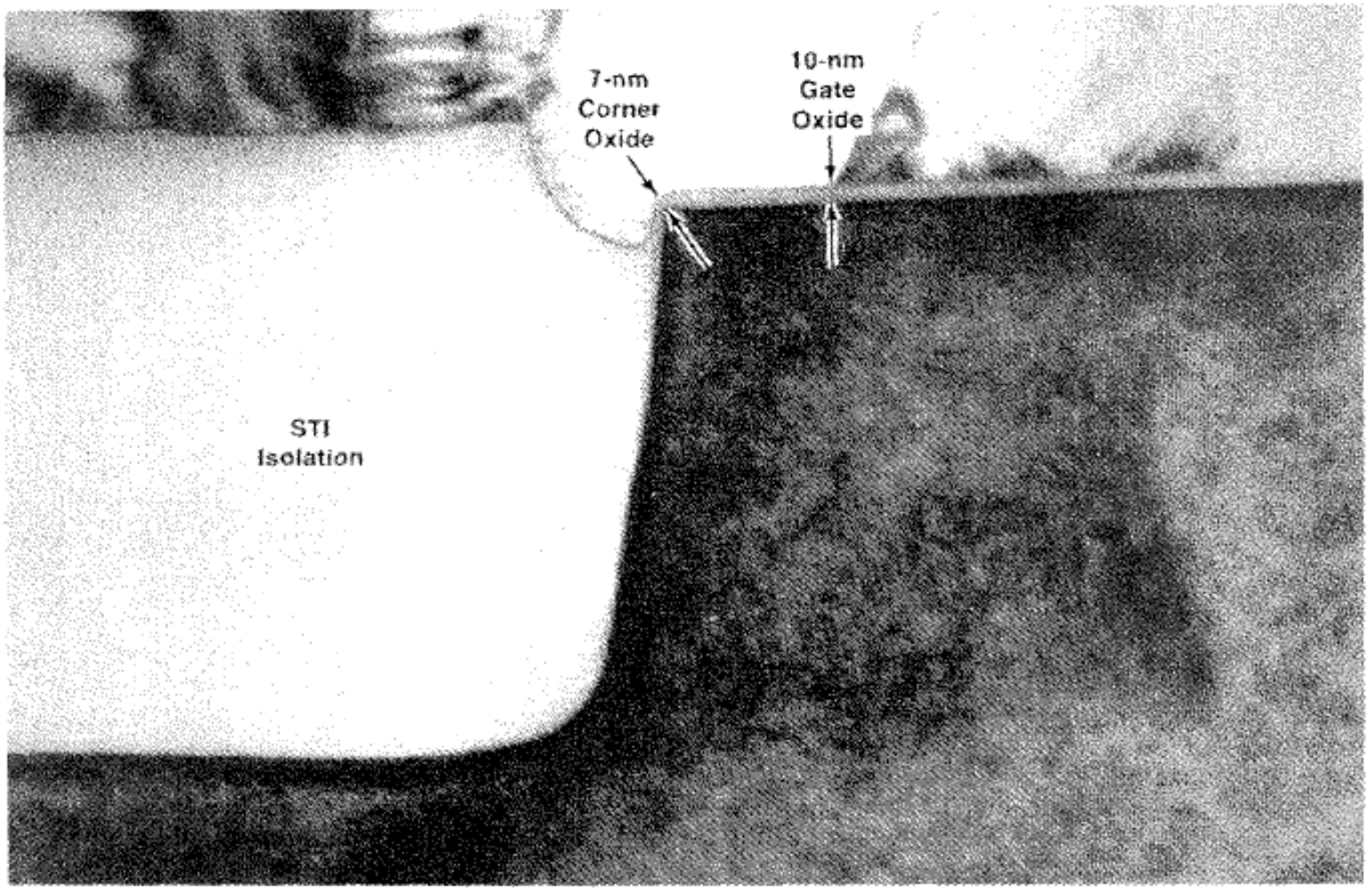
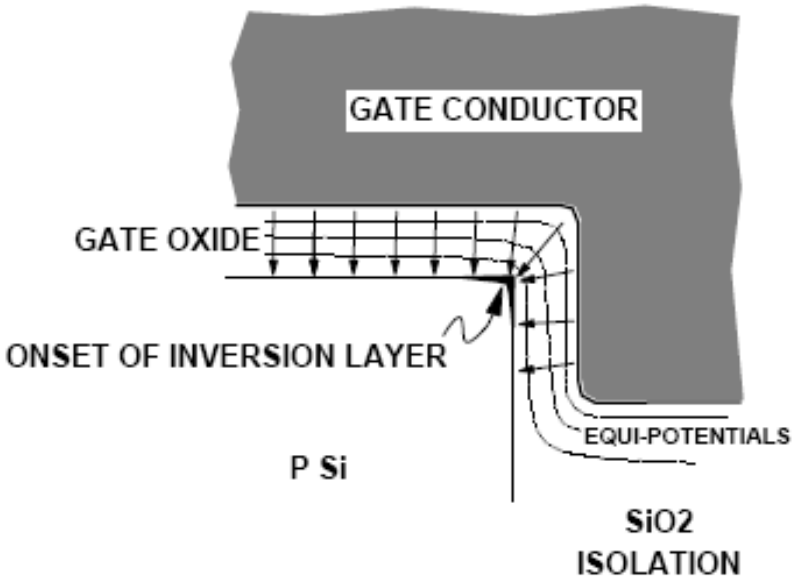


Figure 11. Cross section through the width of a MOSFET isolated by shallow trench dielectric.

OVERVIEW OF PROBLEM TO BE SOLVED

US 5,798,553

ELECTRIC POTENTIALS AND FIELDS IN THE VICINITY OF THE SILICON CORNER:



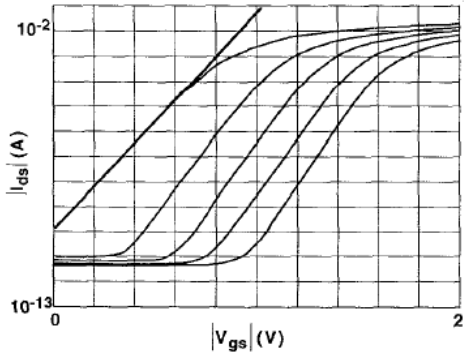
- ELECTRIC FIELD IS STRONGEST AT THE SILICON CORNER

  - DUE TO SMALL RADIUS OF CURVATURE
  - HIGHER CORNER FIELD
    → STRONGER INFLUENCE OF GATE VOLTAGE ON Si SURFACE POTENTIAL
    → CORNER INVERTS FIRST
    → Vt corner < Vt planar

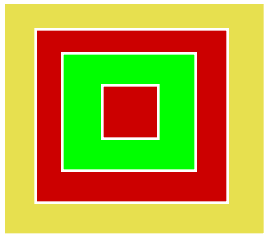
Physical Evidence: Measured Data - Same Wafer

❖MOS Characteristic of device specifically designed without a corner

(Note, this is NOT a solution!)
This design is an annular device ring. Large, leaky, not optimized…



ure 13. IV characteristics of diffusion isolated BC-PFET. Device geometry W_{eff}/L_{eff} = 500µm/0.53µm; bias conditions are V_{ds} = -2.8, V_{gs} = 0.0V to -2.0V, V_{nw} = 0.0V to 4.0V. The drawn subthreshold slope at V_{nw} = 0.0V does not indicate the presence of the conducting edge.



❖MOS Characteristic standard device design

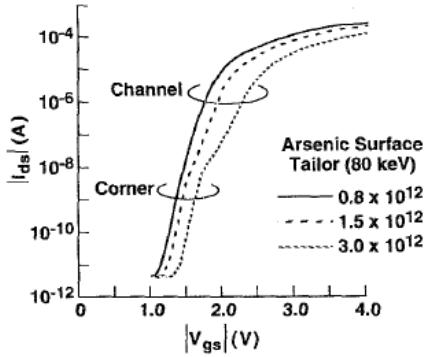
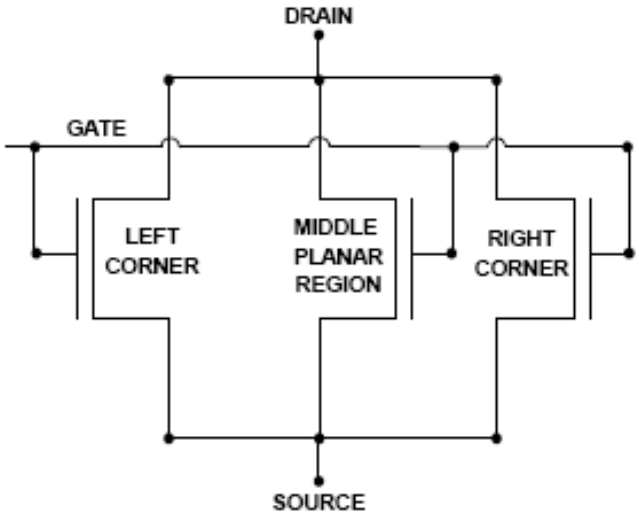


Figure 2. IV characteristics of SC-PFET. Increased arsenic dose separates corner and channel contribution with a different subthreshold slope. Device geometry W_{eff}/L_{eff} = 20µm/3µm; bias conditions are V_{ds} = -3.6V, V_{nw} = 0.0V.

OVERVIEW OF PROBLEM TO BE SOLVED

US 5,798,553

SIMPLE DC STEADY-STATE EQUIVALENT CIRCUIT OF SHALLOW TRENCH BOUNDED MOSFET:



- Vt (CORNER MOSFETs) < Vt (MIDDLE MOSFET)
  → **OFF-CURRENT DOMINATED BY CORNERS**

- BUT, EQUIVALENT (ELECTRICAL) CHANNEL WIDTH OF CORNER MOSFETs IS TYPICALLY << PHYSICAL CHANNEL WIDTH OF MIDDLE MOSFET (W)
  → **ON-CURRENT DOMINATED BY MIDDLE**
  - ON-CURRENT ∝ W
  - CORNERS CONTRIBUTE NEGLIGIBLY TO ON-CURRENT

OVERVIEW OF PROBLEM TO BE SOLVED

US 5,798,553

SIMULATED I_S-V_{GS} CHARACTERISTICS

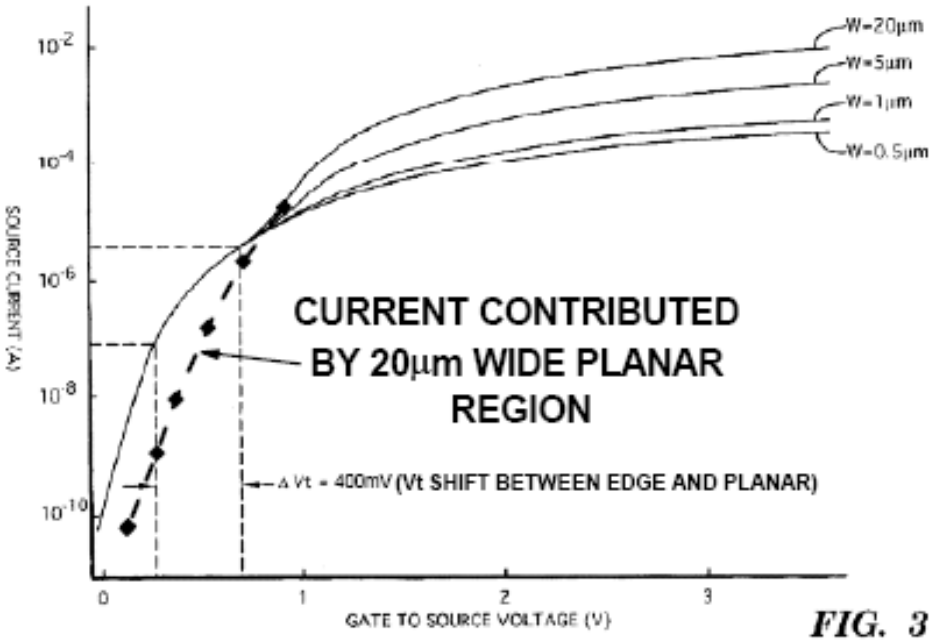


FIG. 3

- CORNERS DOMINATE OFF-CURRENT (V_{GS}=0)
- PLANAR REGION DOMINATES ON-CURRENT (V_{GS} > Vt(PLANAR) ≈ 0.70V) FOR TYPICALLY EMPLOYED CHANNEL WIDTHS (W ≳ 0.5μm) FOR HIGH PERFORMANCE APPLICATIONS
- Vt(PLANAR) – Vt(CORNER) ≈ 400mV
- PROMINENT KINK IN CHARACTERISTIC

OVERVIEW OF PROBLEM TO BE SOLVED

US 5,798,553

- NEED HIGHEST ON-CURRENT FOR HIGHEST PERFORMANCE
  - $dV/dt = I_{ON}/C_{LOAD}$
- NEED LOWEST OFF-CURRENT FOR LOWEST STANDBY POWER
  - LOW POWER (BATTERY) APPLICATIONS

→ MUST MINIMIZE CORNER CURRENT

- CORNER CURRENT INCREASES STANDBY POWER WITHOUT CONTRIBUTING TO PERFORMANCE

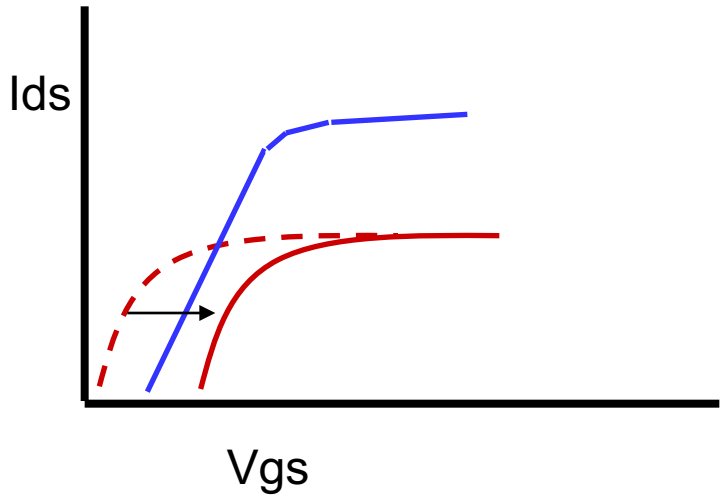
OR

- HIGHER OVERALL Vt's REQUIRED TO MEET STANDBY POWER TARGET DEGRADES PERFORMANCE

∴ **INVENTION SEEKS TO SUPPRESS CORNER CURRENT WITHOUT DEGRADING CURRENT FROM MIDDLE PLANAR REGION**

THE SOLUTION
US 5,798,553

- MAKE Vt (CORNER) ≥ Vt (PLANAR REGION)
  - SELECTIVELY INCREASE CHANNEL DOPING CONCENTRATION AT THE CORNERS BUT NOT AT THE MIDDLE PLANAR REGION



THE SOLUTION
US 5,798,553

FIG. 2A

- STARTING WITH A STANDARD MONOCRYSTALLINE SILICON SUBSTRATE (WAFER)
  - THERMALLY GROW A THIN (PAD) OXIDE
  - DEPOSIT A SILICON NITRIDE PAD LAYER BY CHEMICAL VAPOR DEPOSITION (CVD)

THE SOLUTION

US 5,798,553

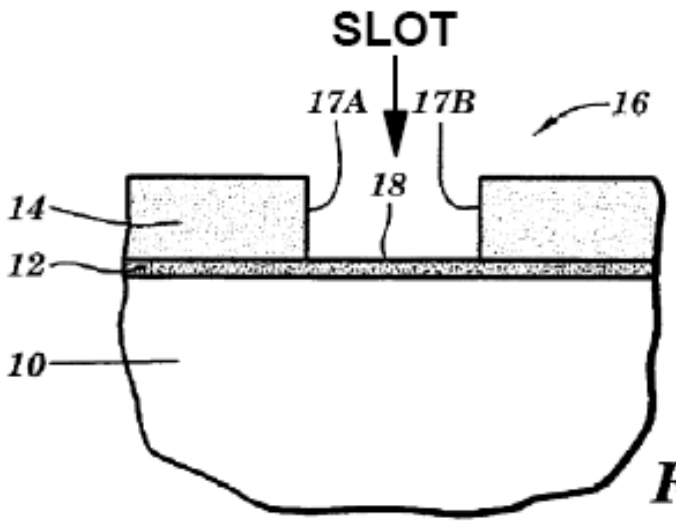


FIG. 2B

- USING A PHOTORESIST MASK (NOT SHOWN), ETCH A SLOT THROUGH THE NITRIDE PAD
  - USE OF AN ANISOTROPIC (DIRECTIONAL) REACTIVE ION ETCH (RIE) FOR SiN SELECTIVE TO SiO2

THE SOLUTION

US 5,798,553

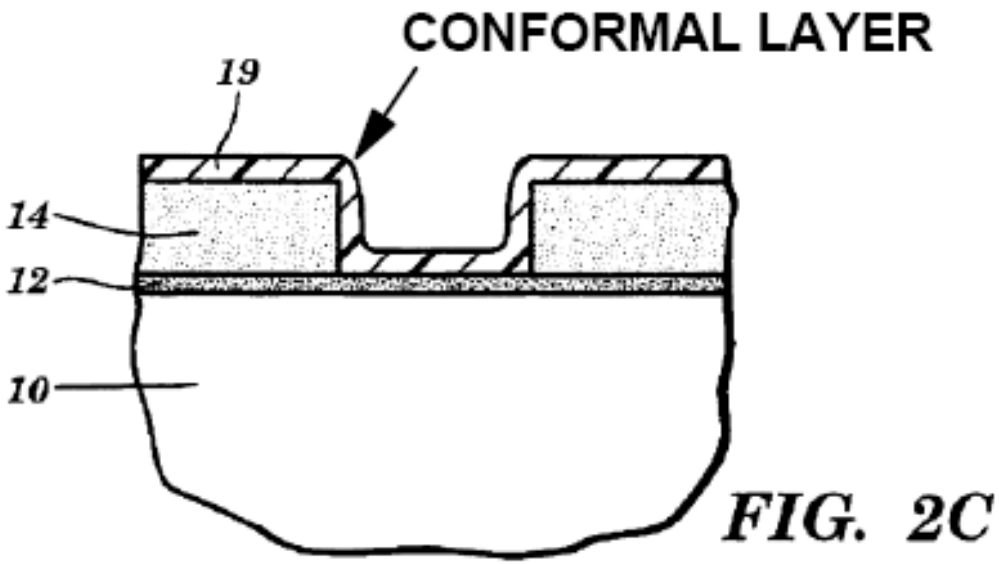


FIG. 2C

- DEPOSIT A CONFORMAL LAYER
  - e.g. CVD SiO2, OR A POLYMER

THE SOLUTION
US 5,798,553

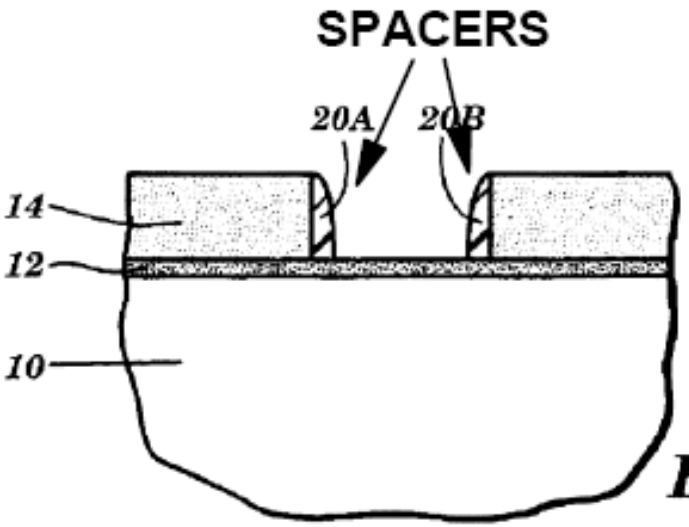


FIG. 2D

- USE A REACTIVE ION ETCH (RIE) TO DIRECTIONALLY ETCH THE CONFORMAL LAYER

  - ETCHES HORIZONTAL SURFACES MUCH FASTER THAN VERTICAL SURFACES

→ FORMS SIDEWALL SPACERS IN SLOT

THE SOLUTION

US 5,798,553

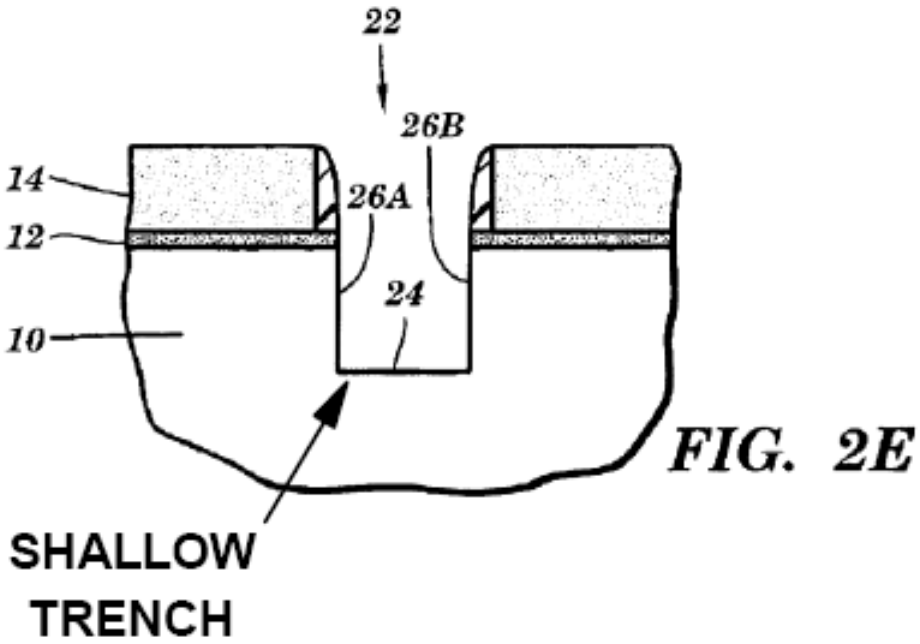


FIG. 2E

- USE A REACTIVE ION ETCH (RIE) TO DIRECTIONALLY ETCH THROUGH THE REMAINING PAD OXIDE LAYER (12)
- USE A SILICON RIE (CHANGE ETCH CHEMISTRY) TO DIRECTIONALLY ETCH SHALLOW TRENCHES (24) INTO SILICON

THE SOLUTION
US 5,798,553

SPACER REMOVAL

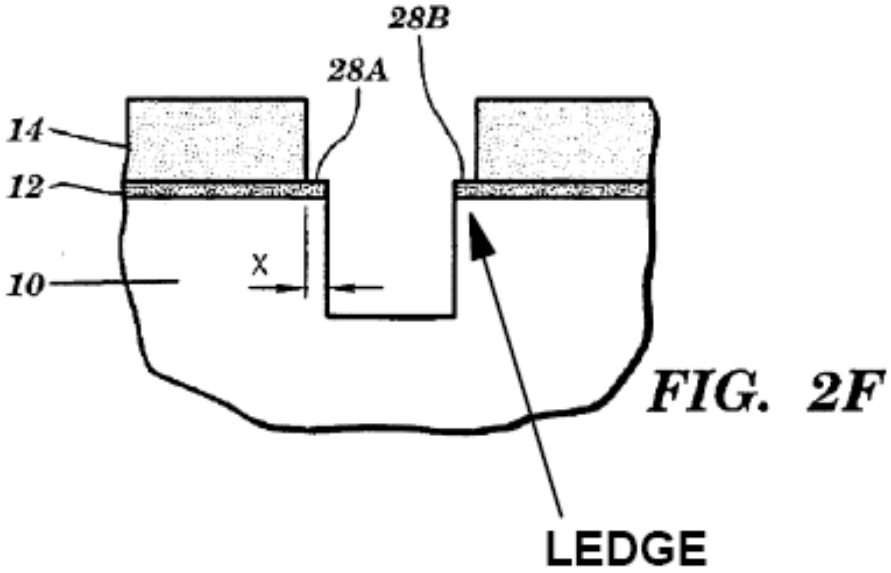


FIG. 2F

- USE AN ISOTROPIC (WET OR DRY) ETCH TO REMOVE THE SPACERS SELECTIVE TO NITRIDE AND SILICON

  - LEAVES A LEDGE OF LENGTH X (SPACER THICKNESS) WHICH IS NOT COVERED BY NITRIDE PAD
  - A PORTION OF PAD OXIDE (12) MAY BE REMOVED BY THIS ETCH

THE SOLUTION
US 5,798,553

LEDGE IMPLANT

- P-TYPE FOR NFET
- N-TYPE FOR PFET

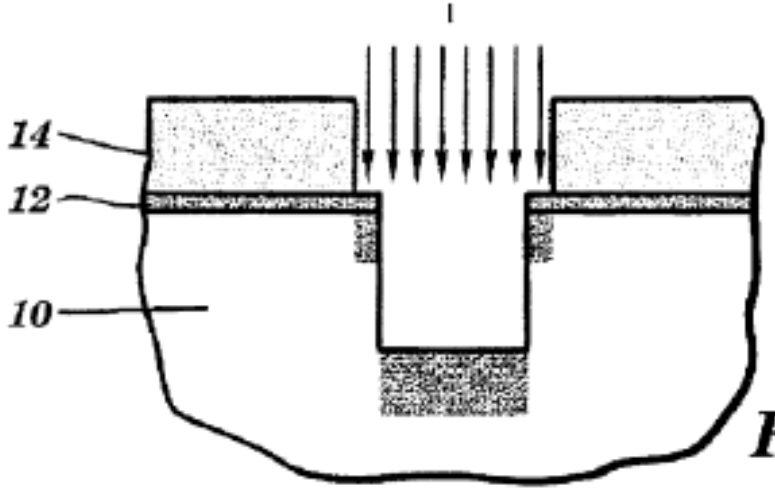


FIG. 2G

- ION IMPLANT THE LEDGE
  - SELECTIVELY DOPES EDGE HIGHER THAN MIDDLE PLANAR REGION
  - RAISES Vt (CORNER) ≥ Vt (PLANAR)

THE SOLUTION

US 5,798,553

SIMULATED I_S-V_{GS} CHARACTERISTICS

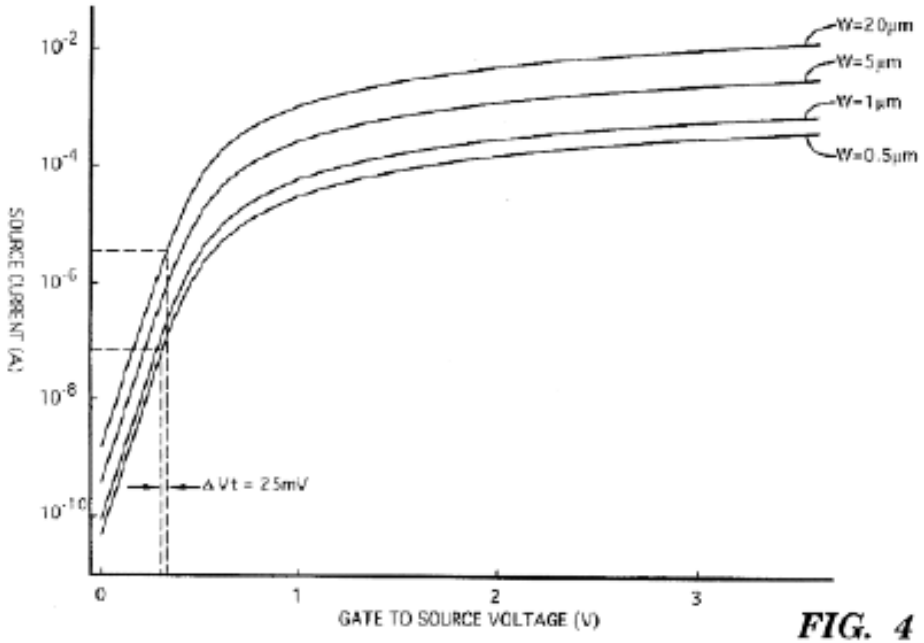


FIG. 4

- Vt(PLANAR) – Vt(CORNER) = 25mV
  - INVENTION PROVIDES A FACTOR OF 16 REDUCTION IN Vt MISMATCH !
  - FOR W=20μm, Vt(PLANAR) MAY BE REDUCED BY ≈ 250mV WITHOUT EXCEEDING OFF-CURRENT TARGET OF 0.1nA
    → 250mV INCREASED OVERDRIVE (V_{GS}-Vt)
    → SIGNIFICANT PERFORMANCE BOOST

COMMENTS ON PATENT
US 5,798,553

- WHAT IS NEW?
- WHAT IS USEFUL?
- WHAT IS NON OBVIOUS?

Can you Publish ?

File Date: 9/16/1997
Issue Date: 8/25/1998

Impact of Shallow Trench Isolation on Reliability of Buried- and Surface-Channel sub-μm PFET

William Tonti *, Ronald Bolam
IBM Microelectronics Division
Essex Junction, Vermont 05452
* (802) 769-6561 (Fax 6567) wtonti@btvlabvm.vnet.ibm.com

Wilfried Hänsch
SIEMENS Components Incorporated
c/o IBM Microelectronics
Essex Junction, Vermont 05452

Abstract

Shallow trench isolation exhibits all the required isolation-technology properties for ULSI [1]. Its high degree of scaleability relies on the fact that its lateral (isolation width) and vertical (isolation depth) dimensions are decoupled due to an almost-ideal box-shape profile of the isolation (Figure 1). A consequence of the abrupt device edge is that a parasitic drain-to-source leakage path can exist at the corner and along the trench sidewall. This paper describes degradation mechanisms of surface-channel (SC) and buried-channel (BC) PFET devices that are directly related with a corner and sidewall parasitic leakage. Both parasitic regions show a characteristic degradation behavior that can limit device reliability for PFETs in the sub-μm regime. The necessary processing conditions that overcome this limitation are also given.

Introduction

The effects of hot carrier degradation on P-channel device characteristics become more important as MOSFET dimensions continue to shrink [2,3,4]. Electron charge trapping and interface state generation are the main contributors to the degradation [5]. This results in a positive threshold shift and an increased source-to-drain drive current.

To improve circuit performance, scaling the device active area and isolation is essential. Reducing channel length and oxide thickness increases drive current capability. The reduced oxide thickness improves the subthreshold slope which, in turn, reduces the device off current (I_{ds} at V_{gs}=0.0V). This scaling trend is essential for today's low-power MOSFET operation requirements.

Shallow trench isolation (STI) provides additional leverage by reducing the isolation feature size; however, a reliability mechanism related to the isolation properties can increase the device off current. A localized hot carrier degradation at the STI-drain-gate region reduces the expected scaling improvement. Figure 1 depicts a two-dimensional cross section, where the drain of the MOSFET would be located in the third dimension. Traditional hot carrier degradation could occur in this dimension and device damage would result [4]. The damaged region would be located along the third dimension bordering the drain, corner and polysilicon gate intersection. The hot carrier mechanism adversely affects drain leakage currents along the boundary; the consequence of hot carrier degradation in subthreshold operation for SC and BC PFET devices are discussed in this paper.

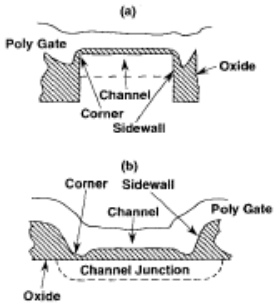


Figure 1. (a) A cross section through the width of a shallow trench bounded MOSFET. The dashed line is the location of the BC-PFET channel junction. The poly recess at the device edges is the gate wraparound. (b) is the equivalent planar structure of (a).

Experiment

To investigate edge hot carrier degradation in STI isolation, we used buried-channel and surface-channel PFETs with a gate oxide thickness of 10.0nm and optimized design lengths of 0.4μm and 0.3μm, respectively [6]. Both devices shared the same N-well in an N substrate and followed the same process sequence: formation of shallow trench isolation, well implants, gate oxide, N^+ polysilicon gate electrode, and source-drain diffusions [7]. The substrate doping concentration was $\approx 1.0 \times 10^{16}$ cm^{-3}. An N-well mask was used to implant the field tailor and anti-punch through doping through a screening oxide into the channel and isolation regions. A second threshold voltage compensation mask was used to independently adjust the surface concentration in the respective channel regions of these devices. The device threshold characteristics were set by using the compensation mask to vary an arsenic threshold-tailor implant for the SC-PFET and a boron implant for the BC-PFET. The resulting buried-layer junction depth for the BC-PFET was

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MY PERSPECTIVE OF FACTORS CONDUCIVE TO SUCCESSFUL INVENTING

- COLLABORATIVE EFFORT
  - NOT FOR LONERS
  - TEAM WITH COMPLEMENTARY SKILLS
  - SYNERGISM→SPARKS NEW IDEAS
- BROAD PERSPECTIVE OF THE ART
  - IMPROVES WITH EXPERIENCE
- THE RIGHT OPPORTUNITIES
  - CHALLENGING PROJECTS
  - BLESSINGS OF MANAGEMENT
- A PASSION FOR SEEKING SOLUTIONS
- PERSISTENCE
  - DOGGED DETERMINATION
- WILLINGNESS TO PURSUE OUTRAGEOUS IDEAS
  - PARADIGM SHIFTS

Acknowledgements

❖ I would like to acknowledge my co inventor and long time friend Dr. Jack Mandelman who has prepared many of the visuals contained in this package.

Questions ?? Ask The....

William Tonti
w.r.tonti@ieee.org
802 238 5401