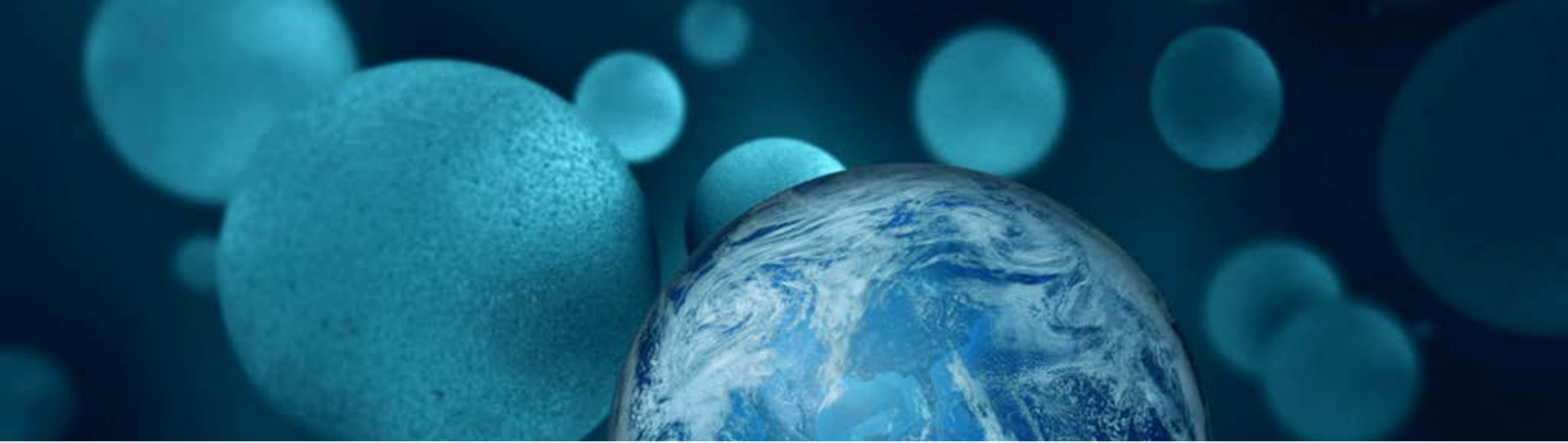


ThermoFisher SCIENTIFIC

ESD System Level / Device Level Testing Pitfalls and Concerns

Tom Meuse
Applications Engineer – Compliance Test Solutions

We Are The World Leader in Serving Science

Global Scale

- Approximately 65,000 employees globally
- More than $20 billion in annual revenue
- Unparalleled commercial reach

Unmatched Depth

- Leading innovative technologies
- Deep applications expertise
- Premier laboratory productivity partner

ThermoFisher SCIENTIFIC

thermo scientific | applied biosystems | invitrogen | fisher scientific | unity lab services

Our Mission: To enable our customers to make the world healthier, cleaner and safer

First, I’d like to thank our hosts for arranging the meeting, dinner and refreshments tonight !!

Overview / Agenda

- With all the different test standards and testing methods, System Level and device level ESD testing can be confusing and lead to questionable results.
- Most System Level tests rely on discharges from handheld simulators being brought into contact with different points on a complete “system”. These discharges can be affected by numerous issues, from environmental to human inconstancies during the testing.
- Device level testing, although better controlled can also lead to questionable results, due to inconstancies in the test requirements and misunderstanding of the results.
- *We’ll review some of the pitfalls associated with the System Level and device level testing methods and their impact on the product and protection designs.*
- *In addition, we’ll review some of the new approaches to System Level design, looking at new “co-operation” methods between System and device ESD protection designers.*

Recent conversations on system level testing

- During the recent EOS/ESD Symposium in Reno NV, a Workshop was held to discuss System Level testing and how to improve system ESD qualification
- With so many standards in use, the question was asked, “What does industry really need for a test method for verifying ESD threshold levels for system designs?
- This question is being asked, because even after so many years of system level testing using the IEC 61000-4-2 standard as a reference, new types of “stress events” have been introduced, adding some uncertainties.
- In addition, OEM’s have begun requesting their IC suppliers meet system level requirements at the device level and this has introduced a new dimension to qualifying devices / systems for ESD withstand thresholds!!

System Level Testing – IEC 61000-4-2 standard

- Most widely used System Level ESD test method – IEC 61000-4-2 standard
  - Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test

- This test includes different methods of failure detection, including both soft and hard failures. Hard failures are easy to detect and analyze, however soft failures posse other issues
  - Soft failures require the Equipment Under Test (EUT) to be functioning and observations need to be made to determine as to what extent the EUT has “hiccupped” during the testing
    a) Normal performance
    b) Temporary loss of function or degradation of performance but *does not require* user intervention to clear
    c) Temporary loss of function or degradation of performance but *requires* user intervention to clear
    d) Hard failure – loss of function or degradation of performance and is not recoverable

System Level Testing – IEC 61000-4-2 standard

- The ESD event, which is meant to represent a person holding a metal object (screw driver, key, etc..) becoming charged and then discharging using a combination of contact and air discharge directly into the test subject or indirectly via coupling planes adjacent to the system under test
  - Air discharge introduces variables which make it difficult to have repeatability and reproducibility
  - In addition, ESD simulators (ESD guns) introduce variability's, as things like, speed of approach, angle of approach and the “gun” being used, all affect the energy introduced into the Equipment Under Test (EUT)
    - Some users have begun using robot arms to minimize the affect the human interaction has on the testing when using the ESD guns
      - This does a couple things, eliminates human inconsistencies and eliminates the repetitive testing on the operator – most tests require 10 pulses in both polarities, so this can be a lengthy test especially when holding the ESD gun

System Level Testing – IEC 61000-4-2 Waveform

- The IEC 61000-4-2 waveform simulates two different events
  - The first is the initial, short duration fast rise time event which represents the metal object discharging
  - The second event is the slow exponential decay discharge which represents the human body discharging – this is similar to the HBM used for device level testing
  - The simplified circuit for this model is 150pF / 330 ohms

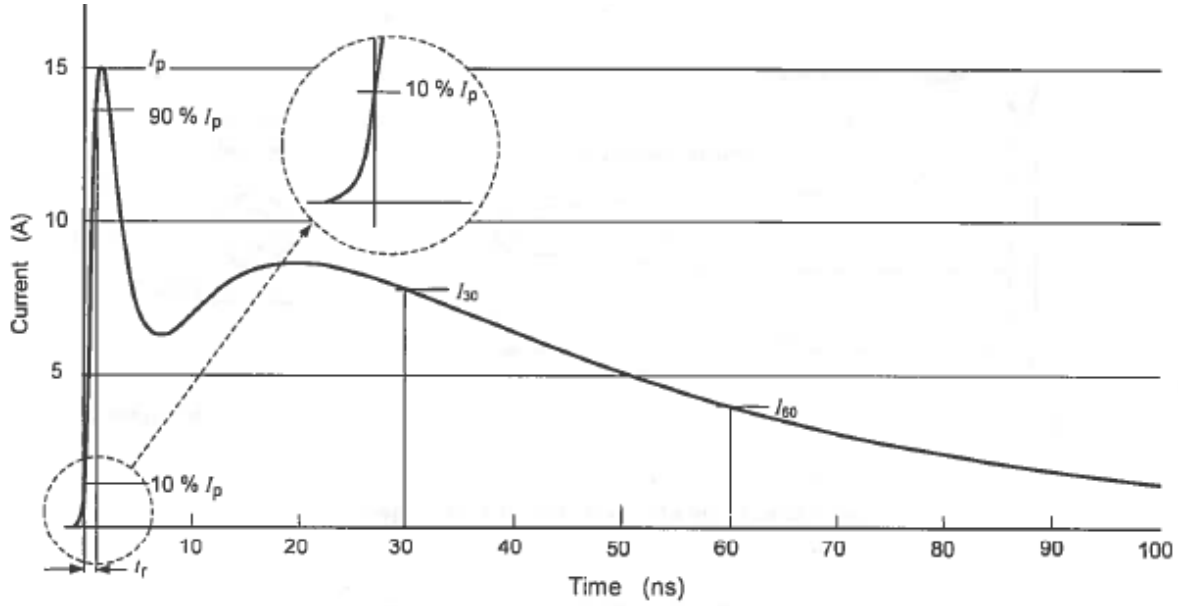


Figure 2 – Ideal contact discharge current waveform at 4 kV

System Level Testing – IEC 61000-4-2 Test Setup

- The test setup can be cumbersome at best
  - Insulated (wooden) table
  - Metal planes on the table top and the floor, with proper resistance between the two planes
  - Once again, ESD gun is manually brought into contact with the EUT
- Issues with the setup can include
  - Improper table material
  - Improper grounding between planes
  - ESD guns not properly grounded
- All of these issues can lead to questionable results, as currents may flow to ground rather than the EUT

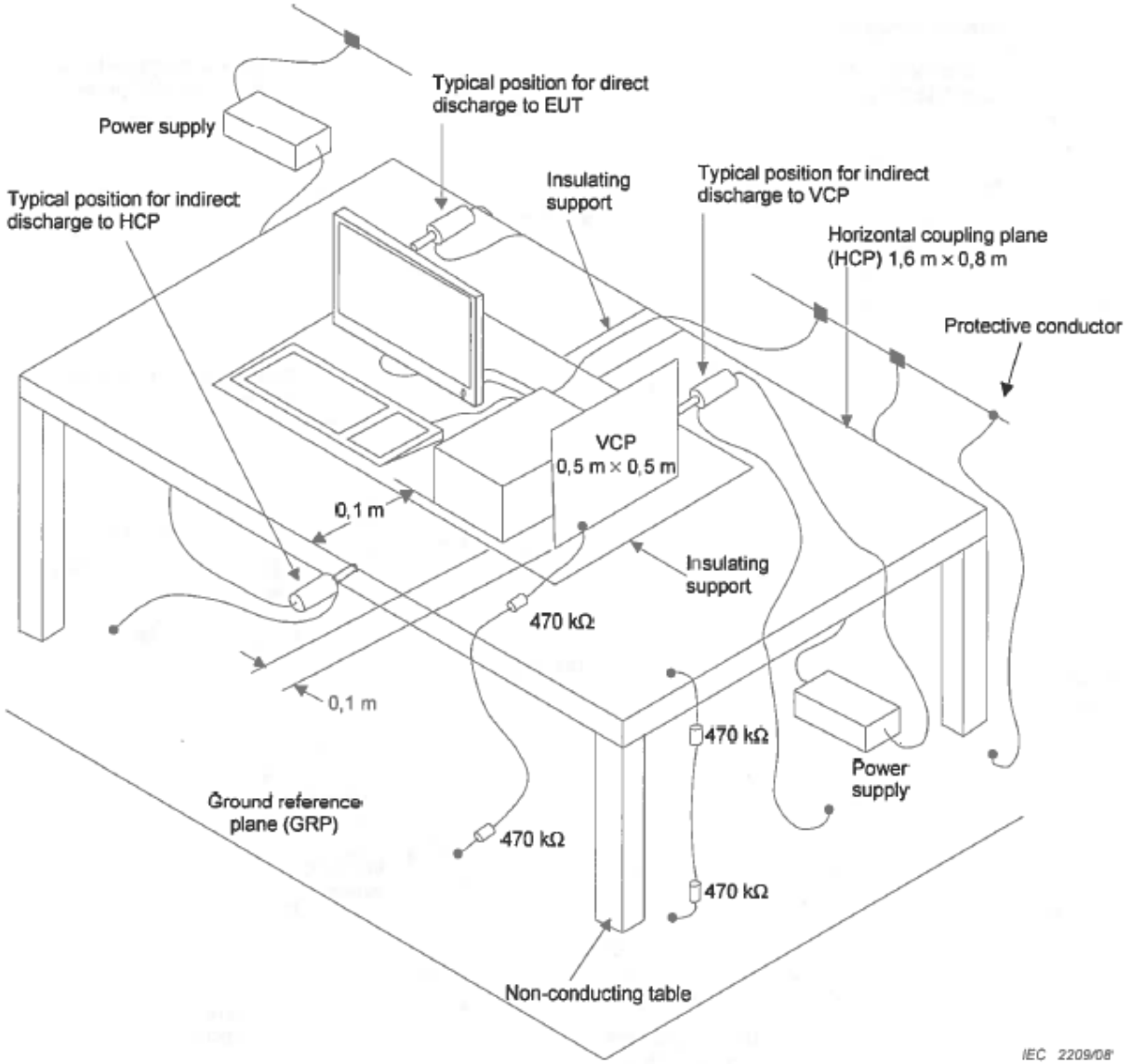


Figure 4 – Example of test set-up for table-top equipment, laboratory tests

ThermoFisher SCIENTIFIC

System Level Testing – IEC 61000-4-2 Test Setup

- The test setup can be cumbersome at best
  - There are also setups for
    - Non-grounded table top equipment
    - Grounded floor-standing equipment
    - Non-grounded floor-standing equipment
  - Each of these setups posses their own set of issues which can lead to questionable results

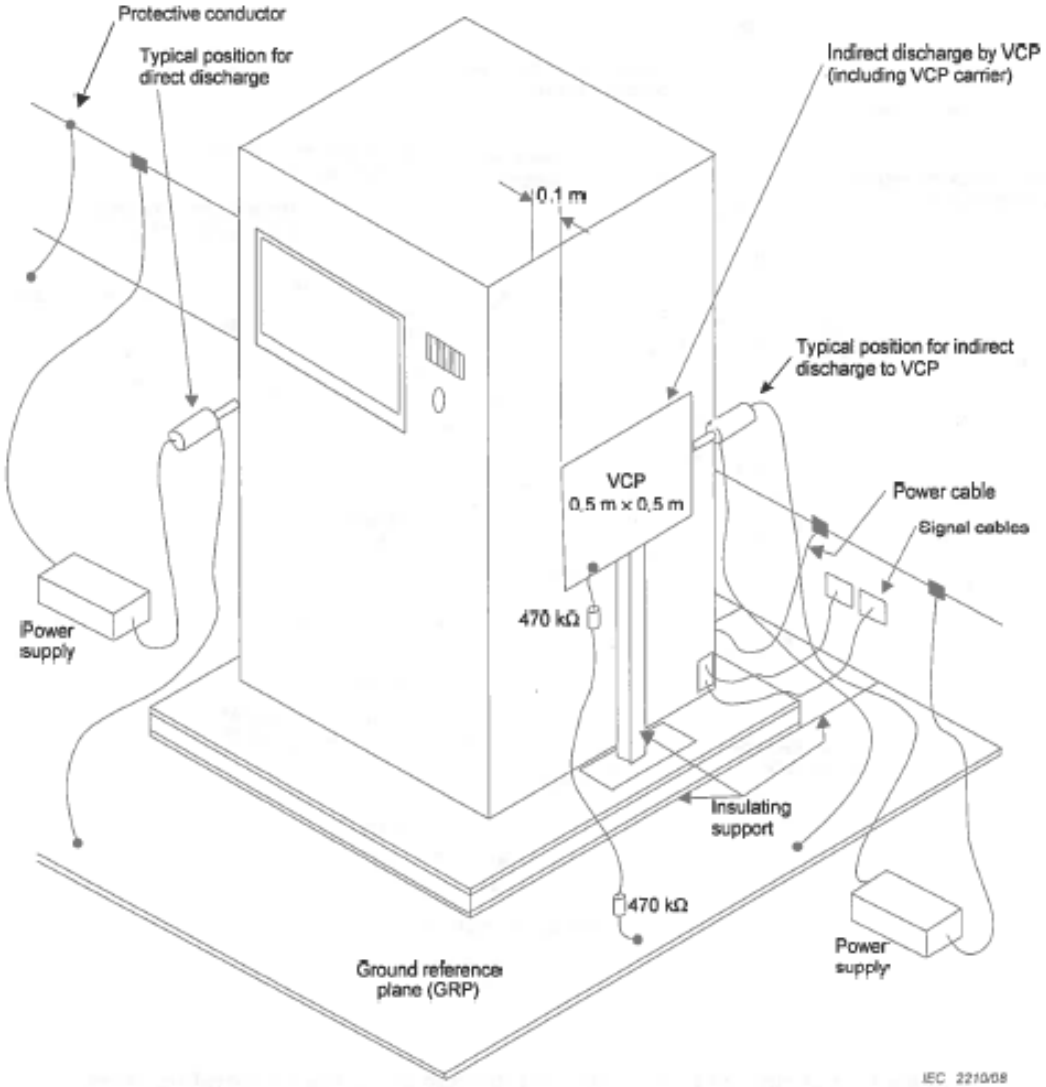


Figure 5 – Example of test setup for floor-standing equipment, laboratory tests

ThermoFisher SCIENTIFIC

System Level Testing – IEC 61000-4-2 Test Setup

- The test method requires certain points of the EUT be directly stressed, however it also lists numerous points that shouldn't be stressed
  - Pins on connectors with metal shells should not be directly stressed, only the outer shell would be stressed
    - This draws a lot of confusion, as it would be expected that a real world discharge might hit one of the pins of the connector
    - There is also a mention, that the rationale for not testing some of the pins is that they may be high performance pins and may not have adequate ESD protection in their path
      - *More of a reason to test them, if you ask me*
  - Indirect application of the discharge is also required
    - Horizontal and vertical coupling planes are positioned around the EUT and discharges are made to the planes to try and cause interrupts
      - Some issues with this testing is the location of the planes is critical and isn't always followed

System Level Testing

- The pressure on system level ESD robustness to guarantee the reliability of systems is increasing, as we have more and more embedded electronics. From equipment manufacturers, it is crucial to assume that their systems can withstand ESD events, so the electronic parts will survive in their final application.

- Papers presented in recent years show that, depending on the system application, devices are not exposed to the same stresses. So when we are talking about IEC 61000-4-2, is it really the relevant ESD stress?

- The following pages show just some of the standards being used within industry for “system level testing”

System Level Testing

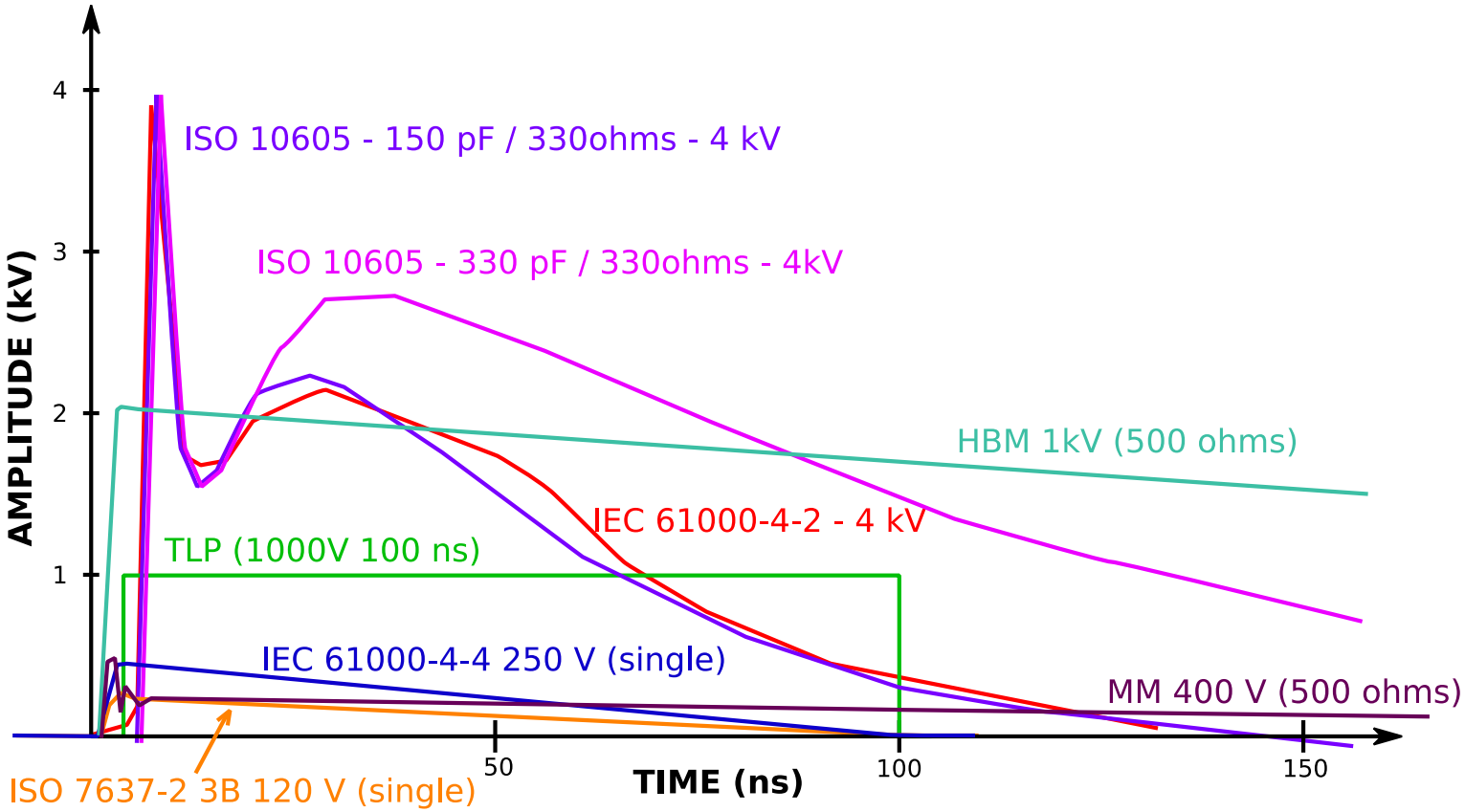
- **Exhaustive list of standards….**

Domains	Standard	Remarks
Aeronautic	DO-160 ABD100 …	International AIRBUS specific. **Close to D0160**
Military	MIL-STD-461 STANAG 4437 ECTP 500 AECTP-501 …	Military Standard for EMC test equipment **OTAN** Standardization Agreement Electromagnetic Environnemental Effects Equipment & sub system EMI testing
Automotive	ISO 7637 ISO 10605 ISO 26262 AEC Q100 AEC Q200 …	Electrical disturbances (ED) ED from electrostatic discharge Functional safety Stress test qualification Packaged ICs Stress test qualification Passives
Medical	IEC 60601 ISO 14971 …	Safety of medical electrical equipment Risk management to medical devices
Spatial	ECSS-E-ST-20-07C …	Space engineering EMC
Civil	IEC 61000 JEDEC JESD22 ANSI …	ESD EOS, Fast transient

In addition, there's a large number of waveforms in all these standards…

System Level Testing

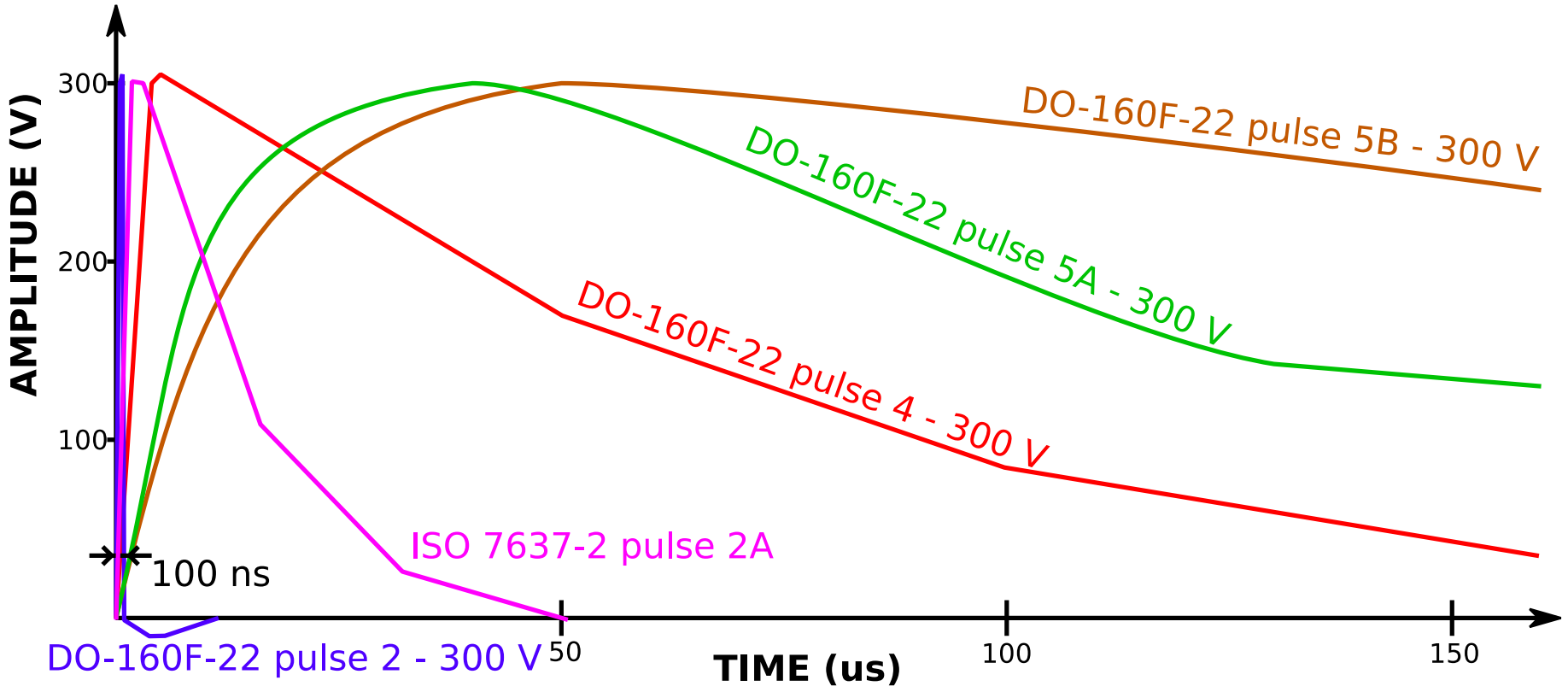
- **A lot of standards (system level) exist for qualifying products - Nanosecond scale…**



ThermoFisher SCIENTIFIC

System Level Testing

- **A lot of standards (system level) exist for qualifying products - Microsecond scale…**



ThermoFisher SCIENTIFIC

System Level Testing but at the device level

- As was mentioned, some OEM's are requiring their IC suppliers to provide system level test information for their devices
  - As it's difficult to perform testing of a device using an ESD gun, the ESD Assoc. developed a work group (WG 5.6), who subsequently developed a method for performing testing of a device using an IEC like waveform – this working group and the method is referred to as HMM (Human Metal Model) testing
  - Although this working group developed a method so people being required to perform the test could all do it the same, there are still concerns, "qualifying a device using the IEC waveform will not guarantee good system level performance"
    - Why – once the device is mounted on a PCB and a discharge occurs, say on the chassis, the waveform doesn't look anything like the IEC waveform when it reaches the device
    - Additionally, other items such as TVS would most likely be in the circuit and these may actually cause the devices ESD protection to function incorrectly or not at all !!

System Level Testing but at the device level

- In an attempt to further highlight whether qualifying a device against the IEC waveform provides any insurance for system level designs, the Industry Council on ESD Target Levels developed a number of white papers on the subject
  - White Paper 3, System Level ESD Part I: Common Misconceptions and recommended Basic Approaches
  - White Paper 3, System Level ESD Part II: Implementation of Effective ESD Robust Designs

These and other white papers from the Council can be found on the ESDA website

https://www.esda.org/standards/complimentary-downloads/

System Level Design Considerations

- In addition to discussing the misconceptions of system level testing, these white papers also introduced a method of co-operation between system designers and device designers
  - System-Efficient ESD Design (SEED)
    - Co-design methodology of on-board and on-chip ESD protection to achieve system level ESD robustness
- This method relies on the transfer of data between device designers (manufacturers) and system level designers
  - The idea is to have device designers provide TLP (Transmission Line Pulse) data to the system level designer, so they can use this knowledge and fold it into their protection schemes on their PCB designs
    - Where would TVS need to be placed?
    - What variety would be required to protect the device being used?
    - How would the TVS interact with the device, based on the TLP knowledge?

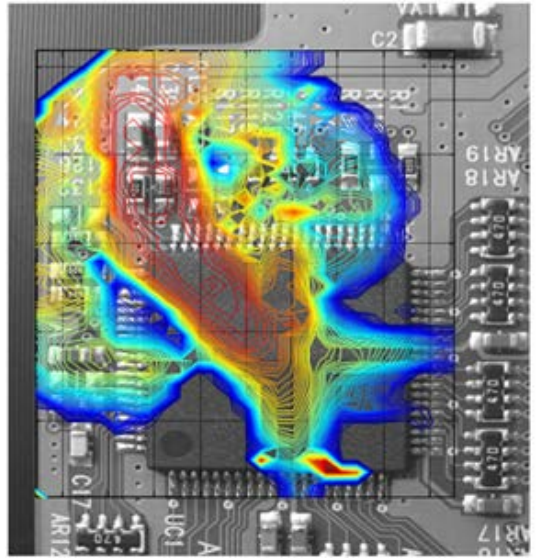
System Level Design Considerations

- To further the SEED concept, a working group within the ESDA was formed to develop ESD Modeling methods, which could be developed and used as plug-ins for simulation software packages, like Spice
  - WG 26 ESD Modeling is developing documents to explain what is required when developing these models, mainly it uses TLP data to develop the models
- Some system level designers try to correlate system level protection versus device level HBM/CDM withstand threshold levels
  - Although this sounds reasonable and the threshold levels from device level testing may help the designer, these threshold levels are actually gathered for the device manufacturing purposes
    - For a given device threshold level, a device manufacturing facility's ESD process control level must be designed so as to ensure no voltages go beyond the lowest device threshold level. i.e. if a device has a 250V threshold, the manufacturing process should be designed to control the process to 100V

System Level Design – Failure Analysis

- Diagnosing failures can be difficult, especially soft failures. Unlike hard failures, where a device is damaged and root analysis can determine what type of event caused the failure, soft failures don't usually leave a "trace"
  - So in many cases, redesigns occur based on knowledge and some times luck when trying to eliminate a failure either during qualification or worse yet, a field failure!

- Some new methods, like EMC scanning techniques can be useful tools when debugging a system design problem
  - ANSI/ESD SP14.5 standard practice document from the ESDA discusses a method of EMC scanning which allows the designer to virtually see where the current flows on the PCB when a discharge occurs on the PCB or perhaps on a connector
    - ANSI/ESD SP14.5 Near-field Immunity Scanning, Component/Module/PCB Level
  - There are other scanning techniques available to help isolate failure paths and provide system designers with information to help in the redesign of the protection approaches



Device Level Testing

- **Qualifying devices to determine their ESD withstand threshold level**
  - As was mentioned previously, these threshold levels are actually gathered for the device manufacturing purposes, to ensure the ESD protection process in the factory will allow the device to be manufactured and handled without causing any failures

- There are many different standards, even duplicates of standards across different Standards Bodies. This of course has caused confusion and in some cases caused device manufacturers to test to multiple standards, when in reality they're doing a similar test on the device to determine its ESD threshold level
  - The ESDA and JEDEC committees have eliminated some of this confusion/multiple work by joining together to develop single documents for the HBM (Human Body Model) and CDM (Charged Device Model) testing methods
    - ANSI/ESDA/JEDEC JS-001, Human Body Model (HBM), Component Level
    - ANSI/ESDA/JEDEC JS-002, Charged Device Model (CDM), Device Level
  - The committee is also working with other Standards Bodies, such as JEITA (Japanese) , AEC (Automotive Electronics Council) and IEC in an attempt to get them to adopt the JS-001 and JS-002 standards - *In some cases, this is a bit of an up hill battle !!*

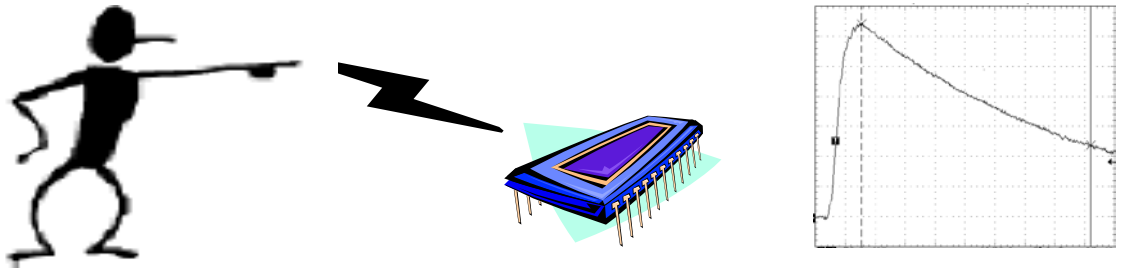
- **Qualifying devices to determine their ESD withstand threshold level**
  - In order to qualify a device to determine it's ESD susceptibility threshold level, both ESDA and JEDEC specify the use of HBM and CDM as the only methods required
  - *MM (Machine Model), which was once required, is no longer required to qualify a device!*
    - The use of Machine Model to qualify a device was being driven by the Japanese and the automotive industry. However, studies have shown that the failure signatures of the HBM and MM events are similar, so there is no need to duplicate testing
      - However, the method is still being used and specified by some companies – there's no way to get away from it ☺
  - There are many different test methods that are in use today, HBM and CDM are the required methods for determining a devices ESD withstand threshold level
    - The following pages highlight some of the device level test methods available today

Device Level Testing – highlighting the different models

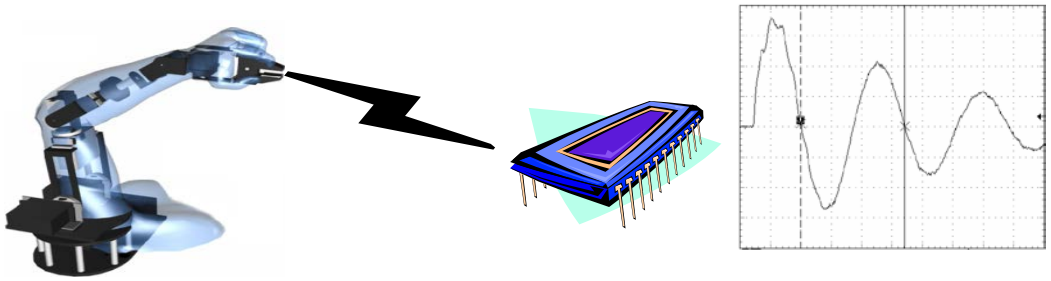
ESD – Electrostatic Discharge

- A person or charged object discharging into a sensitive electronic component or circuit can cause a device to fail or circuit to be upset

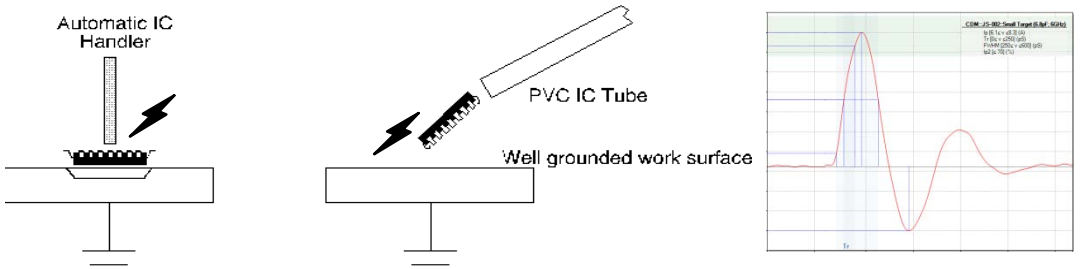
- The threshold of feeling is 2kV to 4kV
- Everyone can feel 5kV*
- 15kV is a ***memorable*** event!!!



Human Body Model Event (HBM) - 100pF/1500 ohm



Machine Model Event (MM) - 200pF/0 ohm

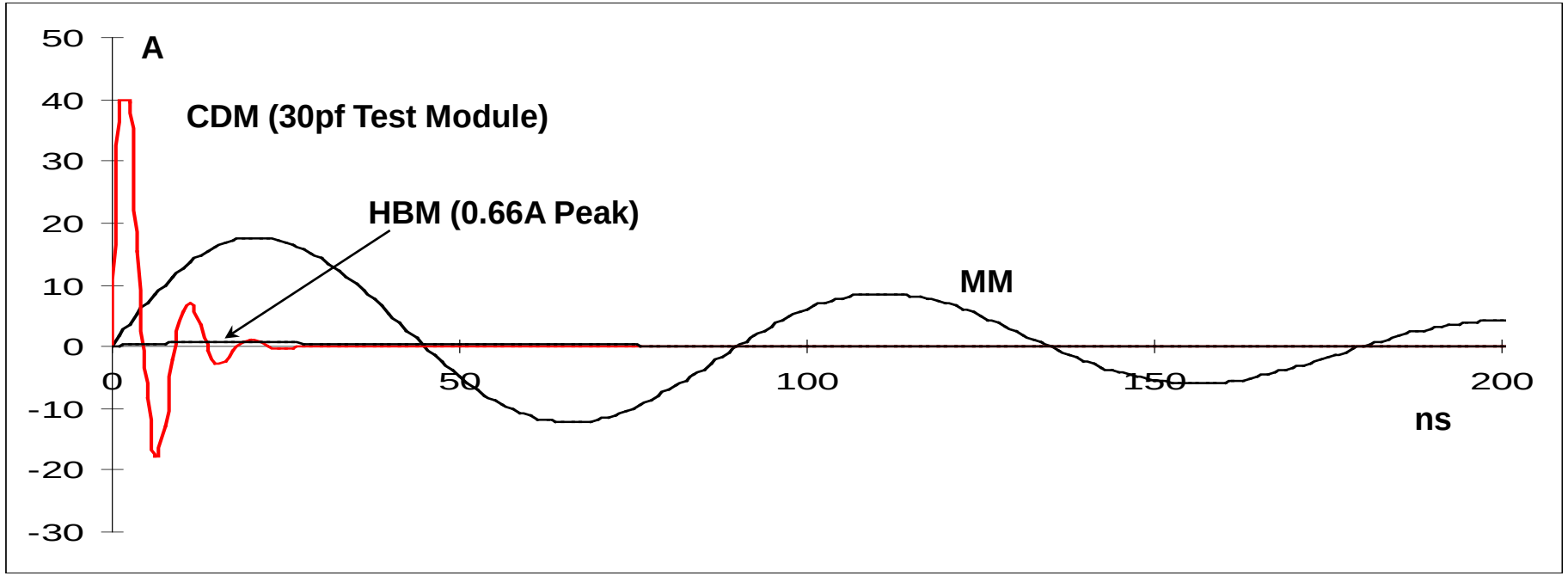


Charged Device Model Event (CDM) - Device Capacitance

ThermoFisher SCIENTIFIC

Overlay of Network Models – highlighting the different models

Comparison of 1kV CDM, HBM and MM discharges



- The CDM discharge is 100x faster than HBM or MM
- The peak current can be 40x that of an HBM pulse

Device Level Testing – highlighting the different models

- **Joint JEDEC and ESD Association standard**
  - JS-001-2017 Human Body Model (HBM)
  - JS-002-2014 Charged Device Model (CDM)
    - A contact method is under development in the Joint JS-002 committee

- ***Electrostatic Discharge Association (ESDA)***
  - ESDA STM5.1 Human Body Model (HBM)
    - Superseded by JS-001-2017
  - ESDA STM5.2 Machine Model (MM)
  - ESDA STM5.3.1 Charged Device Model (CDM)
    - Superseded by JS-002-2017
  - ESDA SP5.4 Transient Latch-up (TLU)
  - ESDA SP5.5 Transmission Line Pulse (TLP/VF-TLP)
  - ESDA SP5.6 Human Metal Model (HMM) 2 pin testing
  - ESDA 14.3 System Level / Cable Discharge Event (CDE)
  - ESDA 14.5 Near-field Immunity Scanning
  - WG 23 Electrical Overstress (EOS)
  - WG 25 Charged Board Event (CBE)
  - WG 26 ESD Modeling
  - WG 27 Electrical Overstress (EOS) in Automotive

- ***Joint Electron Device Engineering Council (JEDEC)***
  - JEDEC JESD22-A114 Human Body Model (HBM)
    - Superseded by JS-001-2014
  - JEDEC JESD22-A115 Machine Model (MM)
  - JEDEC JESD22-C101 Charged Device Model (CDM)
    - Superseded by JS-002-2014
  - JEDEC JESD78 Latch-up

- ***Automotive Electronics Council (AEC)***
  - AEC-Q100-002 Human Body Model (HBM)
  - AEC-Q100-003 Machine Model (MM)
  - AEC-Q100-011 Charged Device Model (CDM)
  - AEC-Q100-004 Latch-up

Device Level Testing – Questions and Concerns

- With all test methods, there are some issues when trying to replicate a real world event but in a controlled manner!
  - *This is what test methods and testers are trying to do!*
- Although the HBM test method has been around for a long time, there are still questions and concerns about the method and whether it is still a useful test
  - Tester artifacts have been reported over time, which on previous technologies weren't a problem but on new technologies they do have an impact
    - Users should be aware of these and standards highlight them for reference
  - Questions on system interaction with the device under test – do parastics within the tester effect the determination of your device ESD threshold level?
    - Use of a 2pin tester is allowed when results are brought into question
  - Is the device being overstressed due to the number of stress combinations required by the standard?
    - Standard has changed over time to try and address some of these concerns

Device Level Testing – Questions and Concerns

- Although the CDM test method has been in use for a long time, it has now, in some ways become more important than HBM for device qualification
  - This is due to the fact that manufacturing facilities and protection designers know how to protect against HBM, whereas unintended CDM events in manufacturing continue to grow!
  - Another reason is, as device geometries continue to shrink and the desire for performance increases, device ESD protection designers are limited in the amount of real-estate their given for protection!!
- Some of the issues with today's CDM Field Induced test method
  - Air discharge – this causes so many problems during testing, due to it's non-repeatability and reproducibility issues. This is being made even worse by the desire to have lower threshold levels on devices, lower voltage makes the non-repeatability even worse!!
    - The Joint CDM Working Group is developing a Contact CDM method, which is based on a 50 ohm contact method developed by Thermo Fisher
  - Lack of knowledge about CDM events in manufacturing and misconceptions about whether designs need to address the event
    - It's interesting to note, that most device data sheets either don't include CDM levels or even worse don't include HBM levels, so how do you know they're protected????
      - The ESDA is developing a standard practice document which outlines recommendations for data sheet, in regards to the reporting of ESD threshold levels

Device Level Testing – Latch-up Testing

Latch-Up is defined as -

"A low impedance path created within the device by triggering a parasitic SCR"

"Once triggered into conduction an SCR will remain in a conducting state until the current flowing through it falls below the holding value"

Typically when the SCR is triggered, very high currents will flow through the device causing failure

Real world latch-up

JEDEC 78 is the most commonly used test method

- Testing is performed by powering the part, making a pre-IDD measurement and then injecting either a current pulse onto a signal pin or applying an overvoltage on the supply rail in an attempt to trigger a latch-up event. Once the stress is removed, a Post-IDD measurement is made to see if there has been an increase in the current draw

Device Level Testing – Latch-up Testing

- JEDEC 78 is the most commonly used test method
  - Although the JEDEC 78 test method has been in use for a number of years, there are a lot of “holes” in the document, in regards to testing analog devices, how to control devices during testing and a number of other issues
    - To help combat these issues, the JEDEC 78 working group is rewriting the document and hope to have a new version out some time next year
  - In my experience, latch-up testing is possibly the hardest and most time consuming test to perform because it requires detailed knowledge about the device and in many cases, knowledge that only the device designer will have
    - *Most of the application questions I receive, focus around setting up a latch-up test and reviewing the results of the tests!!*

Device Level Testing – Questions and Concerns

- Designing to meet ESD requirements for today's and tomorrow's devices and systems will continue to be an important part of a companies qualification process, to ensure electronics can withstand today's harsh environments!!
- Testing methods continue to evolve, with new methods being introduced meet new threats discovered as new technologies emerge
- We all need to be vigilant in designing, handling and testing products to ensure we can meet the needs of our customers, which in some cases is us ☺

Are there any questions on either the System Level or Device Level ESD testing methods?

If there are any other questions, I can be contacted at tom.meuse@thermofisher.com

I’d like to thank you for your time
and your attention tonight !!