Advanced CMOS Process Integration: looking beyond conventional scaling

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Date: Fri July 2nd, 2010 at 10:00am
Location: Arthur St. John Hill Auditorium, UMaine, Orono

Abstract: For over 40 years industry has been able to deliver performance simply by focusing on the challenges of what has been known as classical scaling, but with non-classical scaling fast approaching advanced development and manufacturing, it has become apparent that one must take a broader view of delivering productivity and performance gains at systems level. While progress in both, Front End of the Line (FEOL) and Back End of the Line (BEOL) will continue to make strides through the innovative use of stress engineering, novel materials such as high k dielectrics and metal gates in the FEOL and low k dielectrics and high conductivity interconnects in the BEOL, there is much more to be gained by addressing the issues of memory integration. The scaling of memory poses a very significant challenge as it is quickly becoming a dominant part of the chip real estate and easily exceeds 70% of the chip area and contributes immensely to processor performance. We will examine the tradeoffs and technological and design advances that have made possible the use of embedded DRAMs to replace large blocks of SRAM memory and are being used extensively in high performance computing. As we continue to push technology to its limits, we are discovering new and innovative solutions to systems performance improvements via 3D integration. This presentation will also discuss some of the integration challenges going from 32nm to 22 nm and beyond.

Bio: Ravi M. Todi received his M.S. degree in Electrical and Mechanical engineering from University of Central Florida in 2004 and 2005 respectively, and his doctoral degree in Electrical Engineering in 2007. His graduate research work was focused on gate stack engineering, with emphasis on binary metal alloys as gate electrode and on high mobility Ge channel devices. His research interest includes semiconductor process integration and device technology for non-conventional CMOS scaling. Since 2007 he is working as Advisory Engineer/Scientist at Semiconductor Research and Development Center at IBM Microelectronics Division focusing on high performance eDRAM integration on 45nm and 22nm SOI logic platforms. Ravi is Editor-in-Chief for IEEE Potentials, an elected member of IEEE-EDS and is an IEEE –EDS Distinguished lecturer.