Designing for Yield in Advanced RFICs - Tools for Success

IEEE NH Section Communications and Signal Processing Chapter &
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Abstract: Companies migrating RFIC designs to advanced technology nodes are facing rising yield concerns due to variability in manufacturing technologies. Shrinking device geometries and increasing device count are leading to chips with high variability from chip to chip and wafer to wafer. Even companies producing small runs of chips in these technologies can face significant yield issues in their designs. It is becoming increasingly important to model and understand the tolerances of these critical circuit components with regard to their processing and manufacturing.

Previously, RFICs have not been good candidates for typical Design for Yield (DFY) techniques such as Monte Carlo statistical analysis because of their complexity and the simulation time that was involved. Often these types of simulations were run at the very end of a design cycle, just before tapeout, with little influence on the design process and no possibility of using the data to improve the robustness of the design. Simplified UcornerV cases were used to validate the tolerances of the design. The result was under characterized designs that may have yielded acceptably in more stable CMOS processes, but which cannot achieve the same yield goals in advanced technologies.

Modern RFIC designers can find a full suite of DFY tools in the GoldenGate simulator. Agilent's high speed, high capacity harmonic balance simulation engine can be used to bring Monte Carlo analyses back into the design cycle, enabling designers at all levels of RFIC integration to start characterizing the process sensitivity of their designs. Variations of critical metrics such as IP3, P1dB, and phase noise can all be examined using the existing GoldenGate simulation tools. For larger, more complex designs, GoldenGate enables design teams to take advantage of parallel computing, shifting the simulation burden from designer resources to computing resources. GoldenGate also offers advanced DFY tools that enable users to manage these parallel simulations, view statistical data in real-time, and quickly learn the boundaries of performance variations in a specific technology. Designers can also take specific outlier cases and re-run them in any of the GoldenGate simulation engines to verify problems and redesign sensitive networks.

Join us as we present a fully detailed RF DFY flow using Agilent's GoldenGate simulator and prepare your design teams for the migration to advanced CMOS.

Biography: Jian Yang currently holds the position EEsof Applications Manager at Agilent Technologies. From 1980 to 1989, he earned his BS and MS degrees from Nanjing University of Science and Technology, and PhD degree from University of Electronics Science and Technology, all in Electrical Engineering. In 1990, he came to the University of Waterloo in Canada as a Visiting Research Assistant Professor. In 1992, he joined EEsof Inc as an R&D engineer in Westlake Village, California. Since Hewlett Packard acquired EEsof Inc in 1993, Jian has held positions of R&D engineer, R&D operating manager and EEsof Application Manager, all within the Agilent EEsof organization. Jian's interests are in high frequency electronic design automation.

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