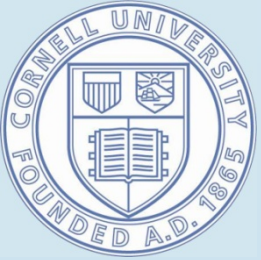

A New Frontier: CMOS Terahertz Signal Generation and Amplification

Ehsan Afshari

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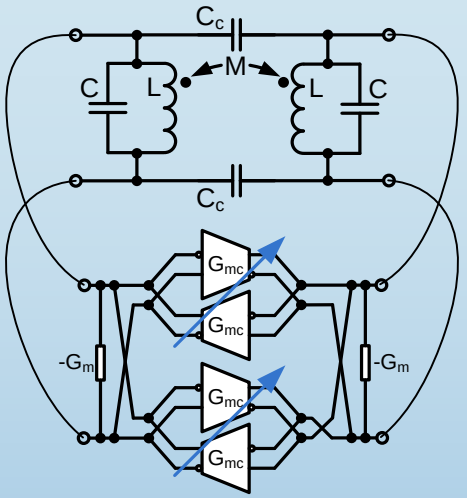
Acknowledgement

- The people who actually make it happen!
- Funding Agencies: ONR, DARPA, FCRP, and NSF.

Other Projects



- Low phase noise oscillators:
  - Dual mode,
  - Quadrature.
- Wideband low phase noise VCO:
  - 2.6GHz – 5.8GHz that satisfies ALL cellular specifications
- Low power, high speed ADC
  - 8GS/sec, 4b with 32mW
  - 1.2GS/sec, 4b with 2mW
- Gain close to f_{max} of transistor
  - A 107 GHz amplifier on standard 130nm CMOS

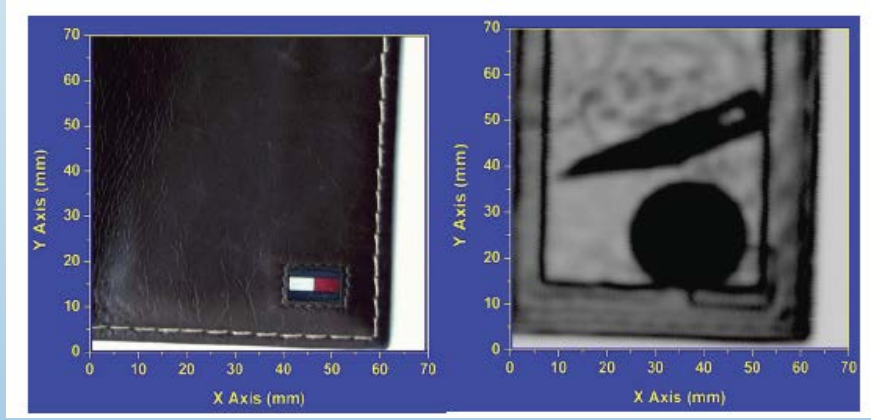
Process	65nm Low Power CMOS					
Vdd (V)	VCO Core: 0.6 V; Digital Control: 1.2V					
Tuning Range	2.48GHz~5.62GHz continuous tuning					
Chip Area	0.294 mm^2					
Phase Noise	Odd Mode			Even Mode		
(dBc/Hz)	Low	Middle	High	Low	Middle	High
Freq (GHz)	2.517	3.696	3.880	3.312	4.463	5.515
Idc (mA)	23.61	17.43	16.49	25.27	20.97	16.43
PN@100kHz	-101.1	-96.44	-94.42	-105.3	-96.03	-89.3
PN@300kHz	-114.4	-112.7	-112.3	-117.5	-110.3	-105.1
PN@1MHz	-128.6	-128.3	-128.3	-129.5	-124.8	-121.3
PN@3MHz	-139.8	-137.1	-137.2	-139.5	-134.6	-130.7
PN@10MHz	-151.9	-151.4	-151.9	-150.2	-147.6	-145.8
PN@20MHz	-156.8	-156.6	-156.7	-155.5	-153.1	-151.7
FoM@10MHz	189.4	192.5	193.7	188.8	189.6	190.7

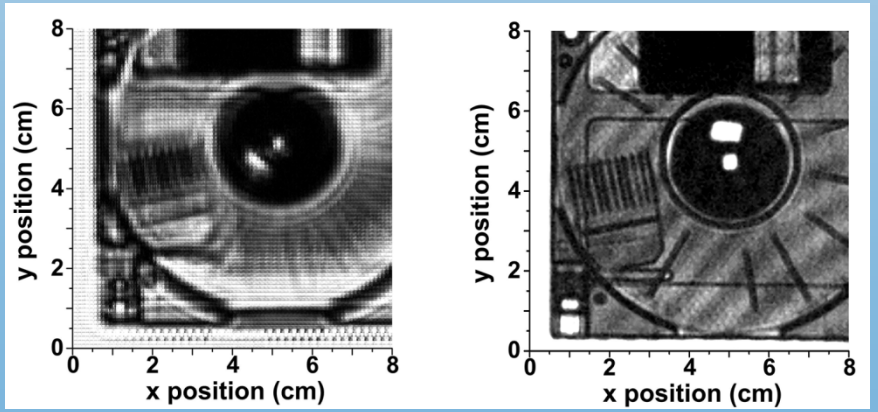
Outline

- Motivation
- THz Signal Generation
  - High Power CMOS Source
  - A Tunable CMOS Source
  - CMOS Frequency Multipliers
  - GaN Implementations
  - Sharp Pulse Generation in CMOS
- THz Signal Amplification
  - Around 300GHz
  - 500GHz and Above
- THz Spectroscopy in CMOS
- THz Imaging Systems

Application of THz Systems

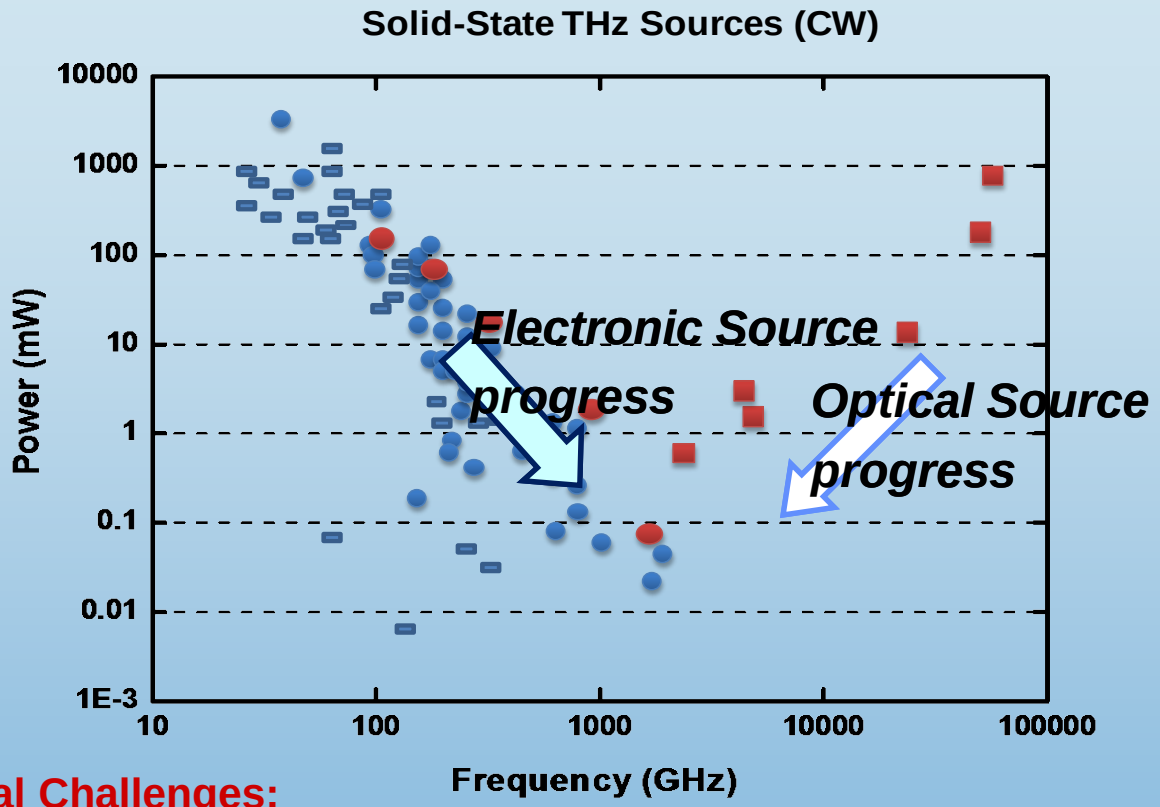
- Imaging (e.g., detection of concealed weapon, cancer diagnosis, and semiconductor wafer inspection)
- Compact range radars
- High data rate communication (e.g.,100 Gbps)





High power is needed for these applications

Challenge



Fundamental Challenges:

- Transistors offer no power gain above f_{max}
- Limited power efficiency of devices
- Limited break down voltage
- Quality factor of passives is low

High power signal generation is the main challenge in realizing CMOS THz systems.

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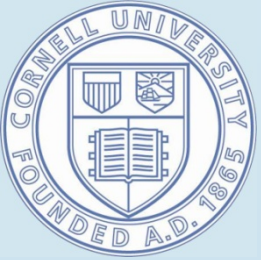
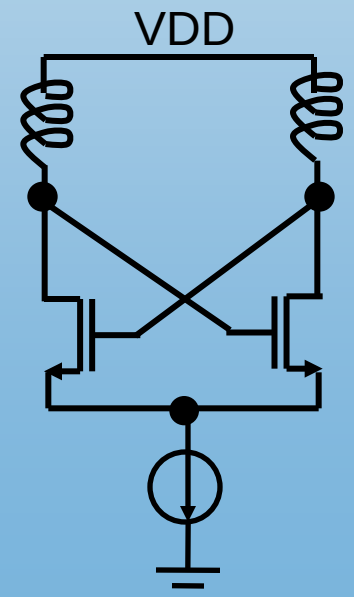


Fundamental Limit?

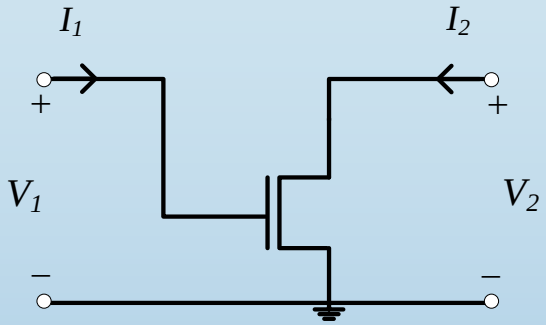
- Most of the fundamental oscillators have the oscillation frequency in the order of the half of the f_{max} of the transistors. Why not higher?
- What is the maximum oscillation frequency of a circuit topology, considering the quality factor of the passive components?
- For a fixed frequency, what is the topology that results in maximum output power?

Fundamental Limit

- Example: IBM 130 nm CMOS process:
  - f_{max}: simulated: 174 GHz
  - f_{max}: measured: ~135 GHz
- Regular Cross-Coupled oscillator:
  - Maximum achievable frequency (simulation): 120 GHz
  - This is with IDEAL inductors!



Activity Condition (II)



$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [Y] \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

- Normalized real power flowing out of the device:

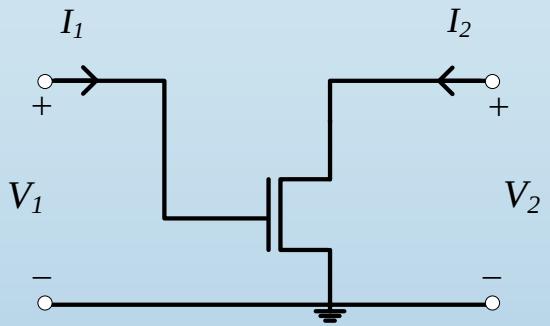
$$\Rightarrow G_m = \frac{P_R}{|V_1||V_2|} = -(A^{-1}G_{11} + AG_{22}) - \left|Y_{12} + Y_{21}^*\right| \cos(\angle(Y_{12} + Y_{21}^*) + \varphi)$$

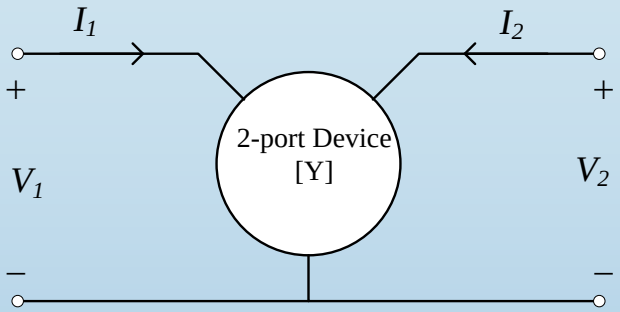
$$G_{11} = real\ (Y_{11})$$
$$G_{22} = real\ (Y_{22})$$

$$A = \left|\frac{V_2}{V_1}\right| \ \& \ \varphi = \angle(\frac{V_2}{V_1})$$

- G_m is the maximum conductance that can be placed across the transistor and maintain the oscillation.

Activity Condition (III)





$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [Y] \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

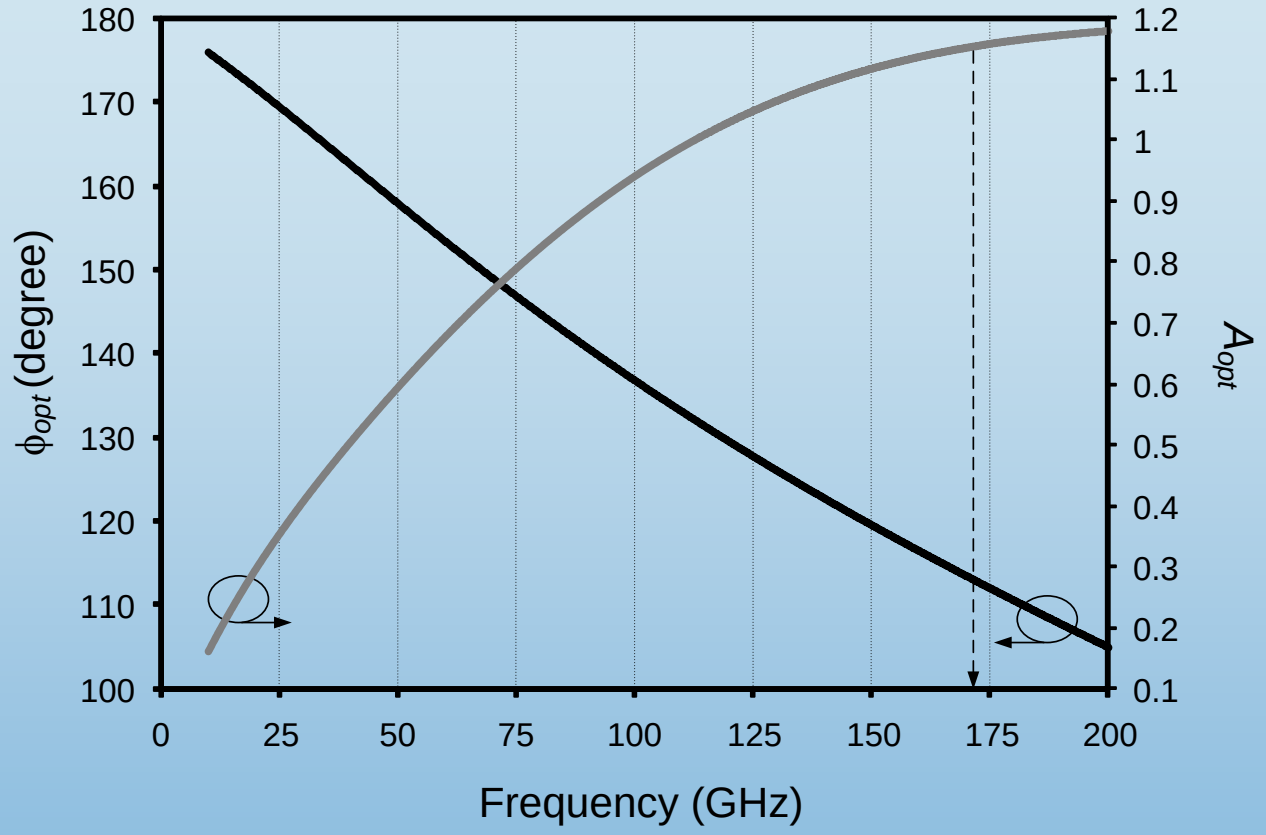
Activity Condition: $\max\left(\frac{P_R}{|V_1||V_2|}\right) = -2\sqrt{G_{11}G_{22}} + |Y_{12} + Y_{21}^*| > 0$

@ f_{max}

$$\max\left(\frac{P_R}{|V_1||V_2|}\right) = 0$$

To achieve f_{max}, A_{opt} and φ_{opt} should be satisfied for the device.

Maximum Activity



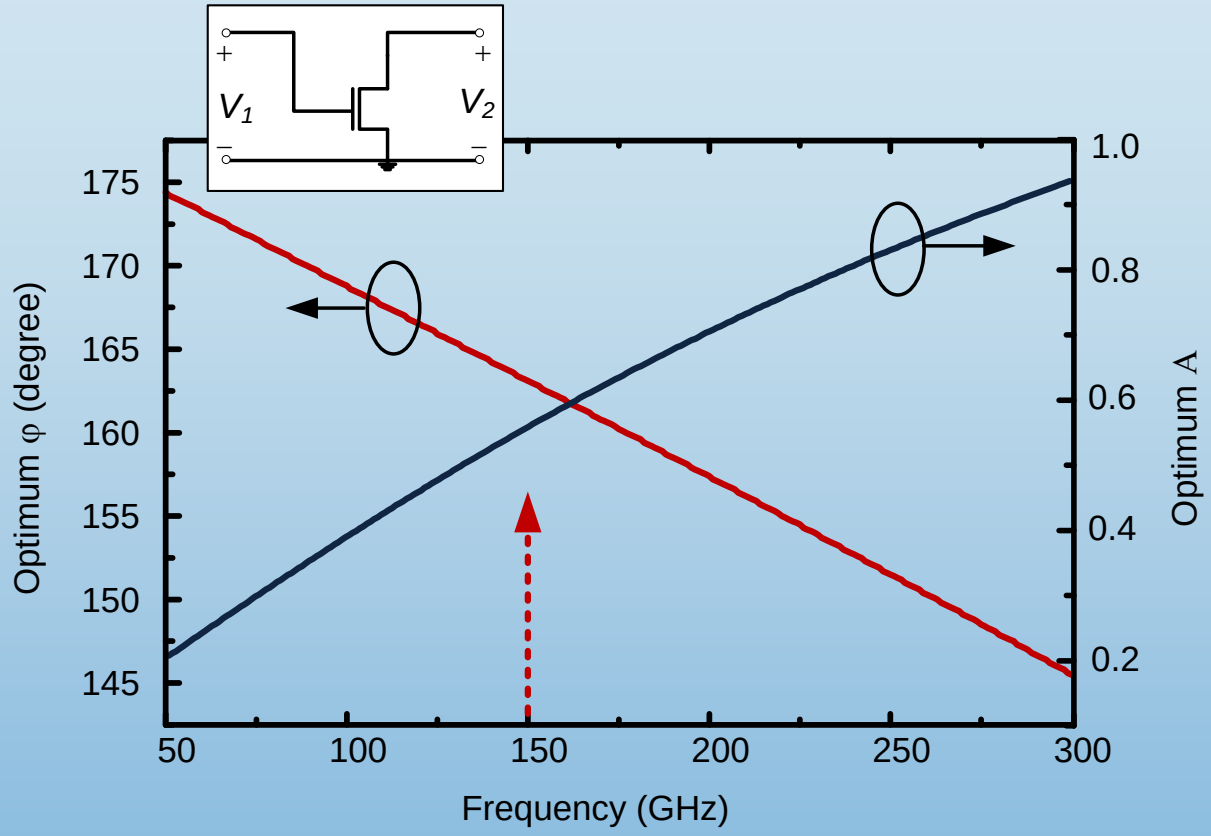
- Optimum gain and phase conditions for maximum generated power (maximum oscillation frequency)

$$\varphi = \varphi_{opt} = (2k+1)\pi - \angle(Y_{12} + Y_{21}^{*}) \qquad A = A_{opt} = \sqrt{\frac{G_{11}}{G_{22}}}$$

Higher Frequency: Harmonics

- In order to achieve higher frequencies, we need to generate strong harmonics
- This means we should maximize the swing at the fundamental frequency
- It might be better to back off from the maximum possible oscillation frequency to boost the harmonic generation
- We need to maximize "G_m"

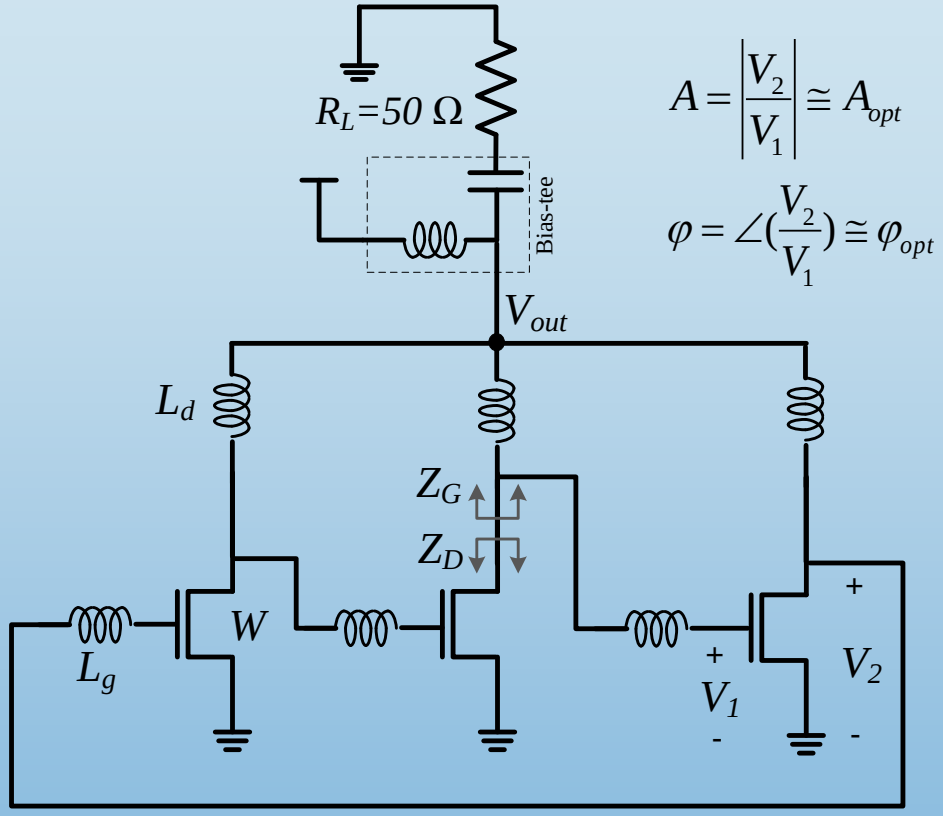
Optimum Conditions



- Optimum phase and voltage conditions in a 65nm process
- Target frequency is 450 GHz

Triple Push Oscillator

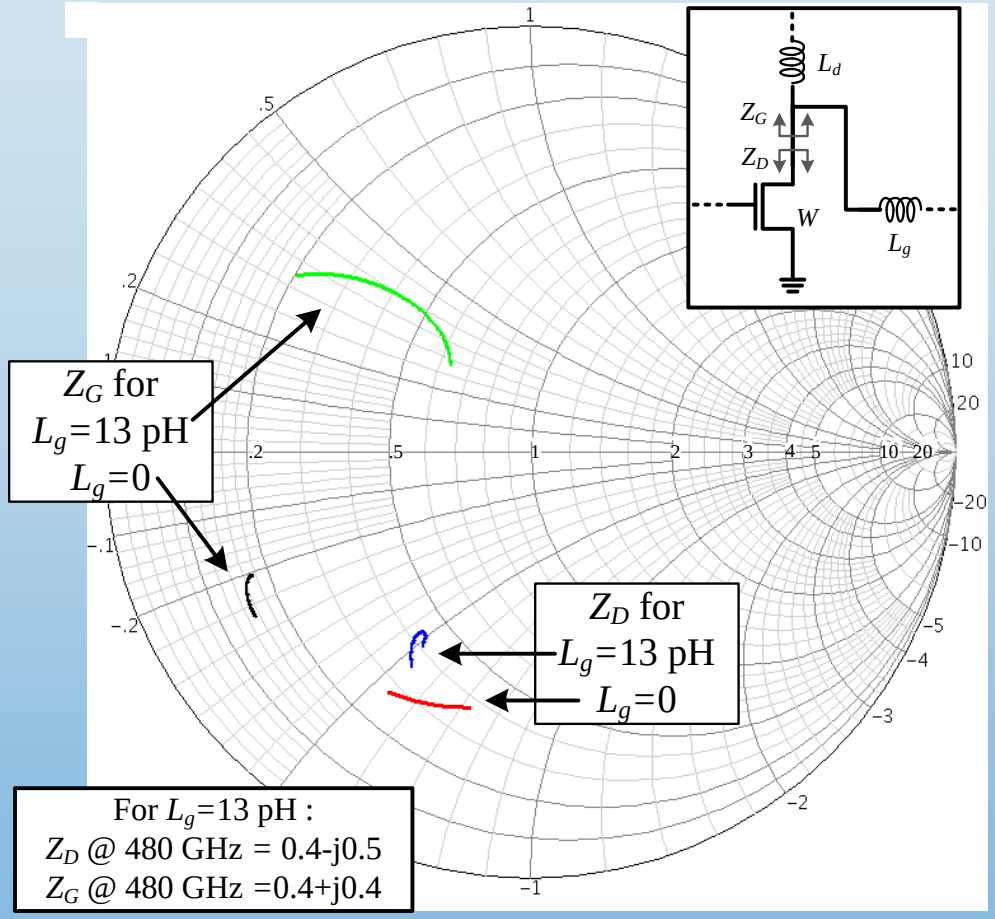
- The gate inductor helps with both amplitude and phase conditions:
  - It resonates with C_{gs} to boost the gate-source voltage, resulting in lower *A* across the device
  - It also delays the voltage to increase the phase shift from 120.



$$A = \left|\frac{V_2}{V_1}\right| \cong A_{opt}$$

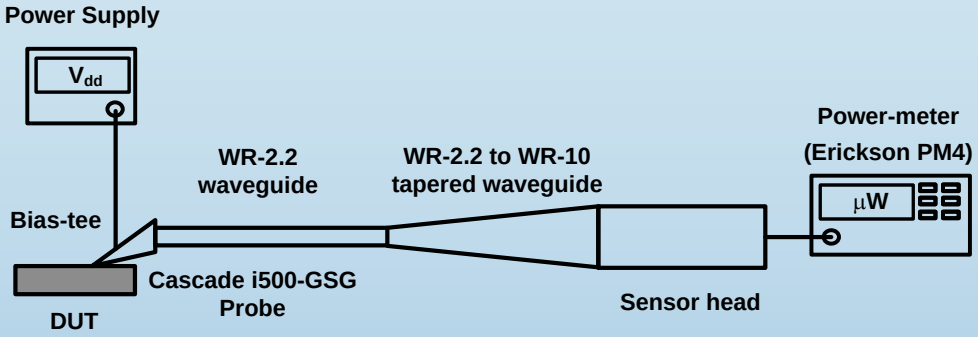
$$\varphi = \angle\left(\frac{V_2}{V_1}\right) \cong \varphi_{opt}$$

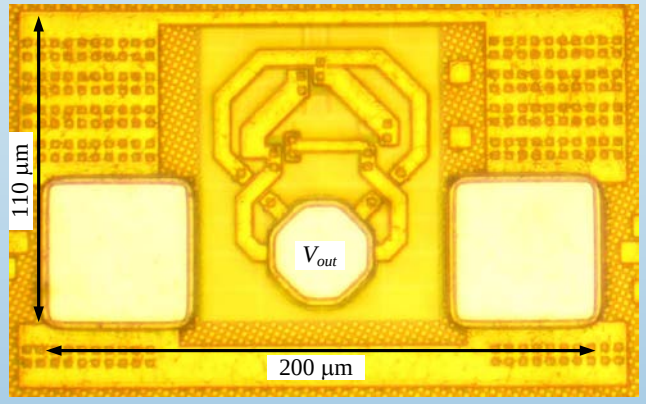
The Effect of L_g on Matching

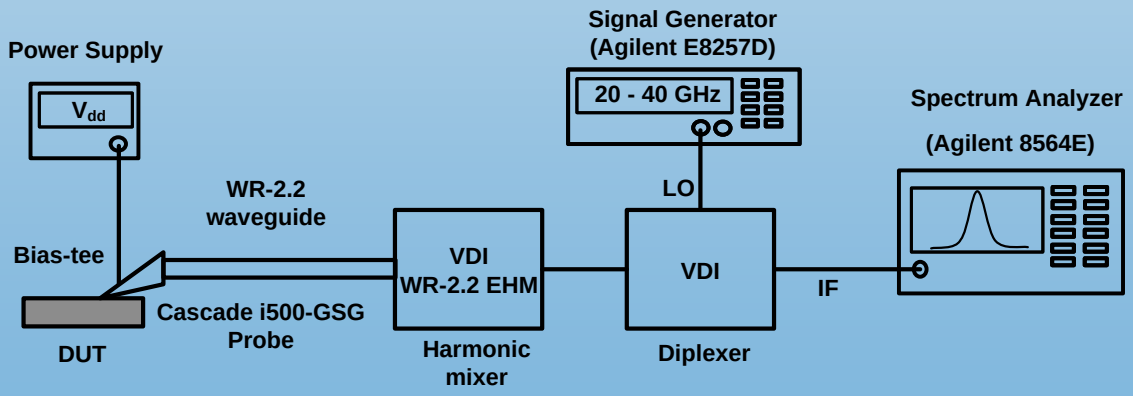


- The gate inductance also helps with matching for the 3rd harmonic.

Implementation

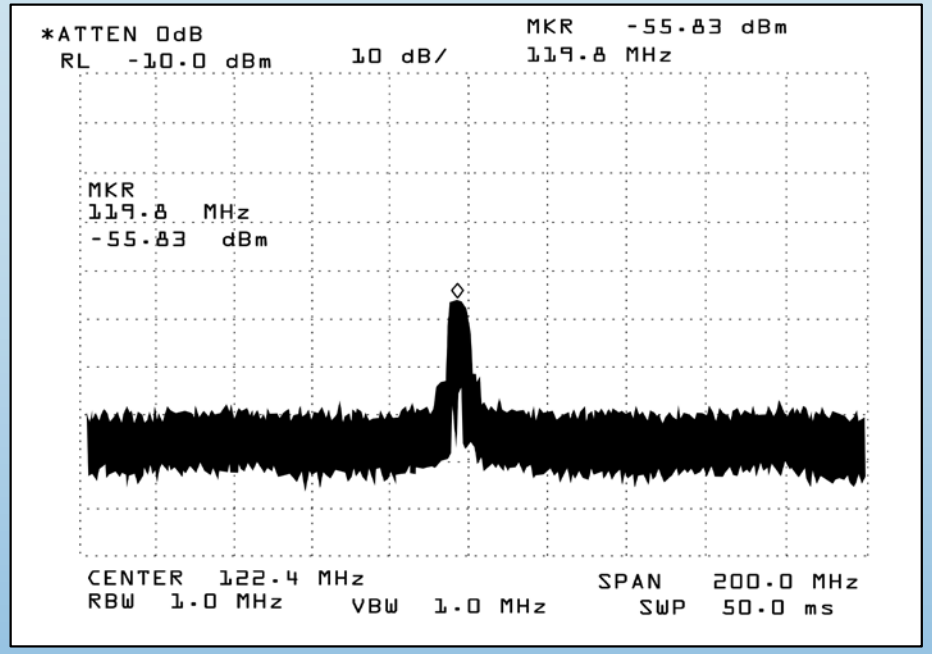


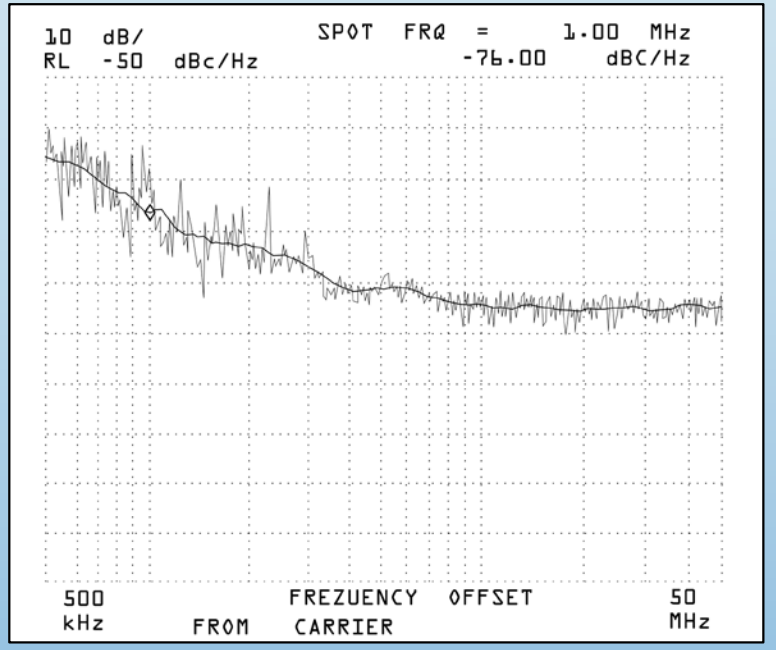




- The power and frequency test setups

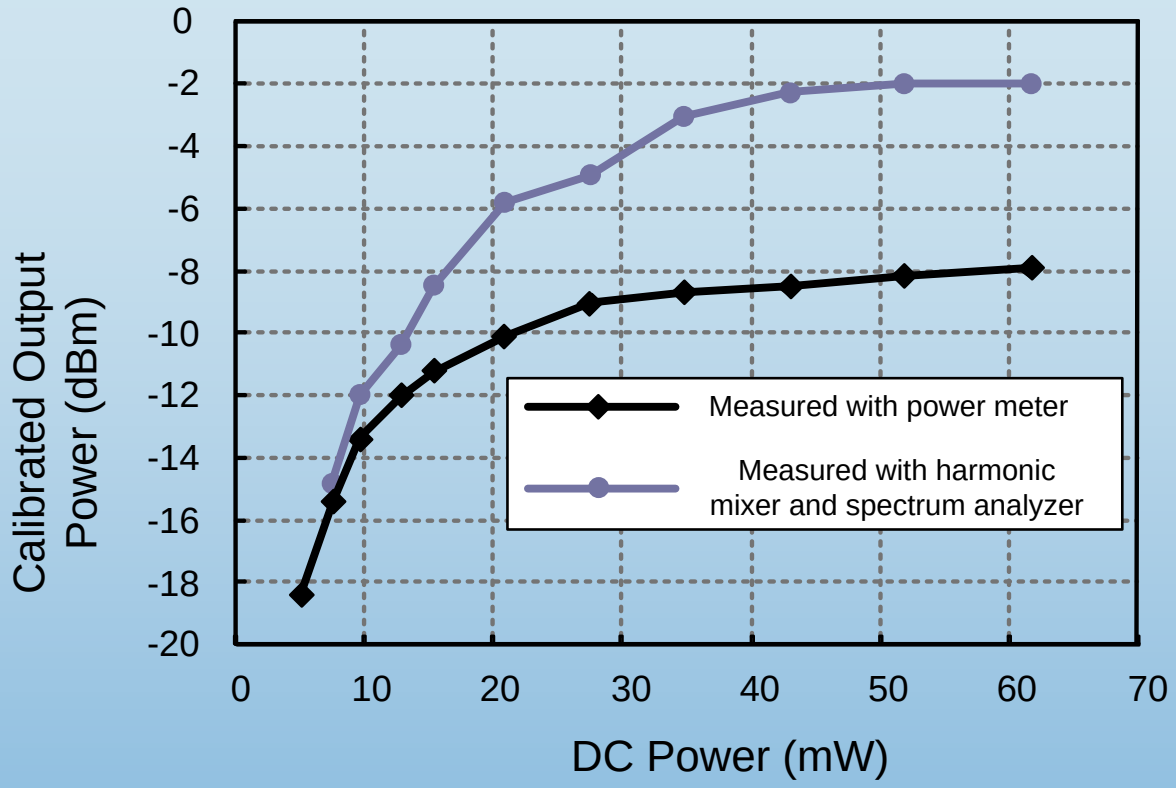
Results: Spectrum





- The second harmonic is 15.5dB lower than the third harmonic
- Output frequency is 482GHz

Results: Power



- Measured output power using both setups

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Challenge: Terahertz VCO

- At mm-wave and terahertz frequencies it is challenging to get high tunability with varactors due to dominance of device parasitics
- Varactors are very lossy at mm-wave and are not desirable in mm-wave and terahertz signal generation

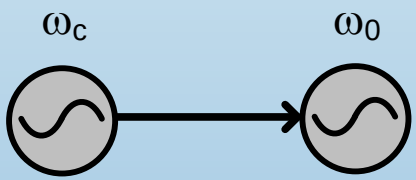
Ref.	Technology	Fundamental (GHz)	Output frequency (GHz)	Power (dBm)	Tunability
JSSC '06	130nm CMOS	102GHz	102 GHz	-25 dBm	0.2%
ISSCC 09	32nm CMOS SOI	102GHz	102GHz	N/A	4.2%
ISSCC `08	45nm CMOS	205GHz	410GHz	-47 dBm	-
ISSCC '11	45nm CMOS	150GHz	300GHz	-19 dBm	-
JSSC '11	65nm CMOS	160GHz	480GHz	-8 dBm	-

A Simple Case: IL

- In an electrical oscillator with locking assumption Alder derives Ω that results in

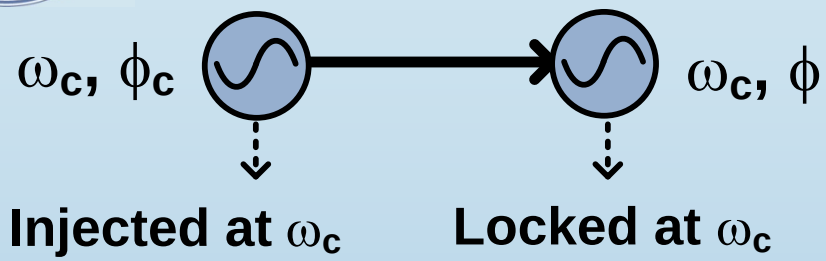
$$\frac{d\phi}{dt} = \omega_0 + K sin(\phi - \phi_c)$$

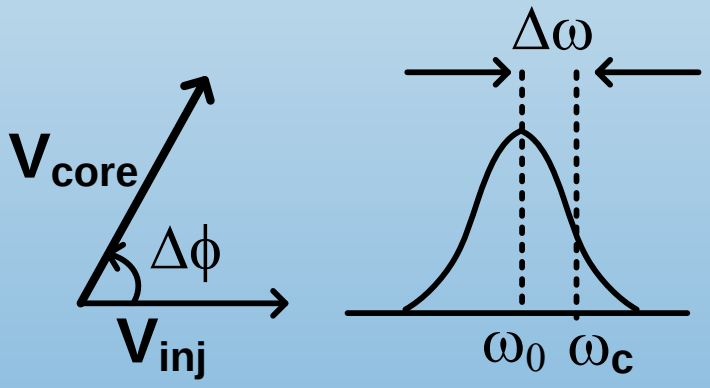
$$|K| = \frac{E_c}{E}\frac{\omega_0}{2Q}$$



- The above equations hold valid only if $\Delta\omega < K$
- There has been a considerable body of study on coupled oscillators ever since.
- This coupling mechanism has remained as a valid first order approximation.

Observation: Frequency Control



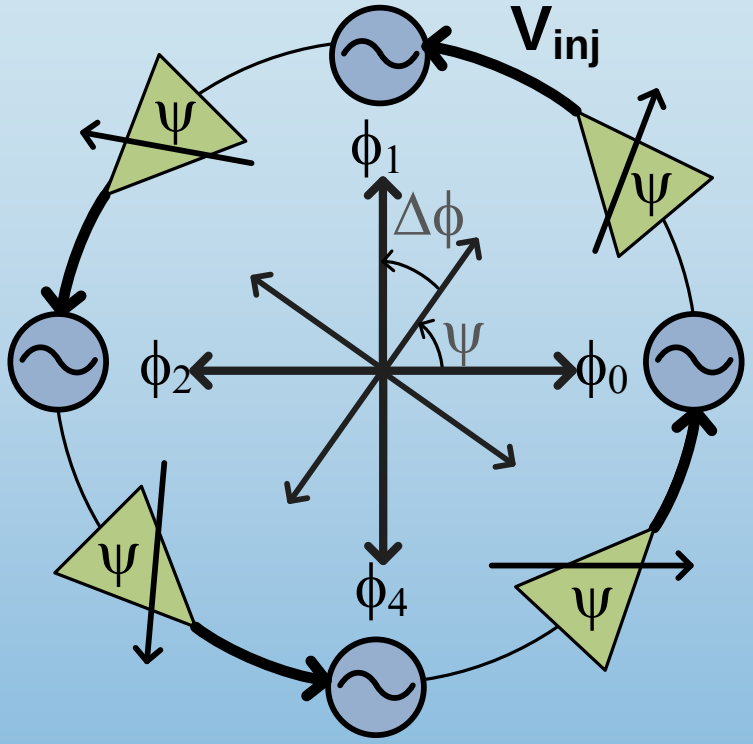


$$\Delta\phi = \phi - \phi_c$$

$$\mathrm{Sin}(\Delta\varphi) = 2Q\frac{V_{core}}{V_{inj}}\cdot\frac{\Delta\omega}{\omega_0}$$

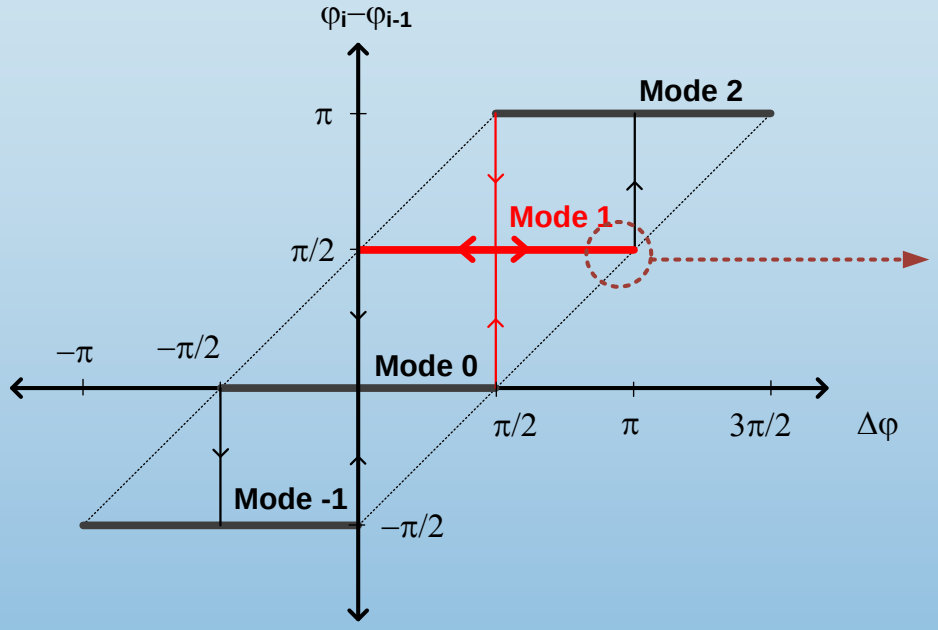
- In injection locking frequency is dictated by the external source and the phase shift is a consequence
- In a VCO we would like to dictate the phase shift and as a result tune the frequency

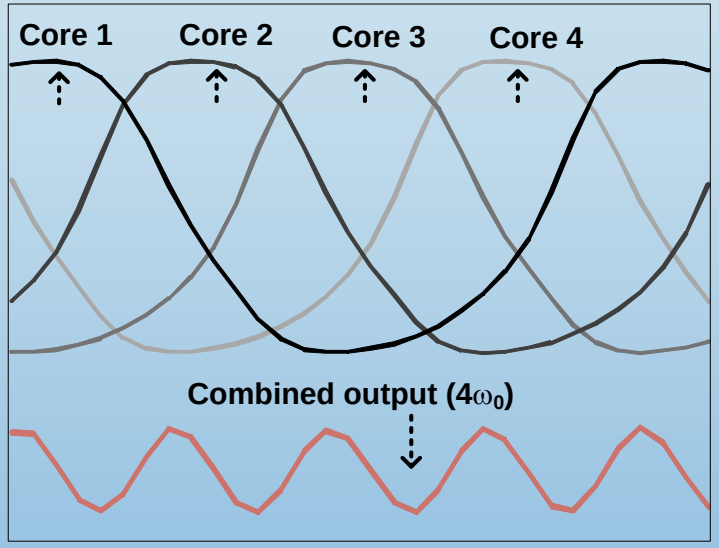
Ring of Coupled Oscillators



Frequency is tuned by changing the phase shift of the coupling block

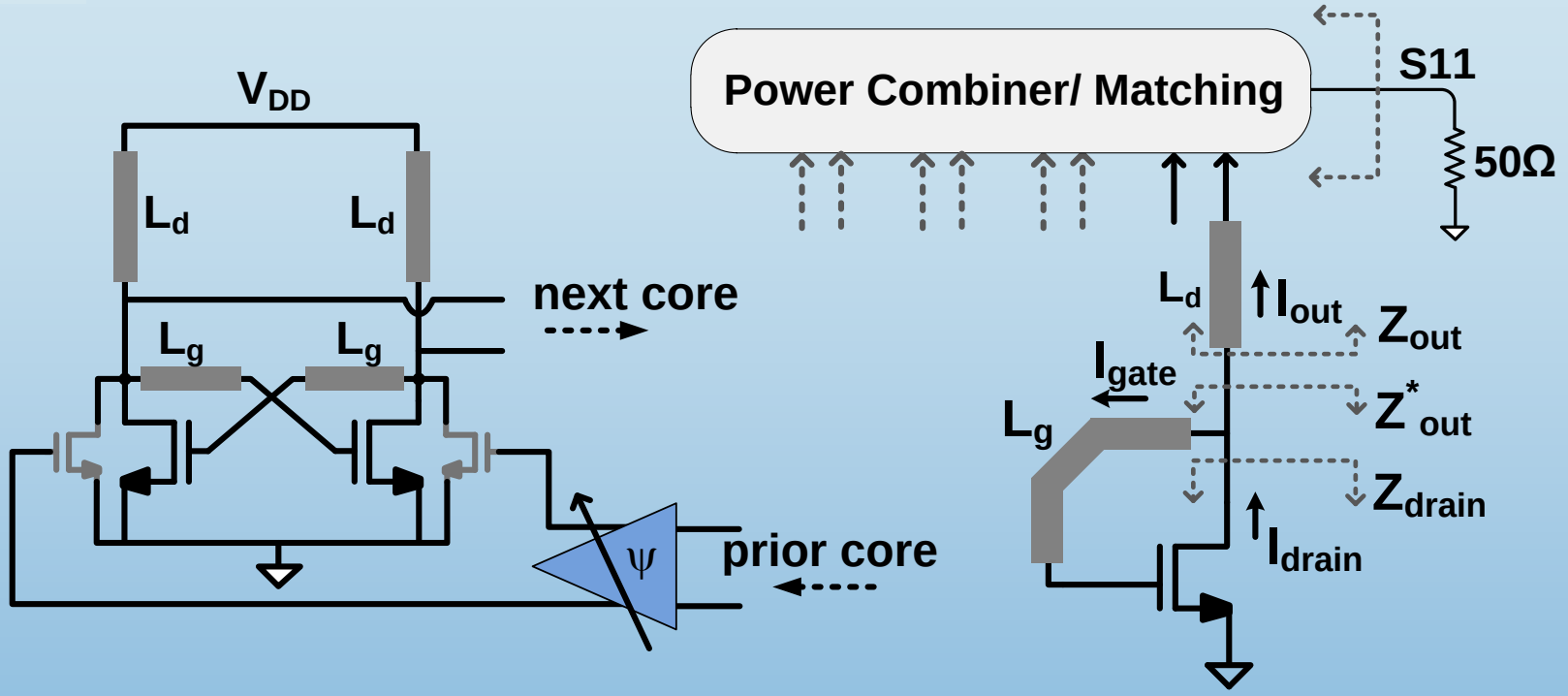
Ring of Coupled Oscillators





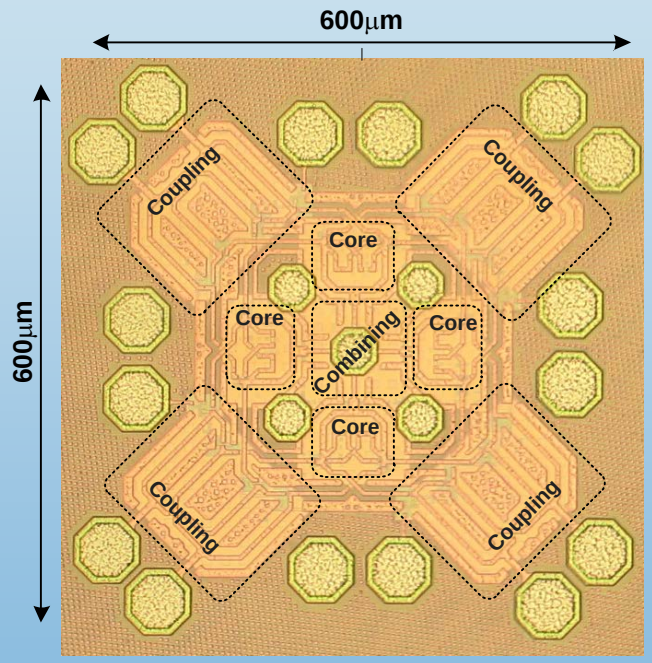
By selecting the coupling mode, we can combine the desired harmonic

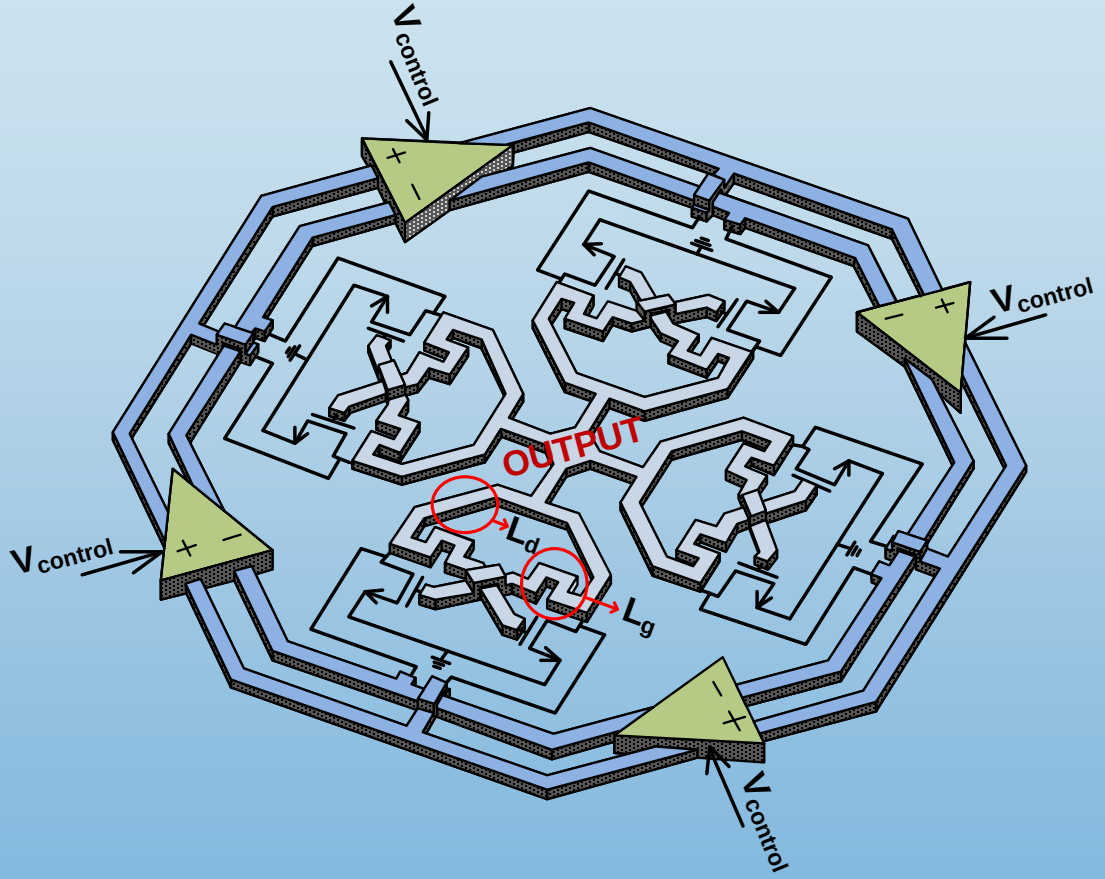
Application: Harmonic THz VCO



- Each core oscillator is optimized to generate maximum power

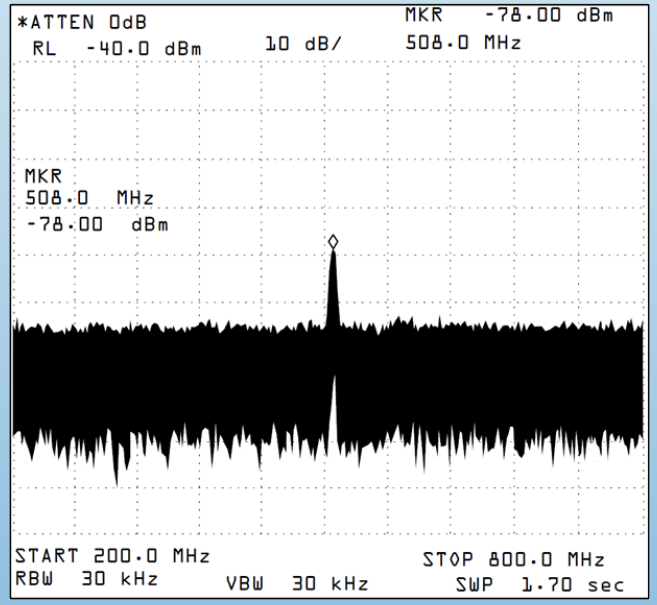
Layout

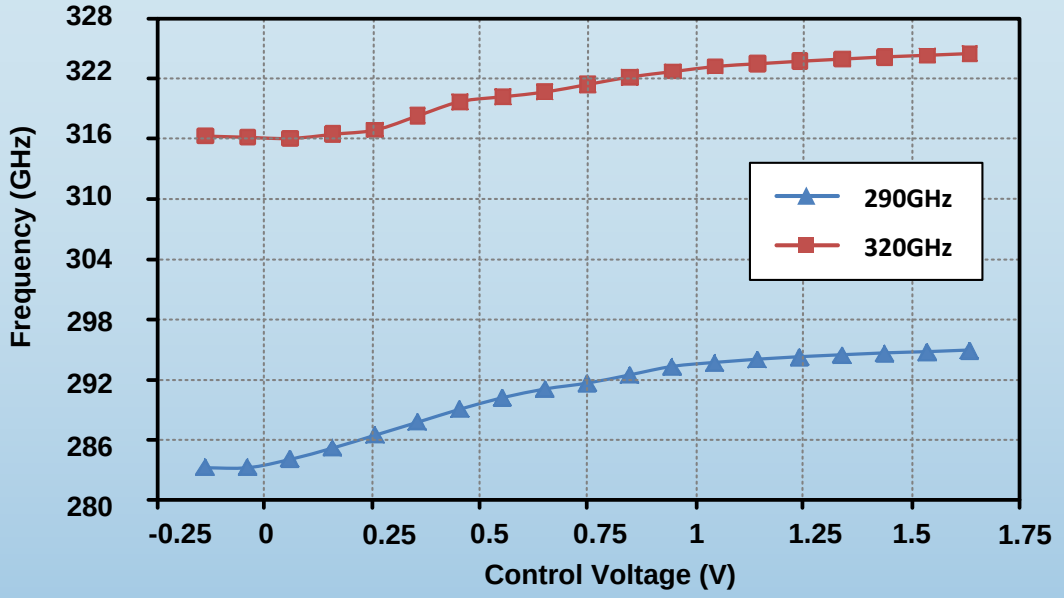


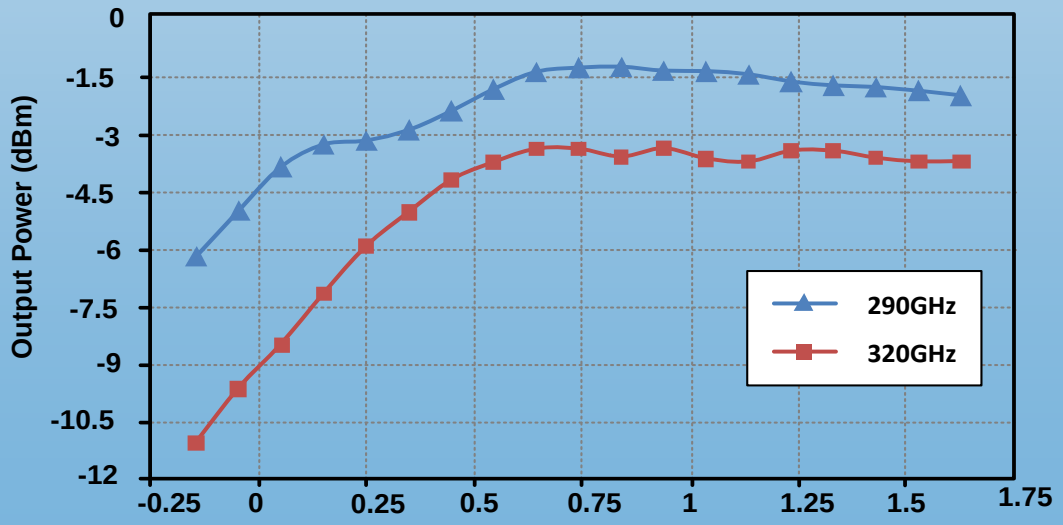


- The chip layout in the employed 65nm CMOS process.

Measurement Results

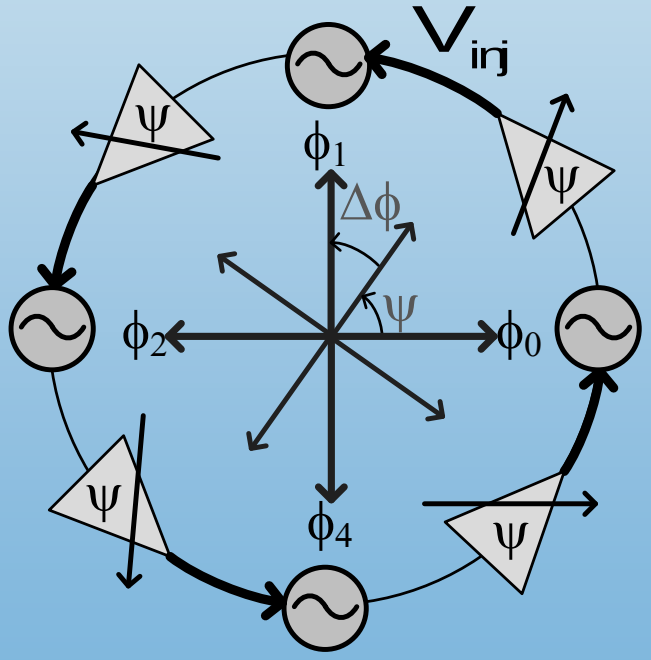


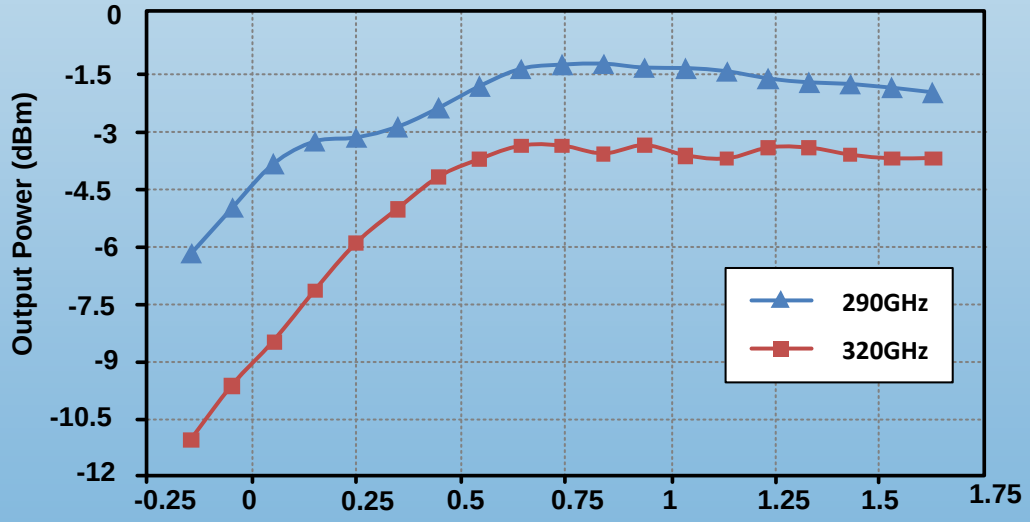




Output power

- The varactor-less core is optimized for maximum harmonic generation and power delivery to the output.

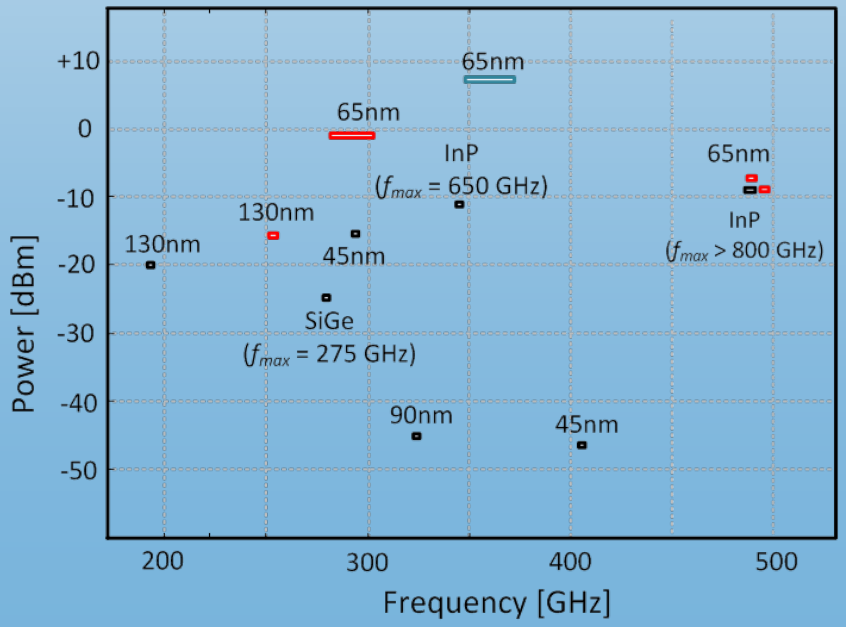


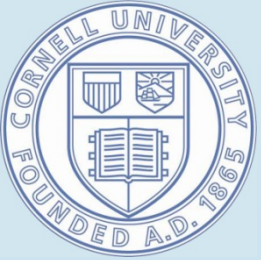


State-of-the-Art Sources

Ref.	This work	This work	[1]	[5]	[6]	[4]	[2]*
Frequency (GHz)	290	320	482	324	291	296	325
Output Power (dBm)	-1.2	-3.3	-7.9	-46	-10.9 (radiated, 4 elements)	-3.9	-3
Tuning Range	4.5%	2.6%	Non-tunable	1.2%	Non-tunable	4%	6.2%
Phase Noise (dBc/Hz)	NA	-78 @ 1 MHz	-76 @ 1 MHz	-78 @ 1MHz	NA	-78 @ 1MHz	NA
DC Power (mW)	325	339	61	12	74	115	420
Technology	65 nm Bulk CMOS	65 nm Bulk CMOS	65nm Bulk CMOS	90nm Bulk CMOS	45nm SOI CMOS	InP HBT (f_{max}>800 GHz)	130nm SiGe HBT
Area (mm^2)	0.36	0.36	0.02	0.03	0.64	0.41	0.51

* [2] is a frequency multiplier, not an oscillator. We added this work to the table to compare with a frequency multiplier at a similar frequency.





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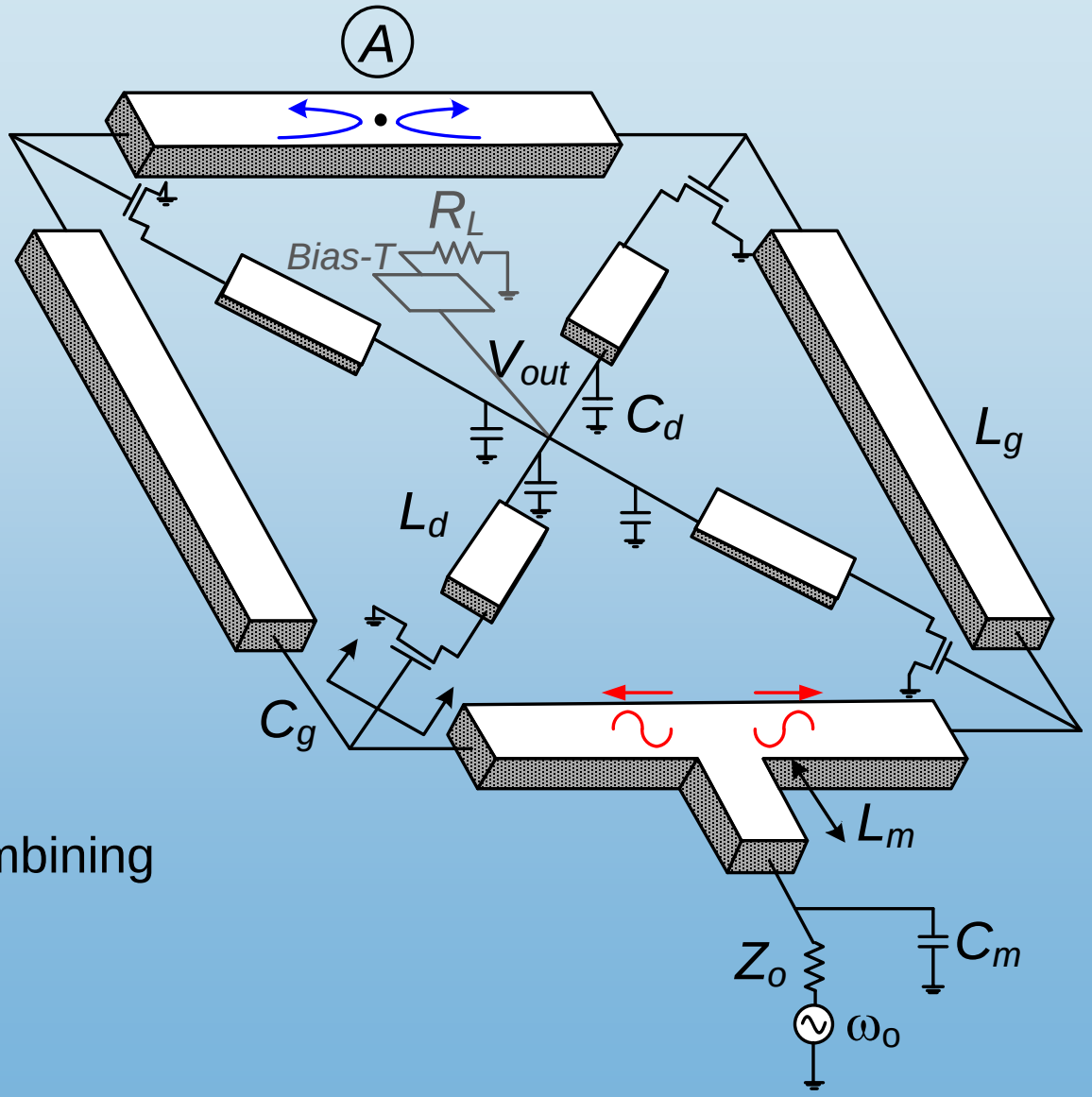
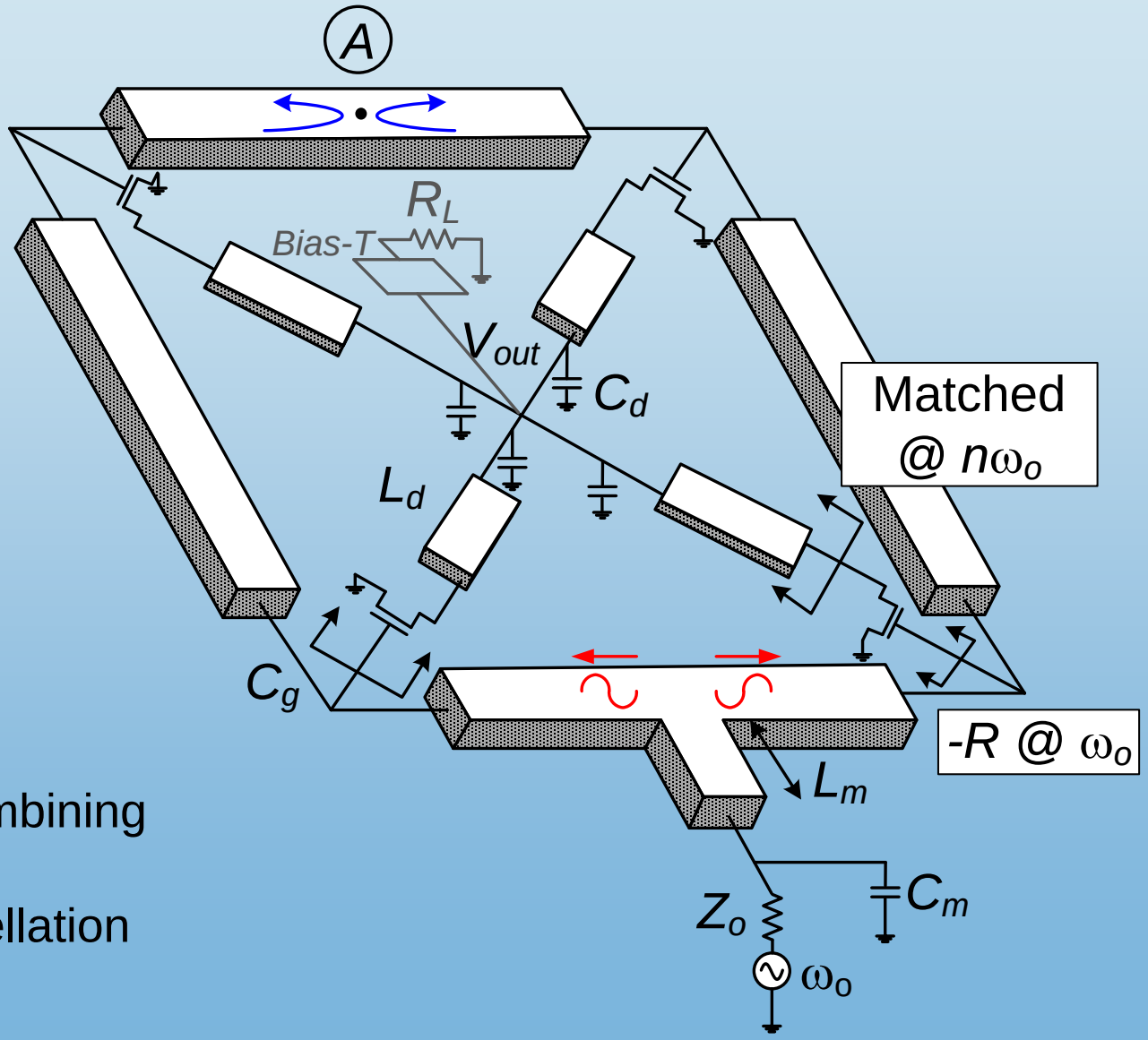
Basic Idea



- Effective harmonic generation and combining

Basic Idea

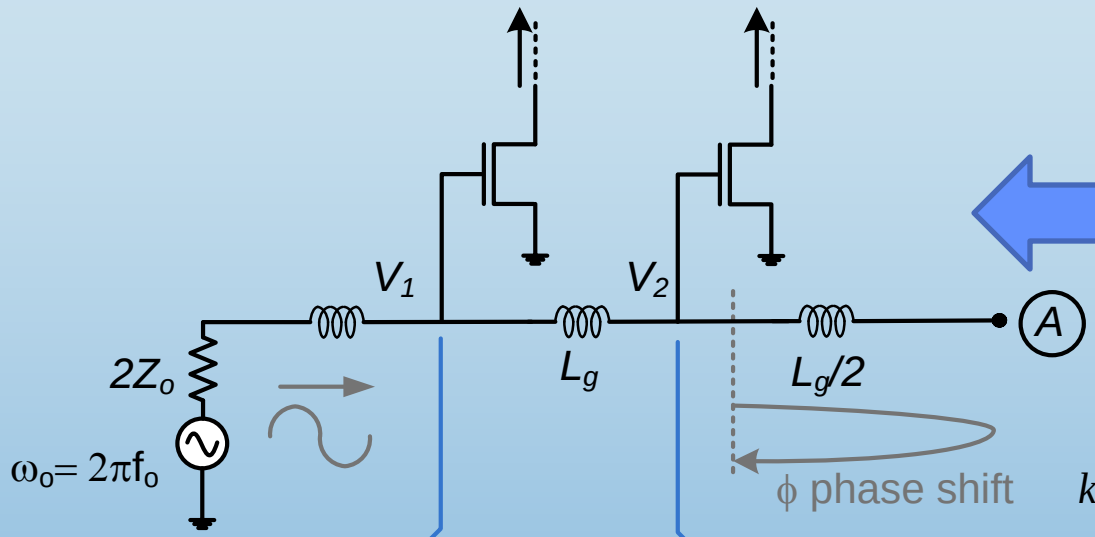


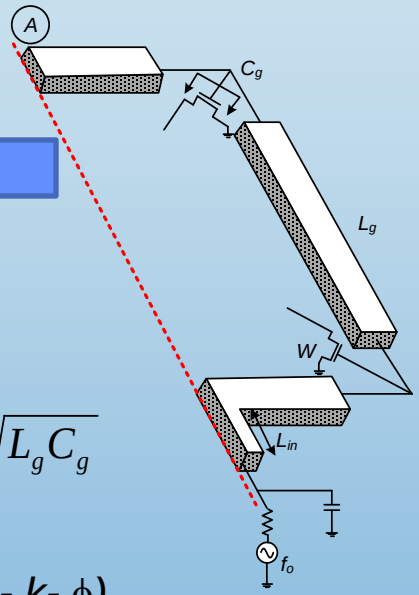
- Effective harmonic generation and combining
- Efficient loss cancellation

Theory

$I_1 = a_1 V_1 + a_2 V_2^2 = \ldots + a_2 \cos(2\omega_o t - 2k - \phi) + \ldots$

$I_2 = a_1 V_2 + a_2 V_2^2 = \ldots + a_2 \cos(2\omega_o t - 2k - \phi) + \ldots$



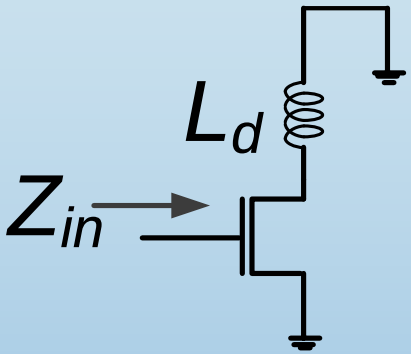


$V_1 = \underbrace{\cos(\omega_o t)}_{\text{incident}} + \underbrace{\cos(\omega_o t - k - \phi - k)}_{\text{reflected}}$

$V_2 = \underbrace{\cos(\omega_o t - k)}_{\text{incident}} + \underbrace{\cos(\omega_o t - k - \phi)}_{\text{reflected}}$

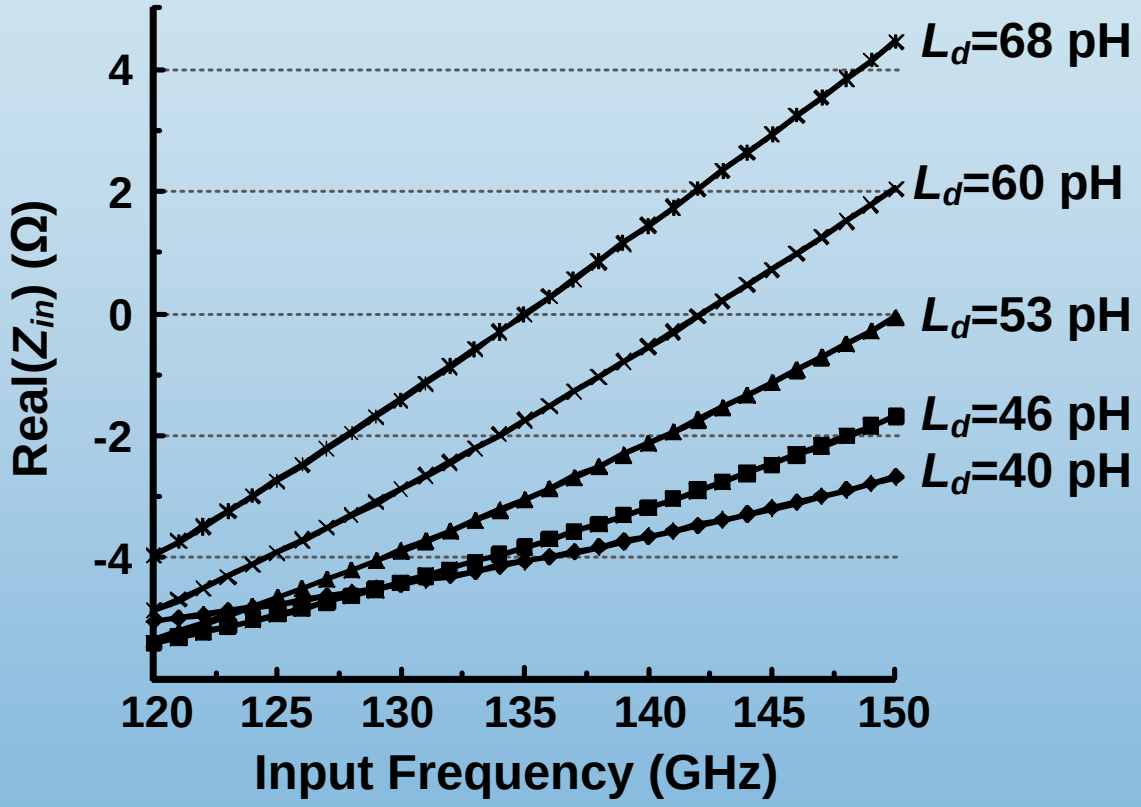
- The second harmonics add in phase at the output
- The basic principle is independent of frequency

Negative Input Impedance



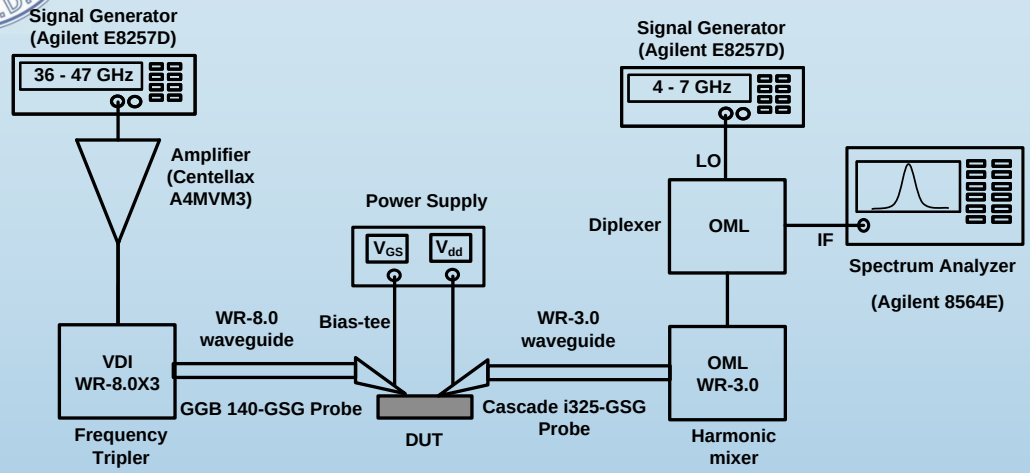
$$L_d\omega_\circ^2\left(C_{gd}+C_{ds}+\frac{C_{gd}}{R_\circ g_m}\right)<1$$

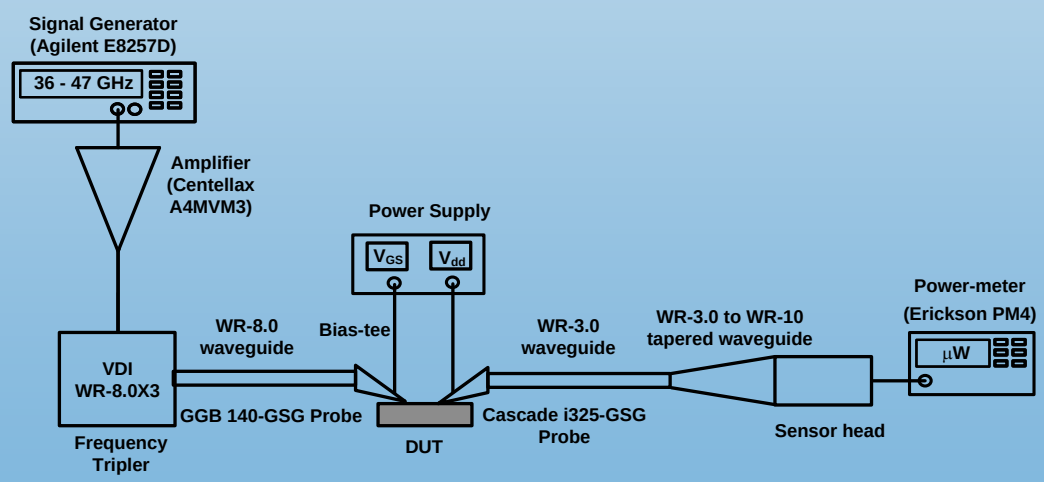
$$\Rightarrow \quad Real(Z_{in}) < 0$$

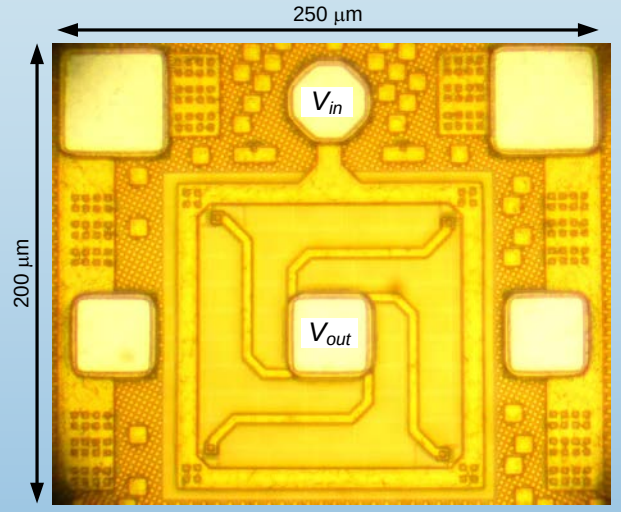


- There is a trade-off between better output matching and higher input voltage swing.

Implementation

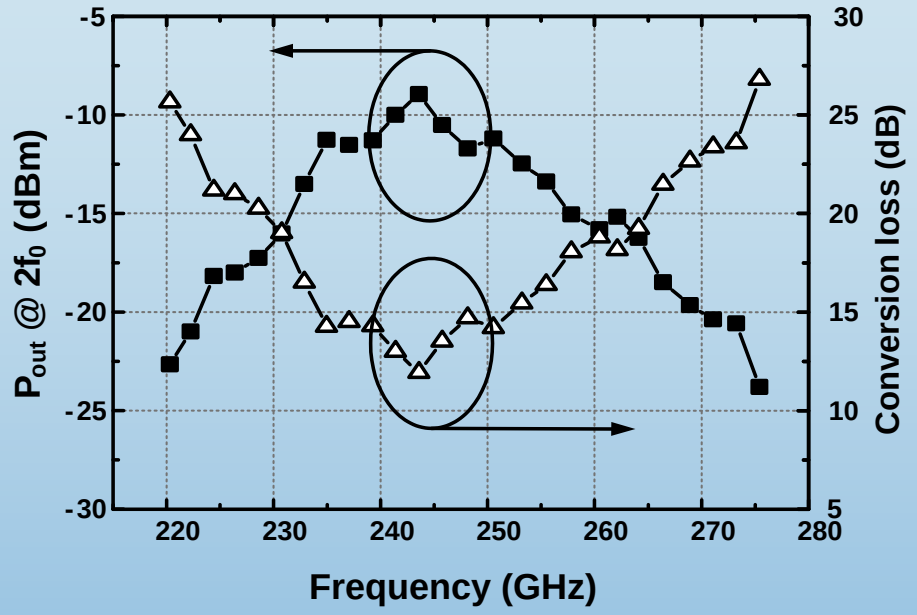


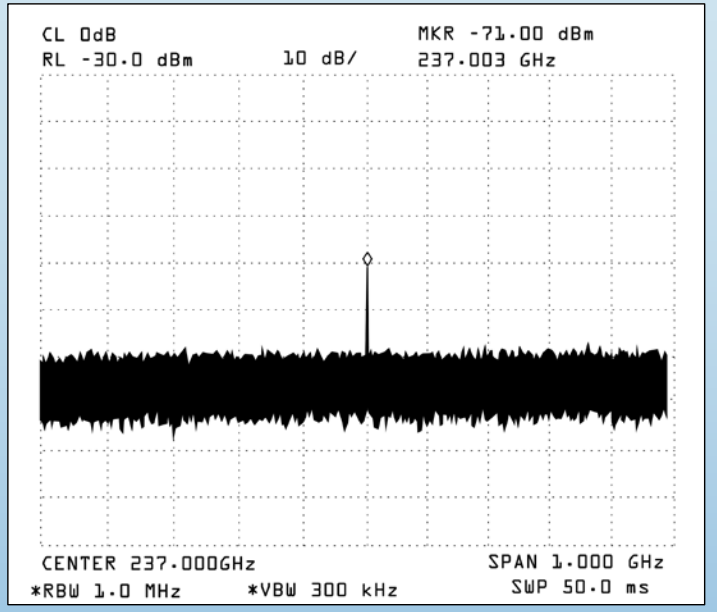




- The power and frequency test setups

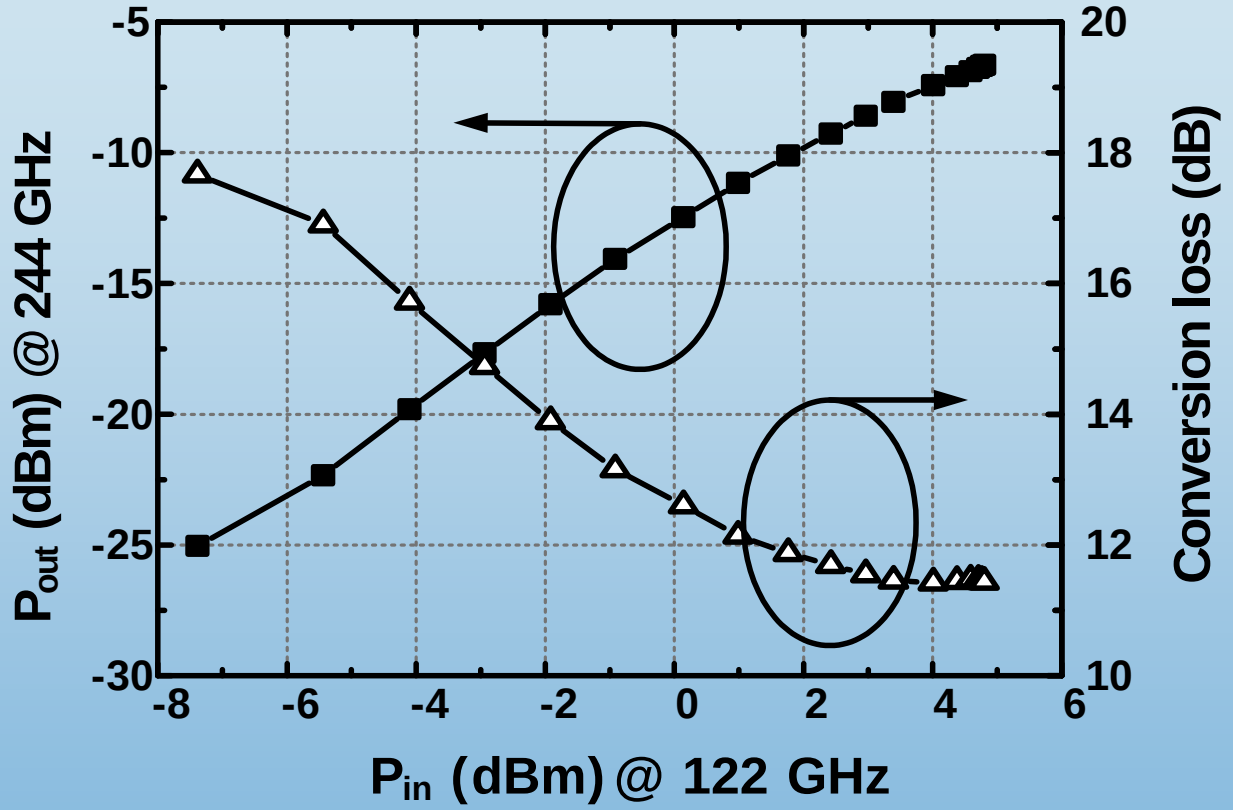
Results





- In this case the input power is kept at 3dBm

Results



- The output power is not saturated
- A maximum of -6.6dBm is achieved at 244GHz

Comparison

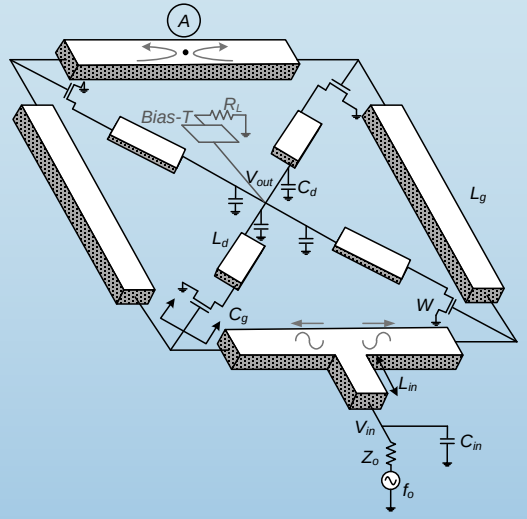
Ref.	This work	[2]	[3]	[4]	[5]	[6]*
Frequency (GHz)	244	115	125	180	300	324
Tuning Range	22.2%	13.1%	12.7%	23.5%	21.4%	1.2%
Power (dBm)	-6.6 / 0	-2.6	-1.5	0	-6.4	-46
Power Measurement	Power meter/ mixer	Mixer	Mixer	Power meter	Power meter	Mixer
Con. Loss (dB)	11.4	NA	10	6.5	7.4	NA
DC Power (mW)	40	12	0	92.5	NA	12
Type	Traveling wave	Injection locking	Schottkey diode	x6 multiplier chain	Single transistor	Superposition oscillator
Technology	65nm CMOS	65nm CMOS	0.13μm CMOS	100nm GaAs mHEMT	50nm GaAs mHEMT	90nm CMOS

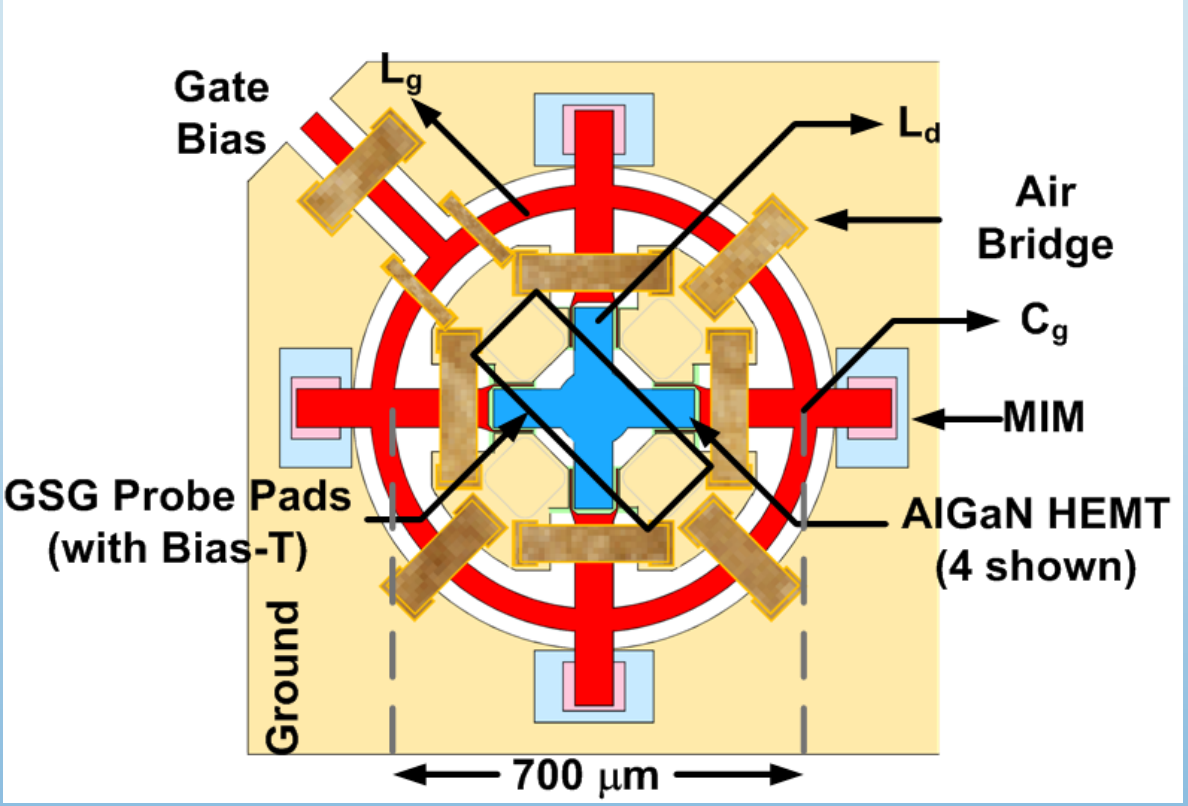
* This is a CMOS oscillator, not frequency multiplier. It is cited to show the maximum output powers on CMOS.

Outline

- Motivation
- THz Signal Generation
  - High Power CMOS Source
  - A Tunable CMOS Source
  - CMOS Frequency Multipliers
  - GaN Implementations
  - Sharp Pulse Generation in CMOS
- THz Signal Amplification
  - Around 300GHz
  - 500GHz and Above
- THz Spectroscopy in CMOS
- THz Imaging Systems

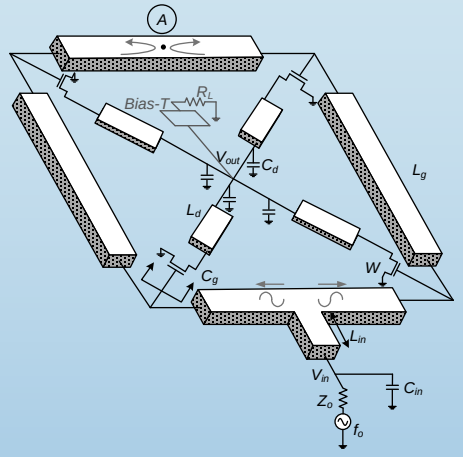
First Prototype

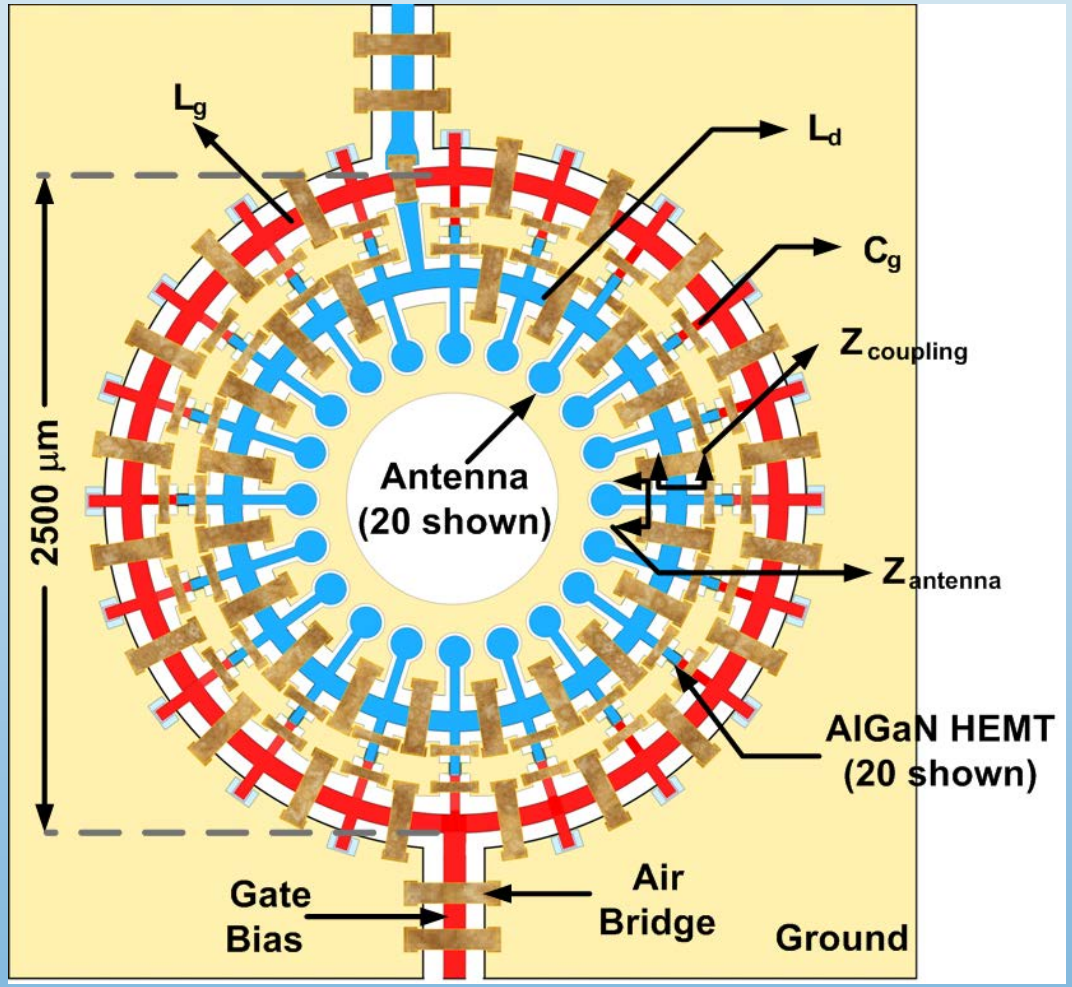




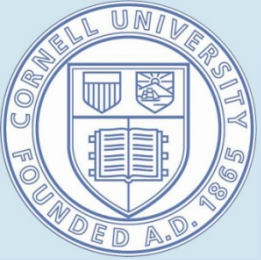
- Simulated maximum output power: 400 - 600 mW at 500 GHz

1 THz Implementation





- Simulated maximum output power: 100- 200 mW at 1 THz



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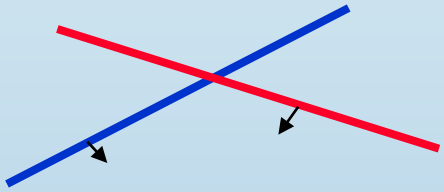
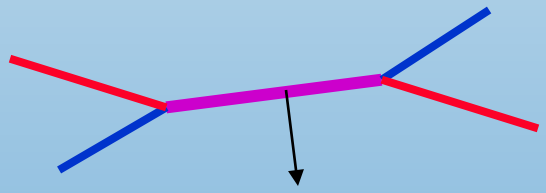
2-D Soliton Resonance



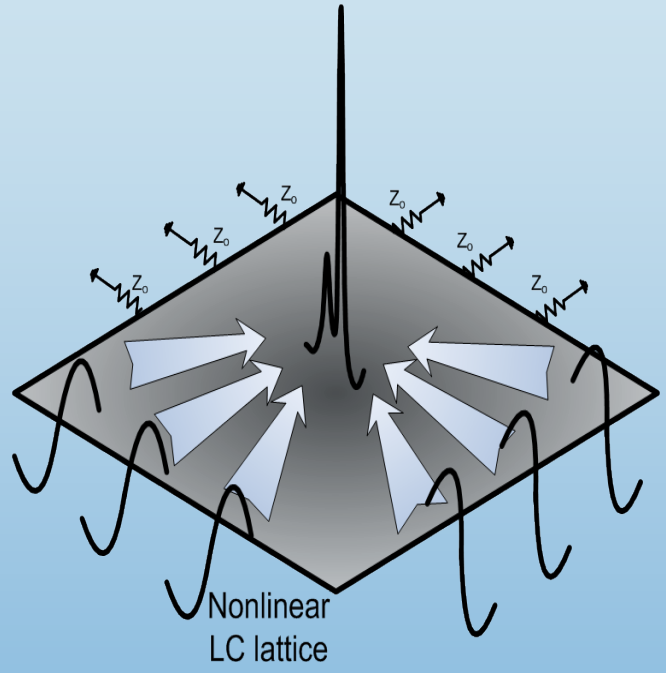


- For a certain range of parameters, two Soliton fronts can combine to generate one.

2-D Soliton Resonance

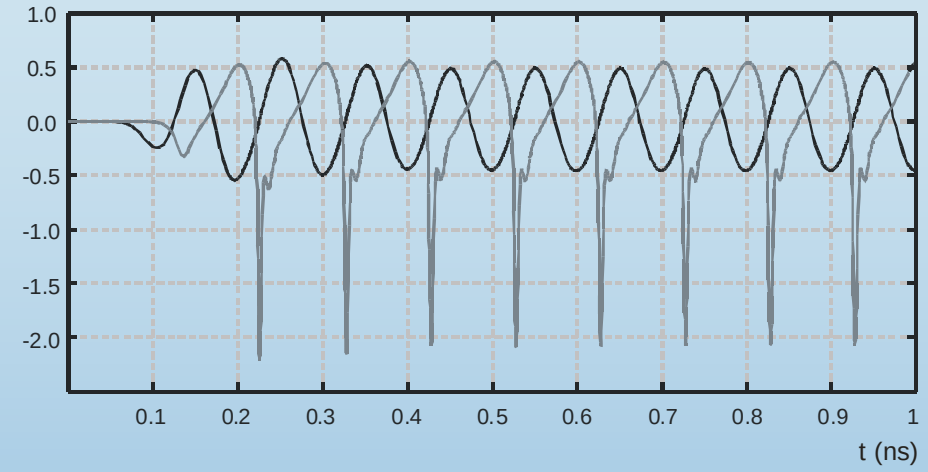
$$L(1+\frac{r_c b_j}{R})\frac{d^2 q_j}{dt^2} = \Delta_d(v_j + r_c\frac{dq_j}{dt}) - r_l\frac{dq_j}{dt}$$

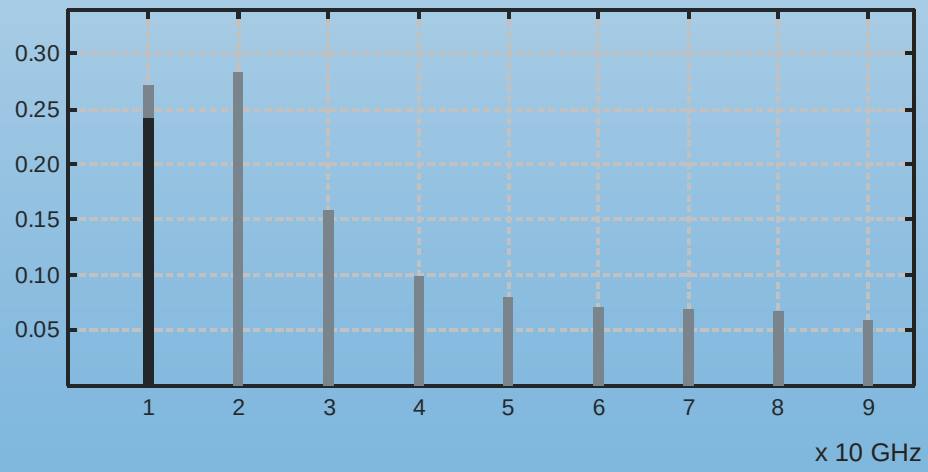
$$-\frac{b_j}{R}[L\frac{dv_j}{dt} + r_l(v_j - V_o + r_c\frac{dq_j}{dt})] + \phi_j V_{in}(t)$$



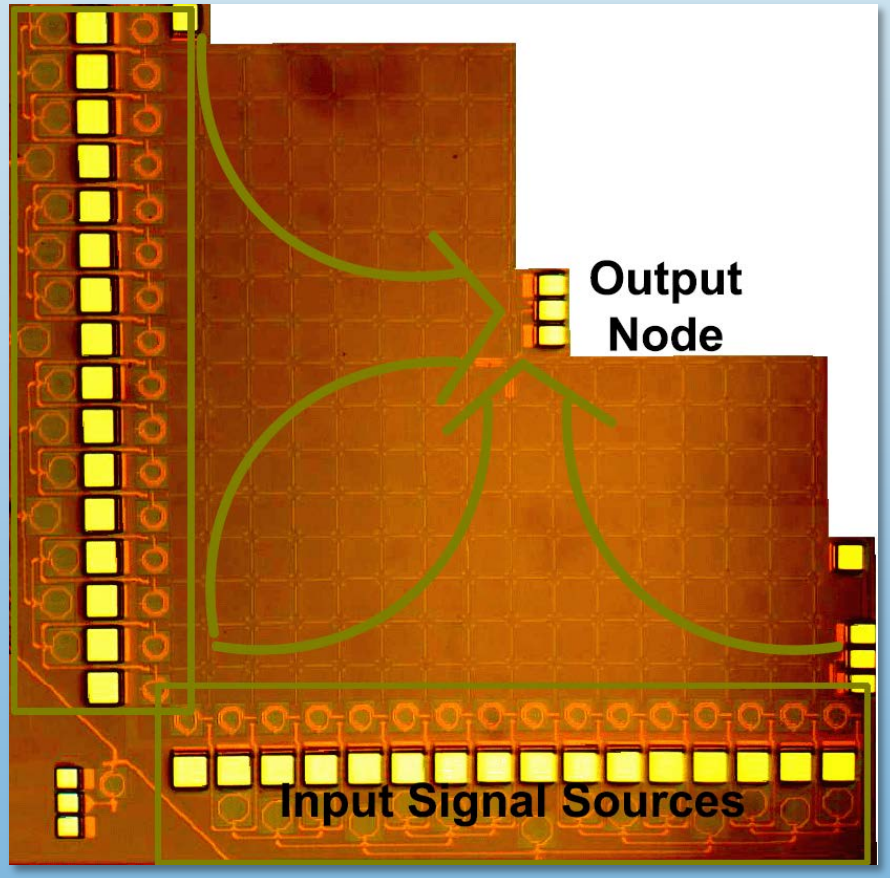
- For a certain range of parameters, two Soliton fronts can combine to generate one.

Prototype





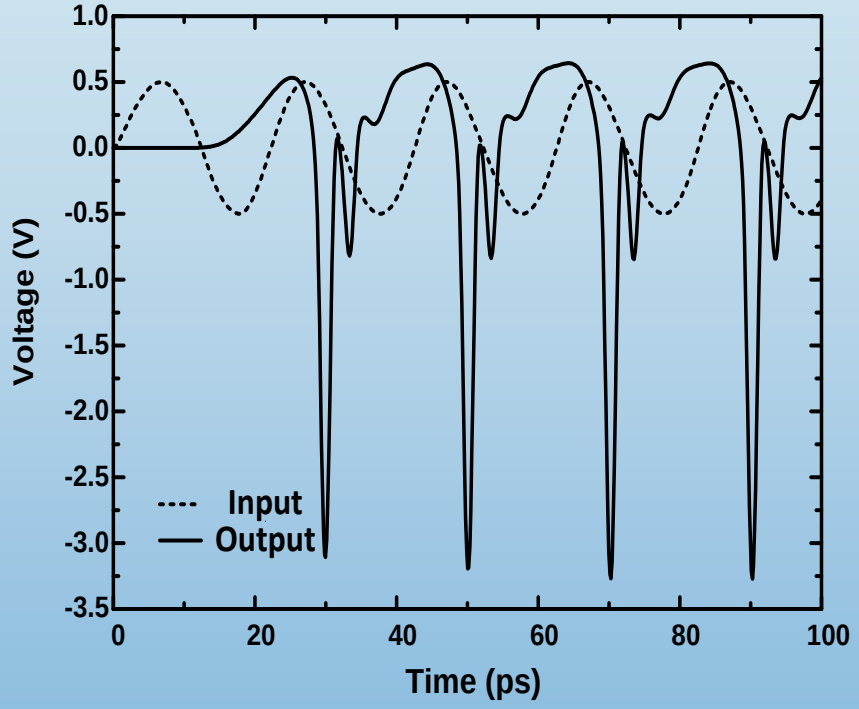
Chip microphotograph



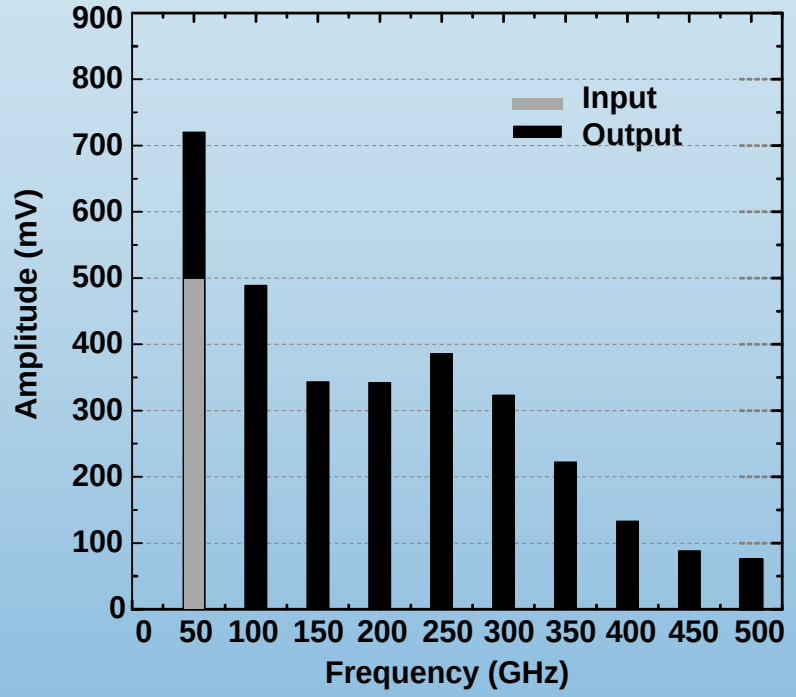
Fabrication in a 0.13 μm CMOS

Optimized Output

Time-domain response



Frequency-domain response



- Output pulse: 1.6psec
- 65nm CMOS
- Better than 1-D line since the signal travels shorter distances.

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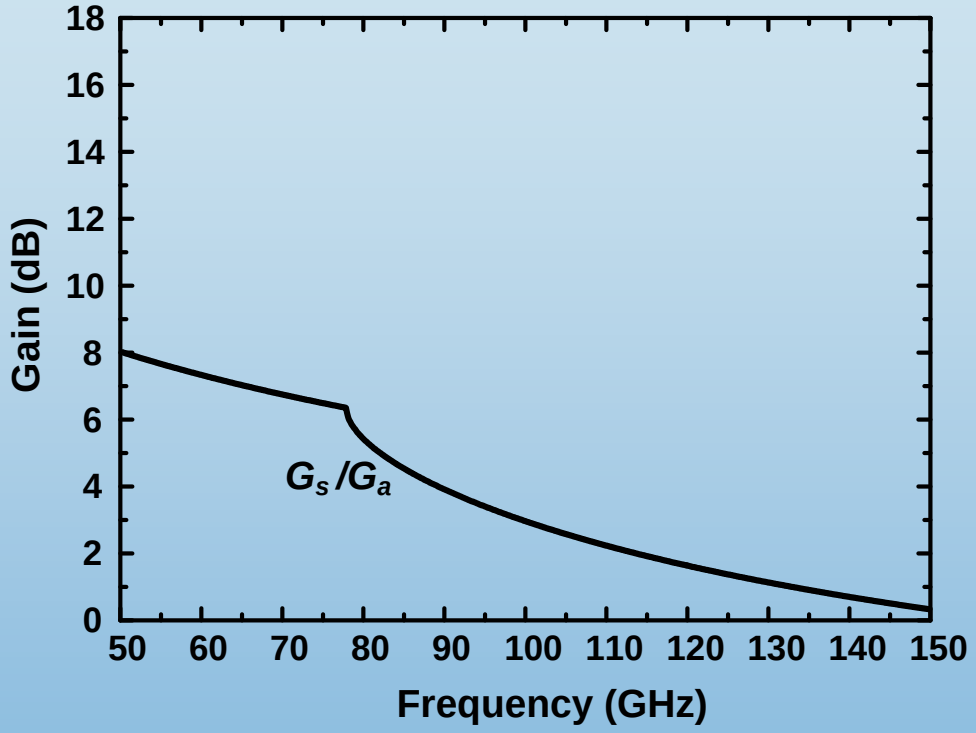
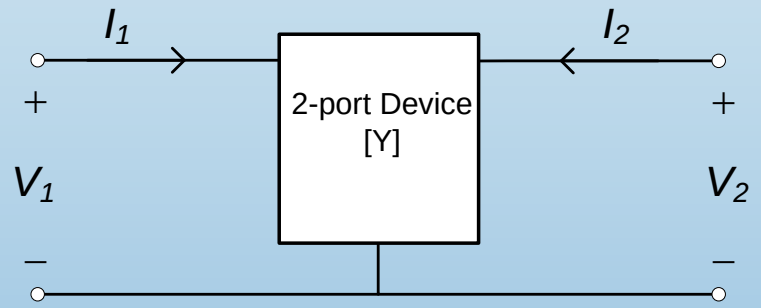
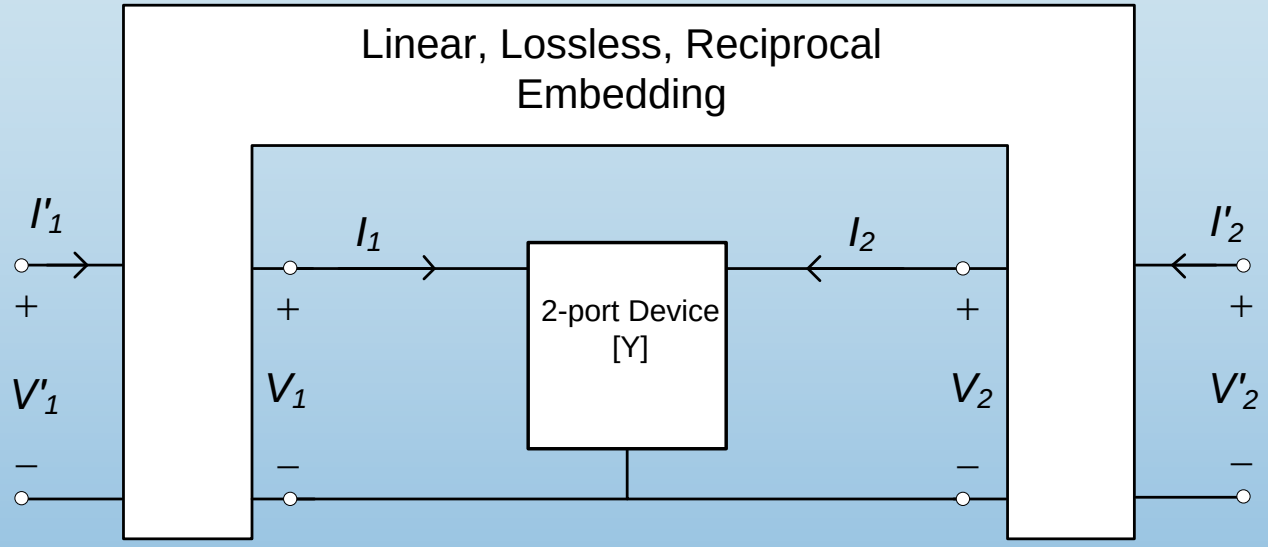
Maximum Stable/Available Gain





- Maximum gains for a single device

Maximum Achievable Gain

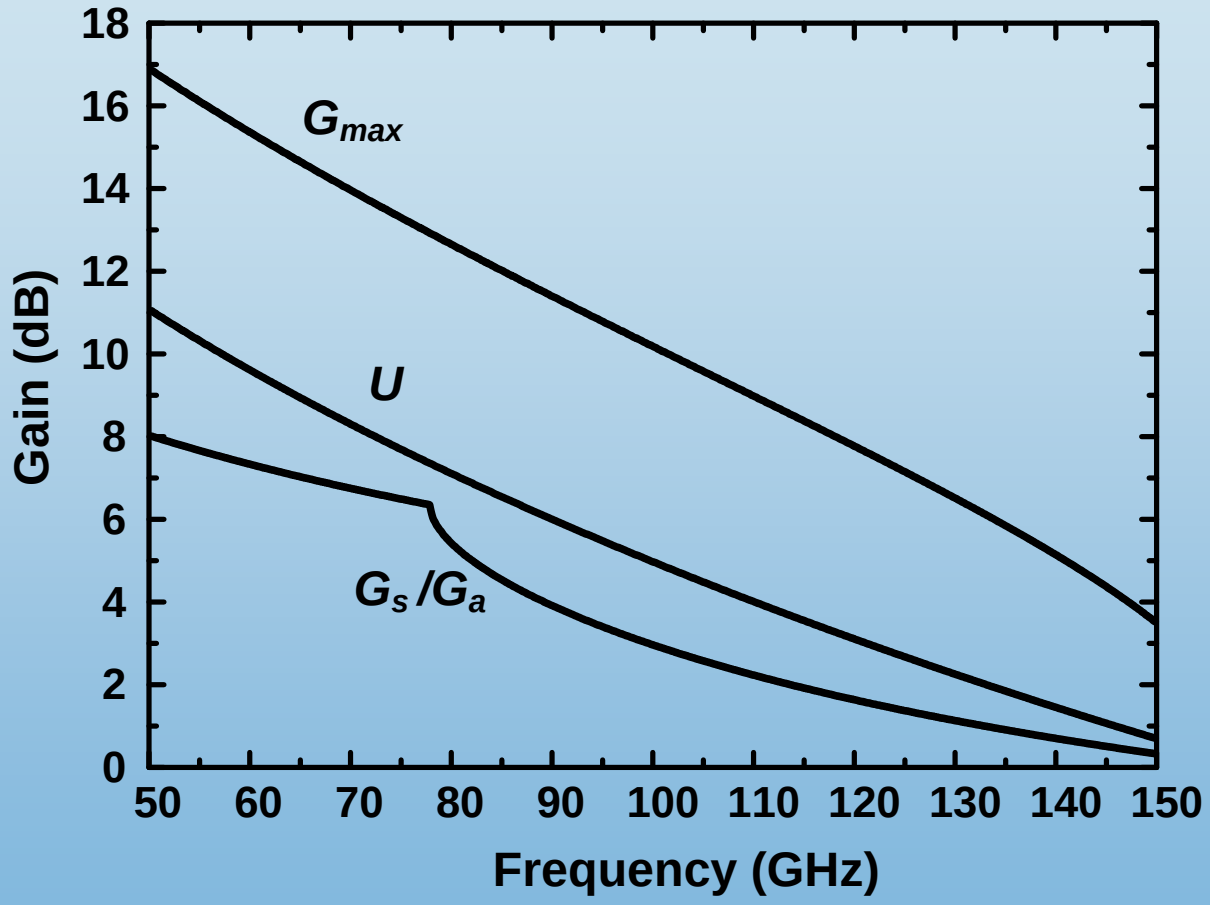


$$U = \frac{\left|Y_{21} - Y_{12}\right|^2}{4(G_{11}G_{22} - G_{12}G_{21})}$$

$$G_{\max} = (2U - 1) + 2\sqrt{U(U-1)} \approx 4U$$

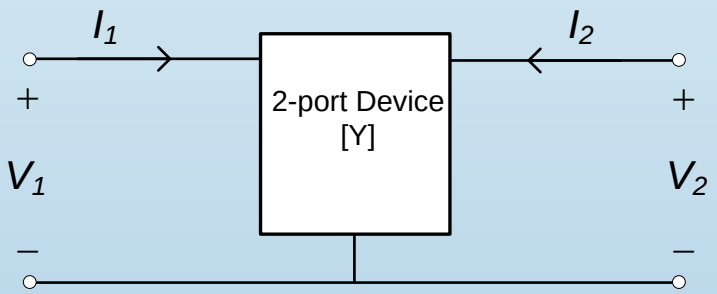
- U is the maximum unilateral gain.
- G_{max} is the maximum achievable gain and is ~6 dB higher than U.

Gain Comparison



Gain simulation of a 40 μm transistor in a 130 nm CMOS

How to Reach G_{max} ?



$$P = V_1^* I_1 + V_2^* I_2$$

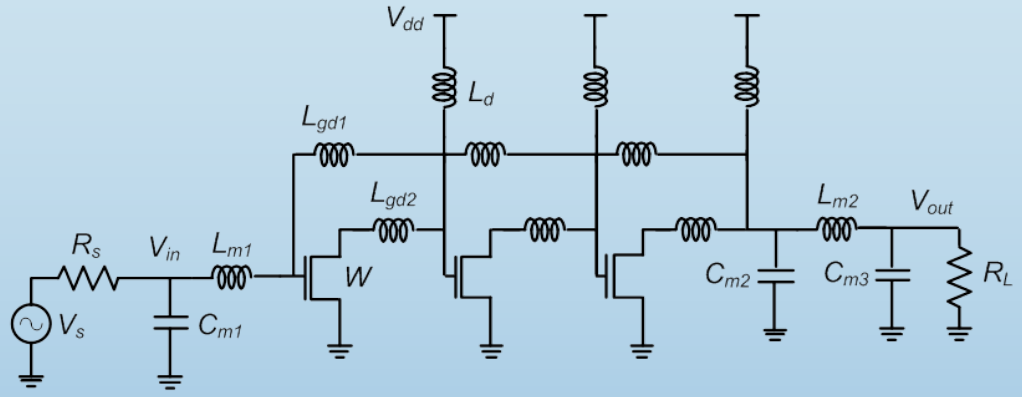
$$\Rightarrow \frac{P_R}{|V_1|^2} = -(G_{11} + A^2 G_{22}) - A\left|Y_{12} + Y_{21}^*\right| \cos(\angle(Y_{12} + Y_{21}^*) + \varphi)$$

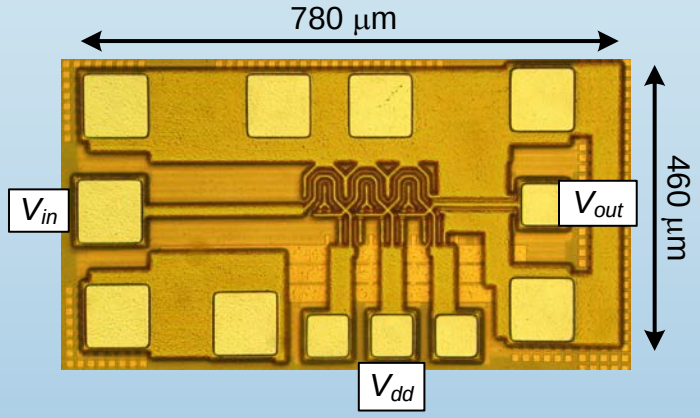
$$A = \left|\frac{V_2}{V_1}\right| \;\&\; \varphi = \angle(\frac{V_2}{V_1}) \qquad A_{opt} = \frac{|Y_{12} + Y_{21}^*|}{2G_{22}} \qquad \varphi_{opt} = (2k+1)\pi - \angle(Y_{12} + Y_{21}^*)$$

For the same $|V_1|$ (i.e., the same input power), maximum P_R (i.e., output power) results in maximum power gain of the device.

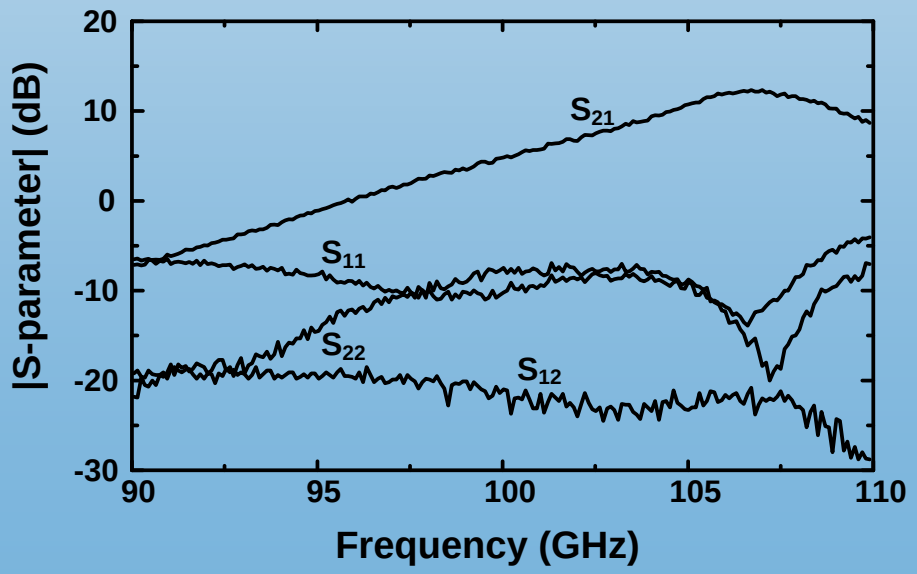
Power Amplifier: the Limit

- The highest possible gain?



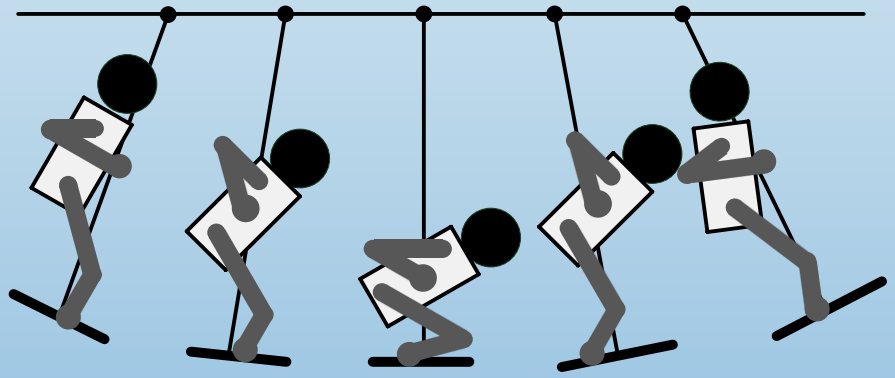


- High gain close to the f_{max} of the process
- Maximum gain at any frequency
- Up to 6dB higher than maximum available gain

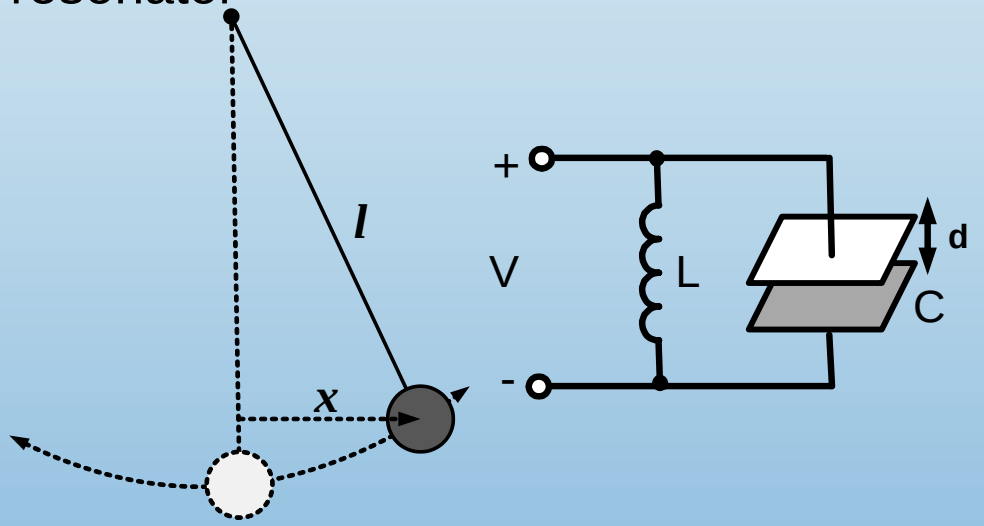


Parametric Amplification

- Parametric amplification at swing



- Duality between swing and LC resonator



The amplitude of the swing increases by moving the body up and down.

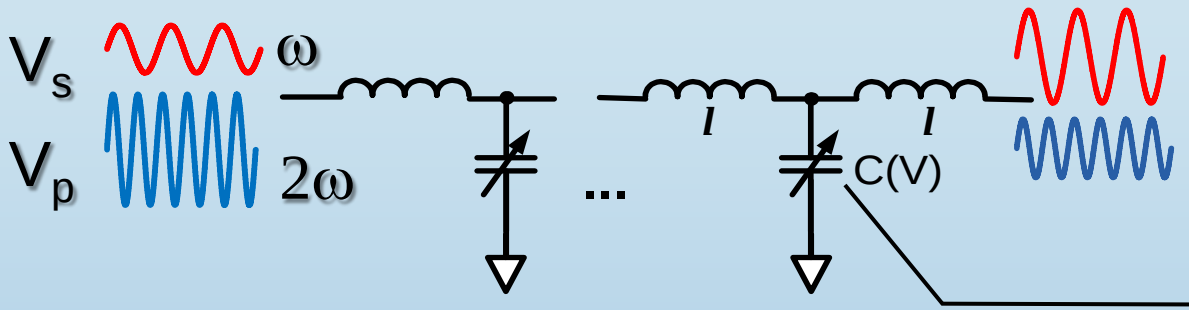
The change of the effective length, *l*, injects the energy to amplify *x*.

$$\frac{d^2x}{dt^2} = -\frac{g}{l}x \qquad \frac{d^2V}{dt^2} = -\frac{1}{LC}V$$

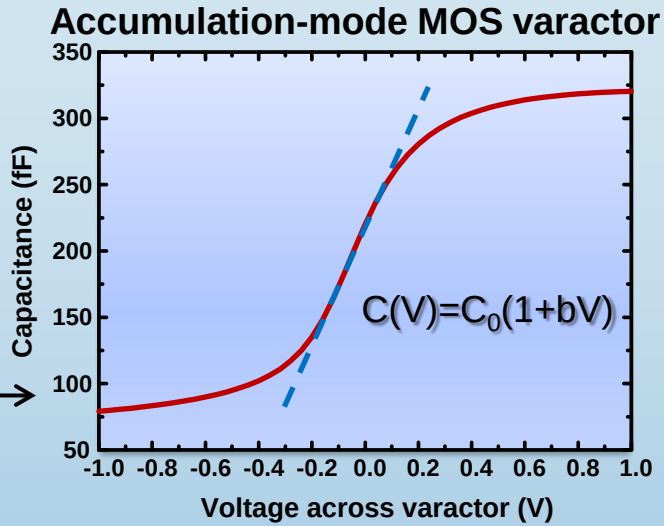
x(distance) $\leftrightarrow$ V (voltage)

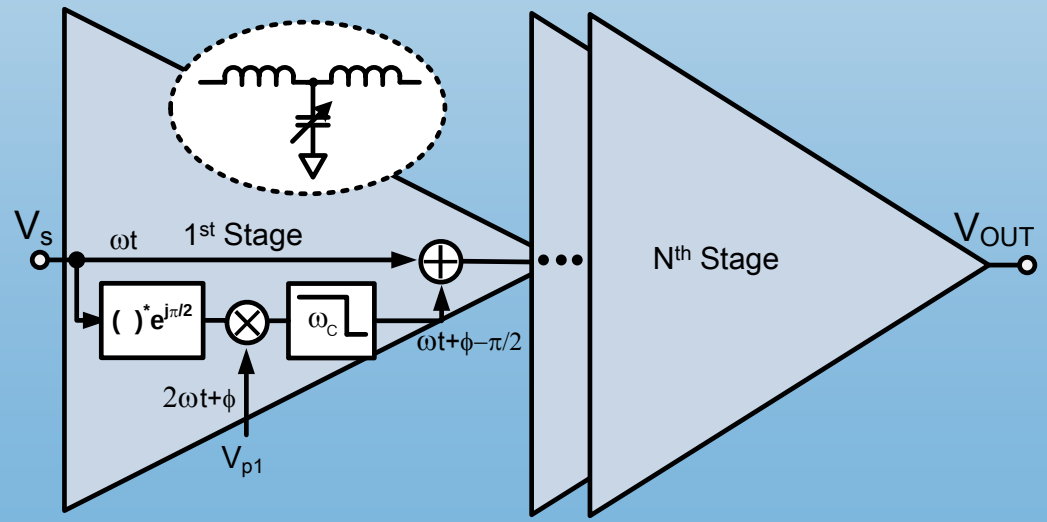
l (length) $\leftrightarrow$ C(capacitance)

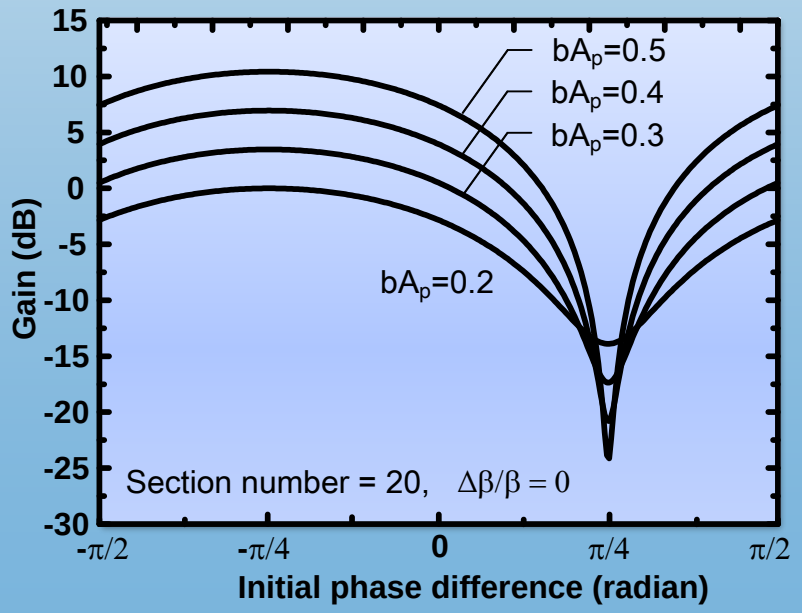
Distributed Parametric Process



$$\frac{\partial^2(V_s+V_p)}{\partial x^2} = LC_0\frac{\partial^2(V_s+V_p)}{\partial t^2} + LC_0 b\frac{\partial^2(V_s\cdot V_p)}{\partial t^2}$$

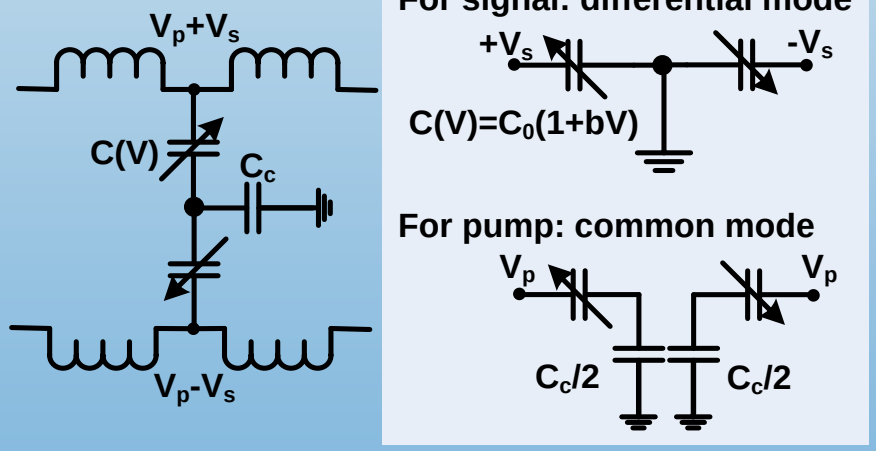




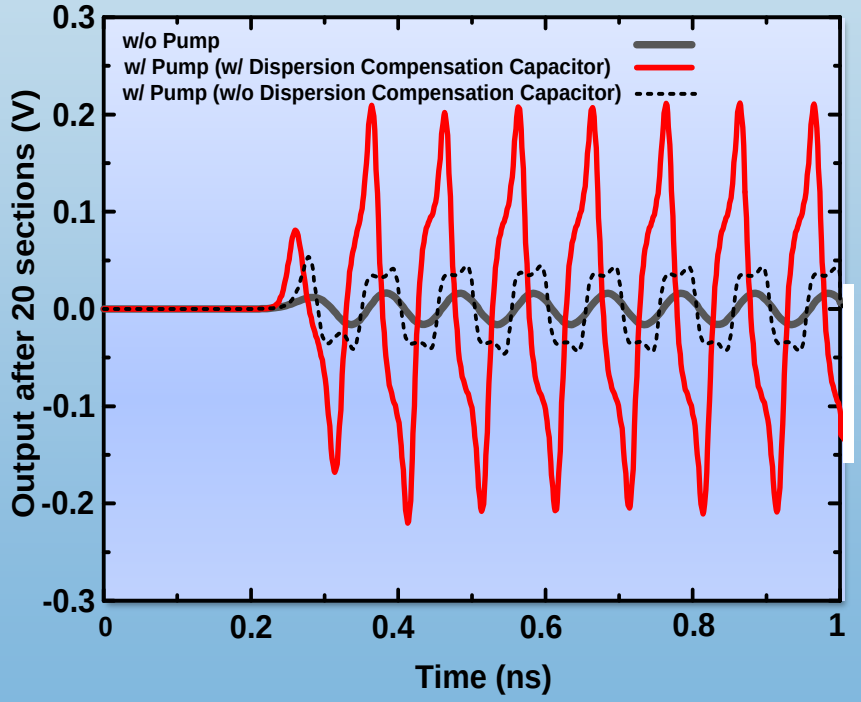


Phase Matching

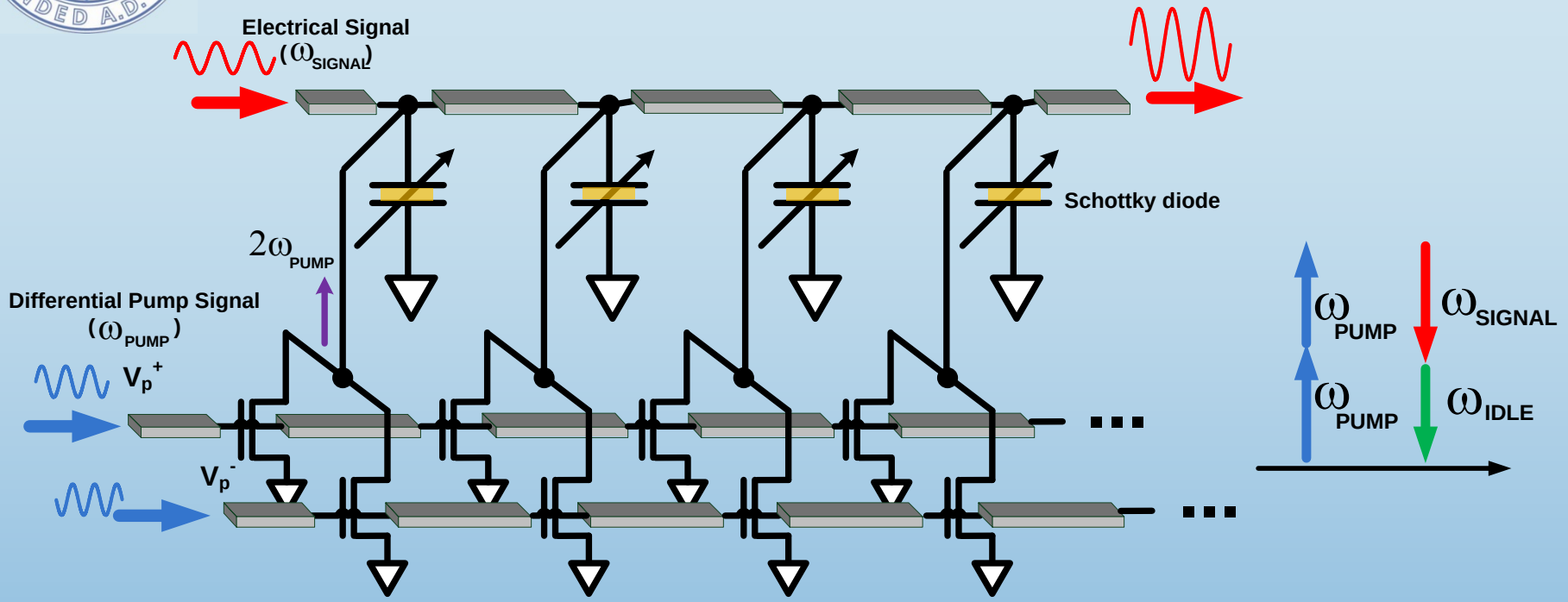
- Proposed phase-matched section



- Simulation result

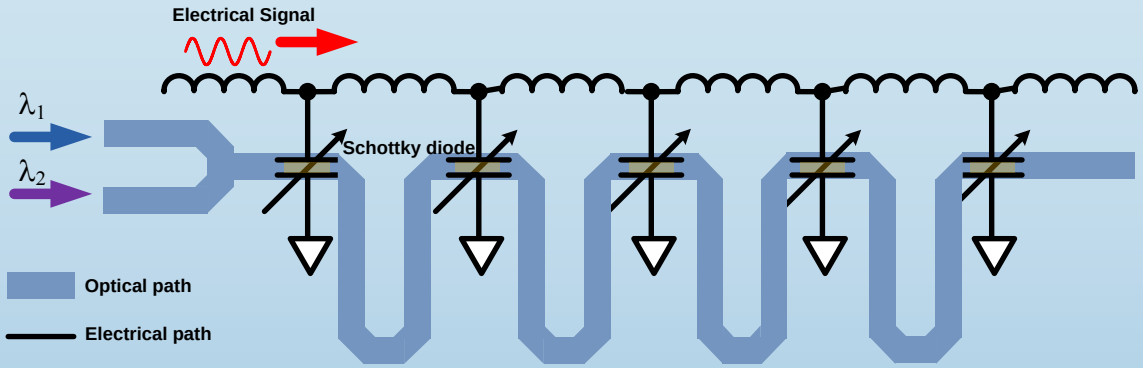


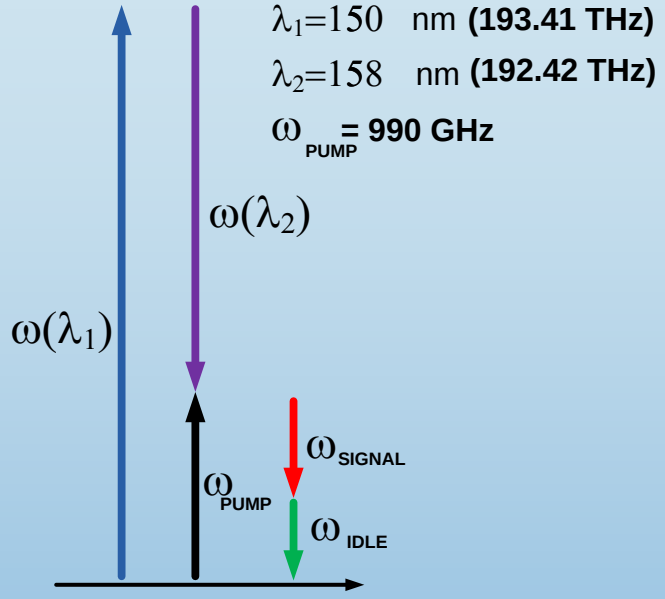
Electronically Pumped Signal



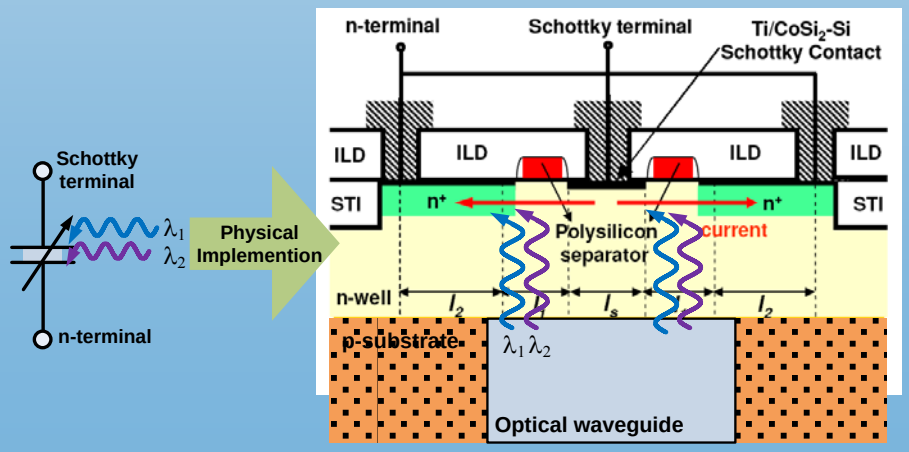
In a standard 65nm CMOS:
@300GHz, 10dB gain, 35GHz BW

Optically Pumped Signal

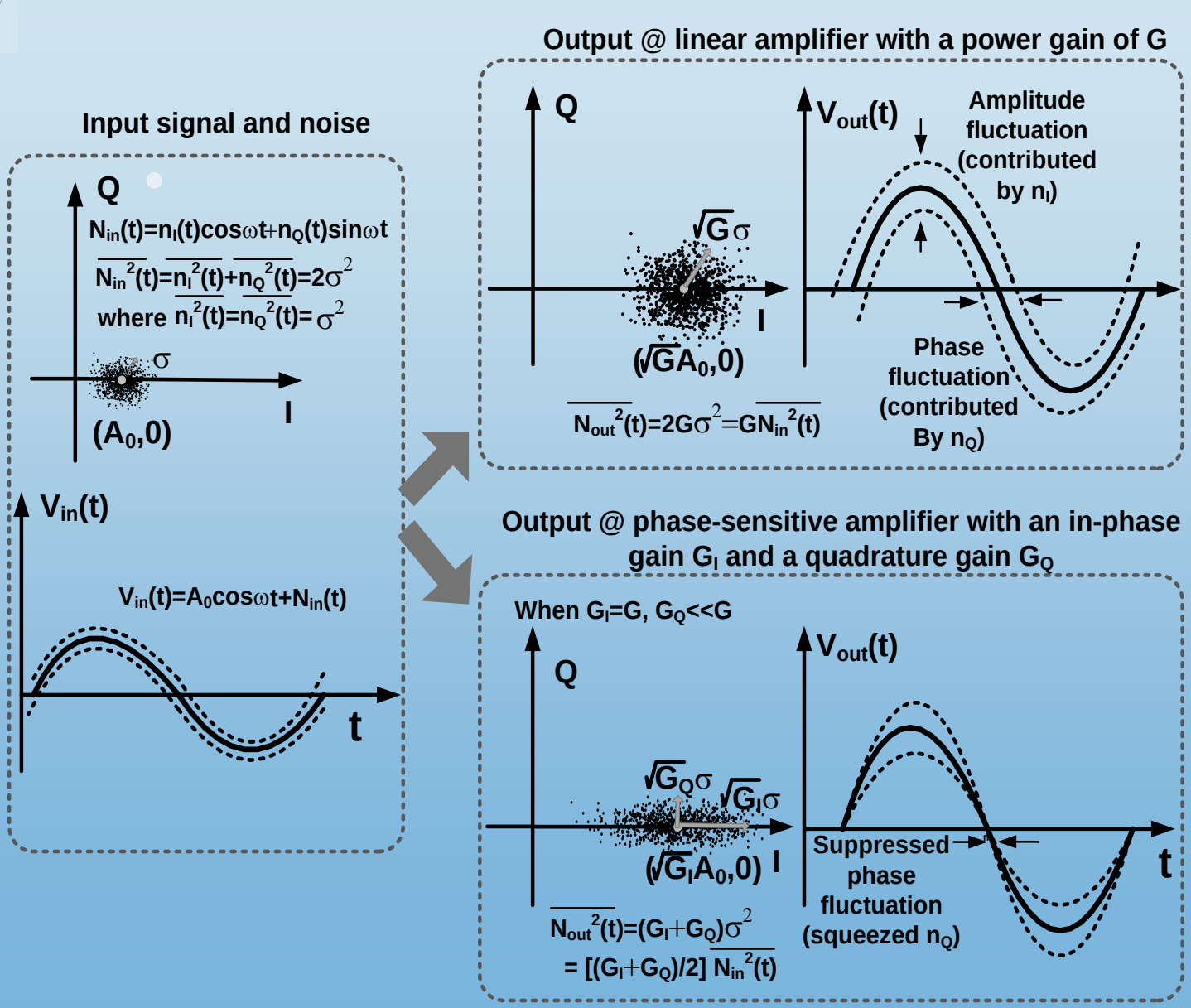


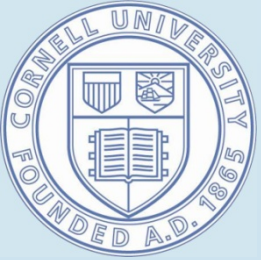


In a standard 65nm CMOS:
@550GHz, 12dB gain, 20GHz BW



Noise Squeezing





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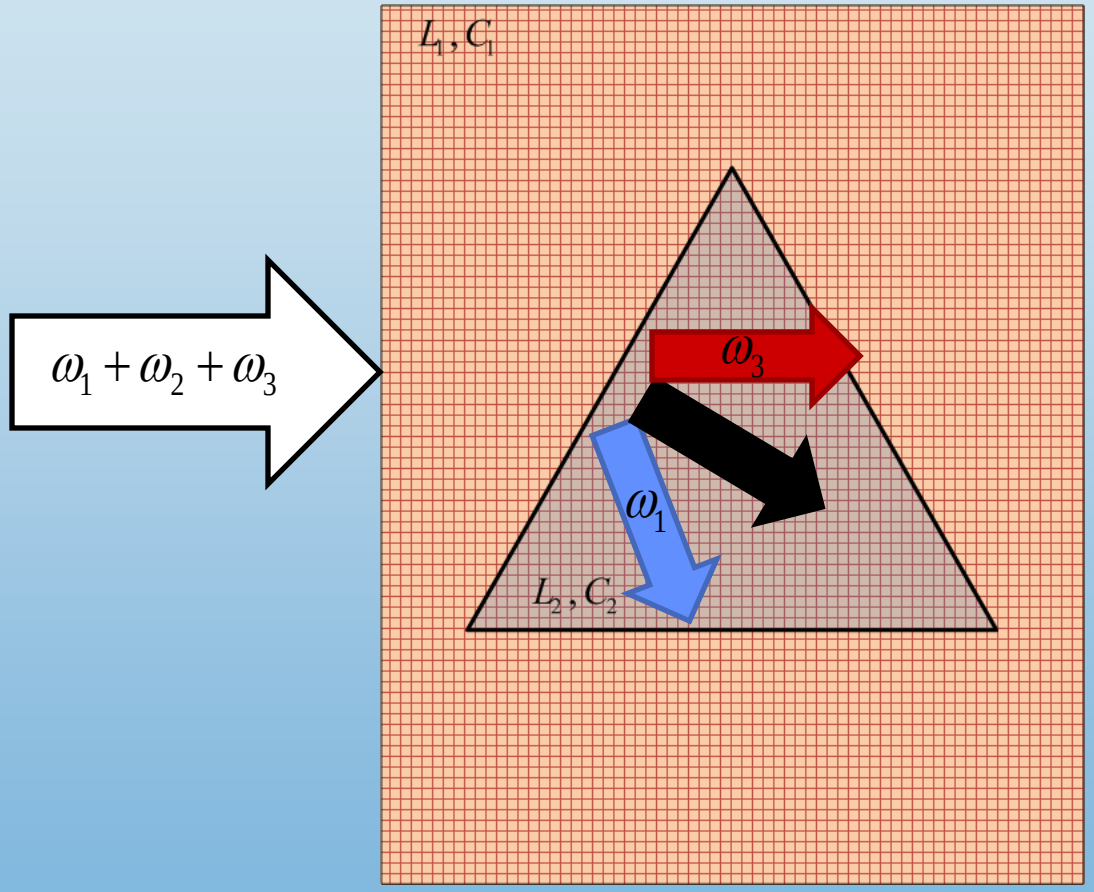
High-frequency Filtering

- The quality factor of conventional passive filters is in the order of the lowest quality factor of the individual components which is low due to ohmic and substrate loss

- We need a filter that offers a quality factor higher than all individual components!

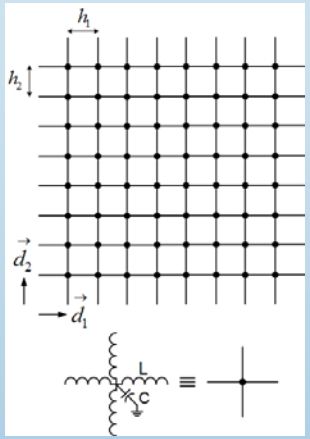
- The quality factor should be function of the geometry.

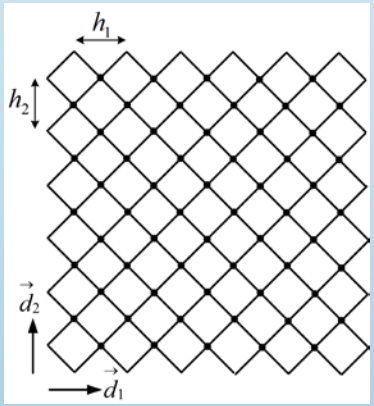
Spatial Filter

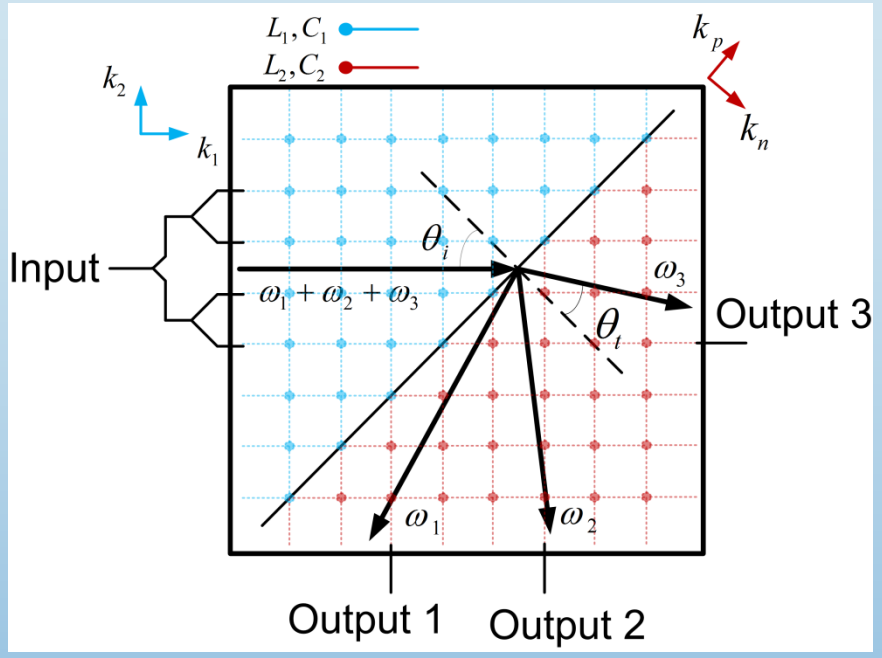


Different frequency components travel in different directions

Basic Principle



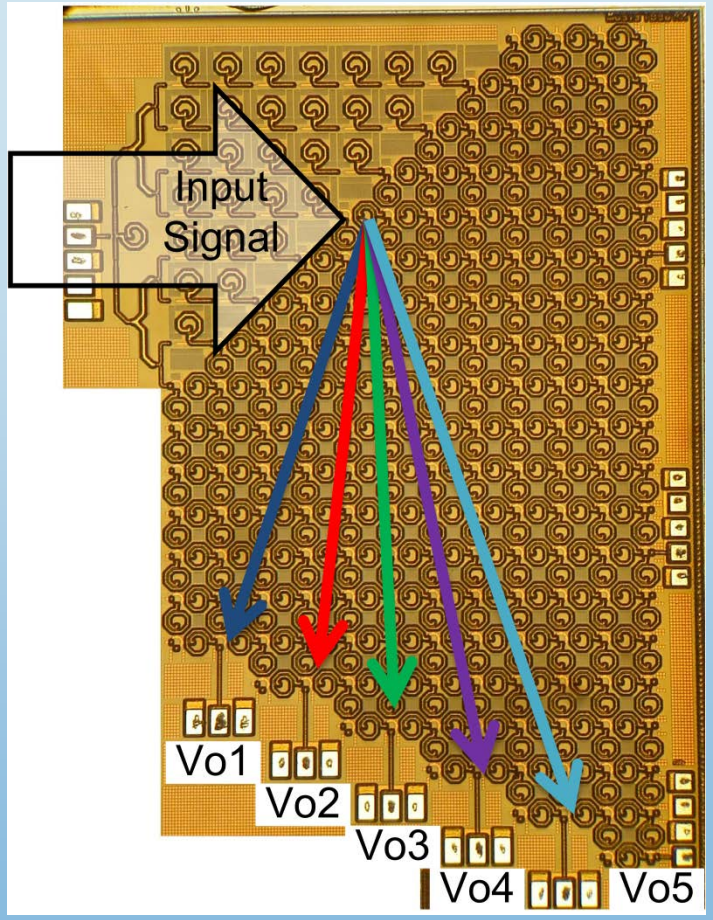




$$\angle \vec{V}_g = \tan^{-1}\left(\frac{h_2 \sin k_2}{h_1 \sin k_1}\right)$$

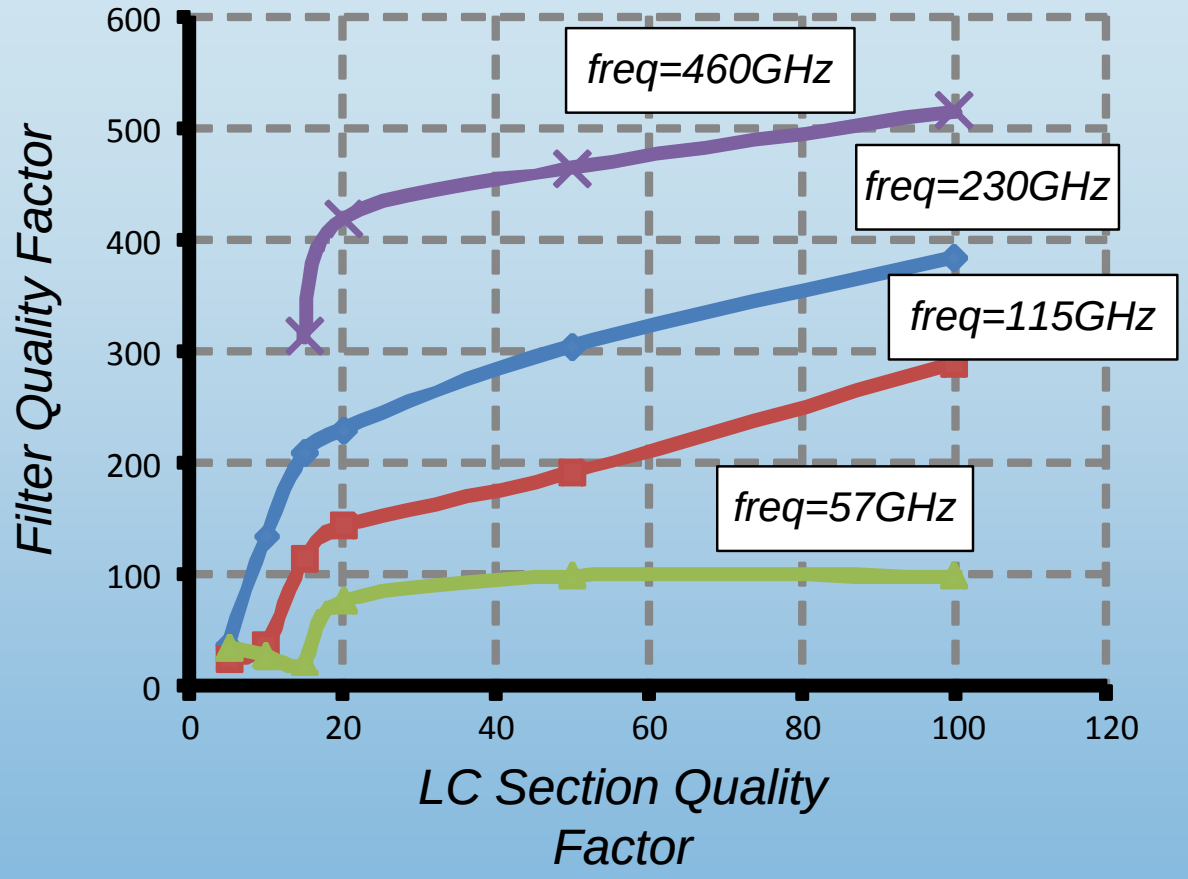
$$\theta_t = \angle \vec{V}_g = \tan^{-1}\left(\frac{h_2}{h_1}\frac{\sin\left(\frac{k_1+k_2}{2}\right)-\sin\left(\frac{k_1-k_2}{2}\right)}{\sin\left(\frac{k_1+k_2}{2}\right)+\sin\left(\frac{k_1-k_2}{2}\right)}\right)$$

First Prototype



- The first implementation at around 40GHz
- Quality factor of around 50

Effect of Loss

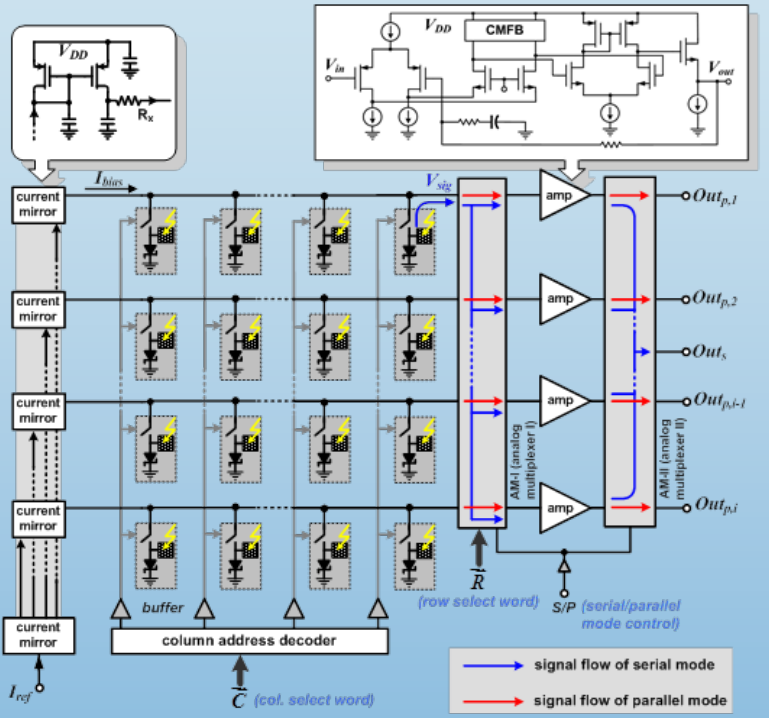


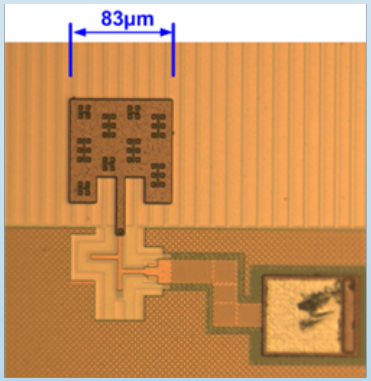
- The performance enhances with frequency

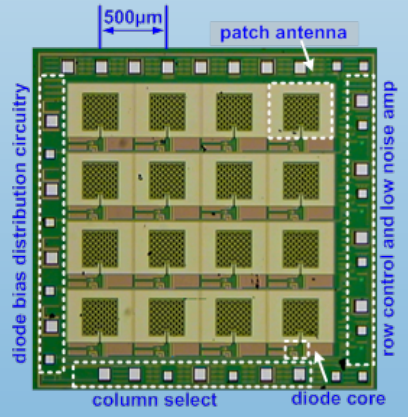
Outline

- Motivation
- THz Signal Generation
  - High Power CMOS Source
  - A Tunable CMOS Source
  - CMOS Frequency Multipliers
  - GaN Implementations
  - Sharp Pulse Generation in CMOS
- THz Signal Amplification
  - Around 300GHz
  - 500GHz and Above
- THz Spectroscopy in CMOS
- THz Imaging Systems

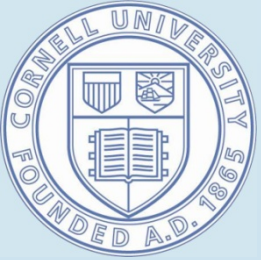
A THz Camera







	ISSCC 2011 [1]	*RFIC 2011* [2]	*IMS 2011* [3]	*This Work*	
Technology	130nm CMOS	65nm SOI CMOS	65nm CMOS	SBD in 130nm CMOS (logic)	
Array Size	3×4	15 (standalone)	15 (standalone)	4×4	single pixel
Responsivity (amplifier excluded)	2.5kV/W @ 300GHz 51V/W @ 1THz	1.9kV/W @ 650GHz (w/ lens)	800V/W @ 1THz	323V/W @ 283GHz	355V/W @ 860GHz
Measured NEP	Not demonstrated	17pW/Hz$^{1/2}$ (w/ lens)	66pW/Hz$^{1/2}$	29pW/Hz$^{1/2}$	32pW/Hz$^{1/2}$
Pixel Multiplexing	Yes (not tested)	No	No	Yes (dual mode)	No



A New Frontier: CMOS Terahertz Signal Generation and Amplification

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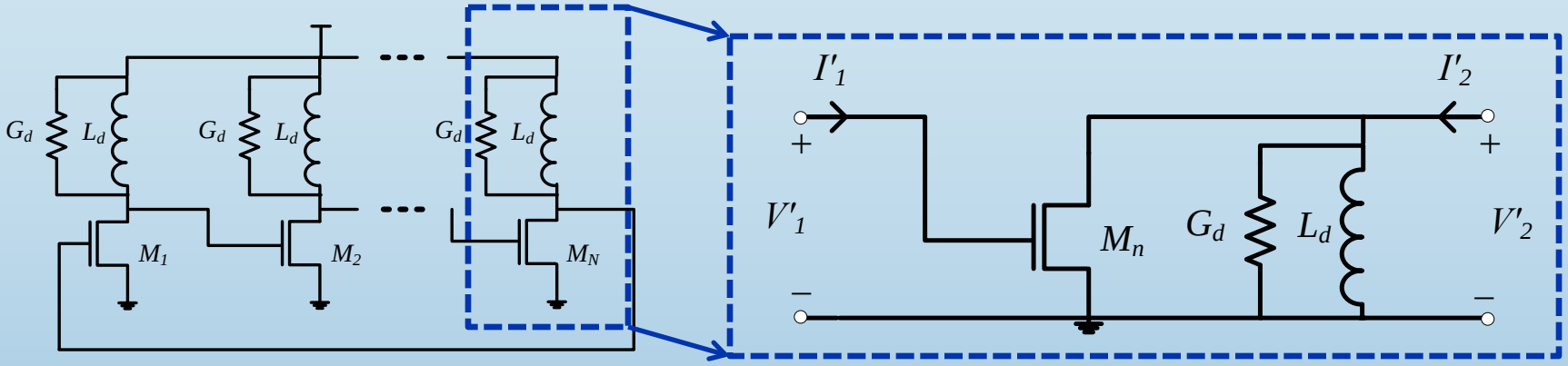
April 2012

Example: Ring



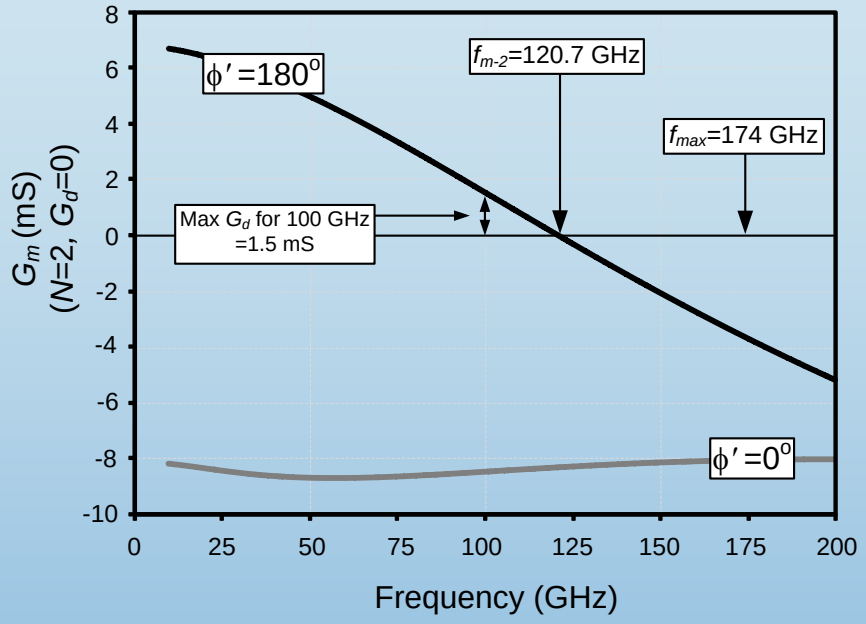
- In a ring oscillator the phase conditions are set by the number of stages
- The gain of each stage is 1.

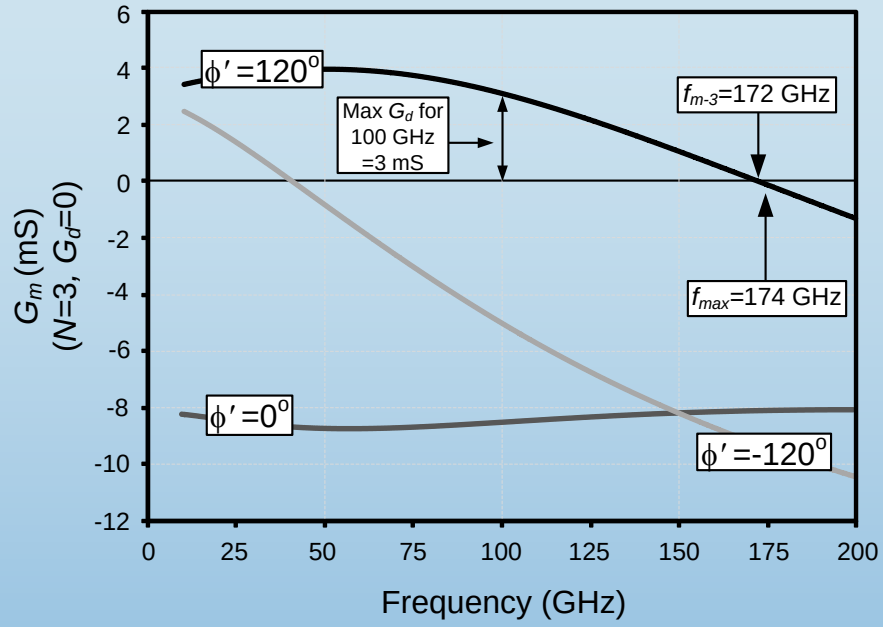
$$\begin{bmatrix} I'_1 \\ I'_2 \end{bmatrix} = [Y'] \begin{bmatrix} V'_1 \\ V'_2 \end{bmatrix}$$

$$A' = \frac{|V'_2|}{|V'_1|} = 1$$

$$\phi' = \angle \frac{V'_2}{V'_1} = k\frac{2\pi}{N}$$

Example: Ring





Simulation of the maximum frequency of oscillation *for a 2-stage ring oscillator in the* employed 0.13 um CMOS process.

Simulation of the maximum frequency of oscillation for a 3-stage ring oscillator in the employed 0.13 um CMOS process.

Activity Condition: $$G_m = \frac{P_R}{|V_1||V_2|} = -(G_{11} + G_{22} + G_d) - \left|Y_{12} + Y_{21}^*\right| \cos(\angle(Y_{12} + Y_{21}^*) + k\frac{2\pi}{N}) > 0$$