Gallium Nitride Power MMICs – Fact and Fiction

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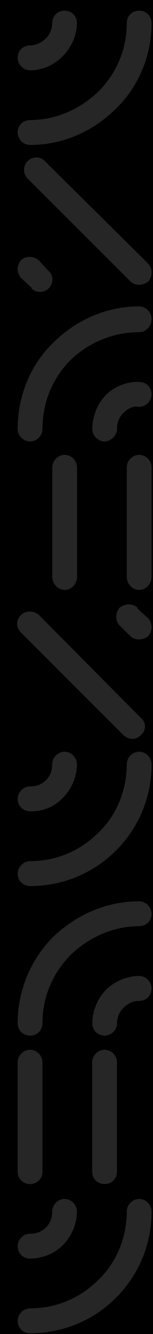


Introduction

- Gallium Nitride has many attractive characteristics
  - High operating voltage capability (V_{BD})
  - High current capability (I_{MAX})
  - Good microwave performance (G_{MAX} , f_T , f_{MAX})
  - Good low noise performance (NF_{MIN})
  - High thermal conductivity Silicon Carbide substrate
- Should be ideal for microwave power applications!

Introduction

- Use of GaN based technology is rapidly growing
  - Military (Radar, EW, Communications)
  - Infrastructure (Basestation, Weather Radar, Satcom)
  - Commercial (CATV, Test equipment)
- Numerous circuit functions have been demonstrated
  - Power amplifiers
  - Low noise amplifiers
  - RF control components

Introduction

- GaN MMIC design however is not without issues
- Some are obvious
  - High voltage / high current
  - Thermal
- Some are less so
  - Wideband power amplifier designs
  - Power combining
  - User interface / driver circuitry

High Output Impedance = More Bandwidth?

- High voltage operation = higher output impedance
  - Reduced transformation ratios
  - Lower loss, wider band matching networks
  - Less complex combining networks or more power
- All true! Sometimes …….
  - Narrow to moderate bandwidth designs do benefit
  - Low frequency wideband designs also benefit

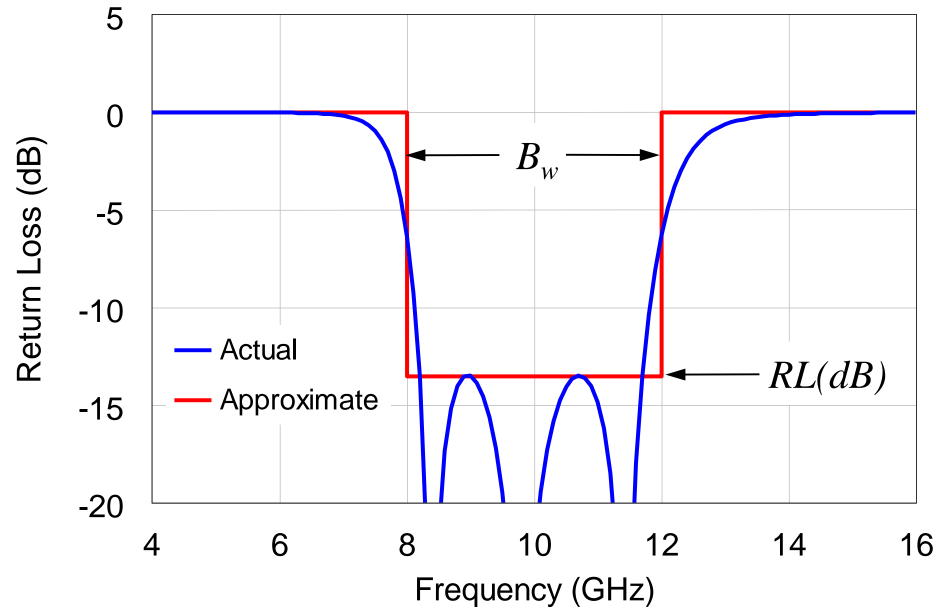
High Output Impedance = More Bandwidth?

- This not always true for reactively matched wideband microwave frequency designs
- A restriction comes into play: Bode-Fano Limit [1]

$$\int_0^\infty \ln|1/\Gamma(\omega)|\,d\omega \leq \frac{\pi}{R_p C_p}$$

$$B_w < \frac{4.343}{R_p C_p RL(dB)}$$

$$R_p \approx \beta \frac{V_D - V_K}{I_{max}}$$



High Output Impedance = More Bandwidth?

- $R_p C_p$ Bias Dependence for a 0.25μm GaN FET

18 GHz Load Pull, 100 mA/mm, 8x50um, 20um Pitch

Efficiency Tuning

Rp (Ohm-mm): 180, 160, 140, 120, 100, 80, 60

Cp (pF/mm): 0.40, 0.37, 0.34, 0.31, 0.28, 0.25, 0.22

Drain Voltage (V): 15, 20, 25, 30, 35, 40, 45, 50

High Output Impedance = More Bandwidth?

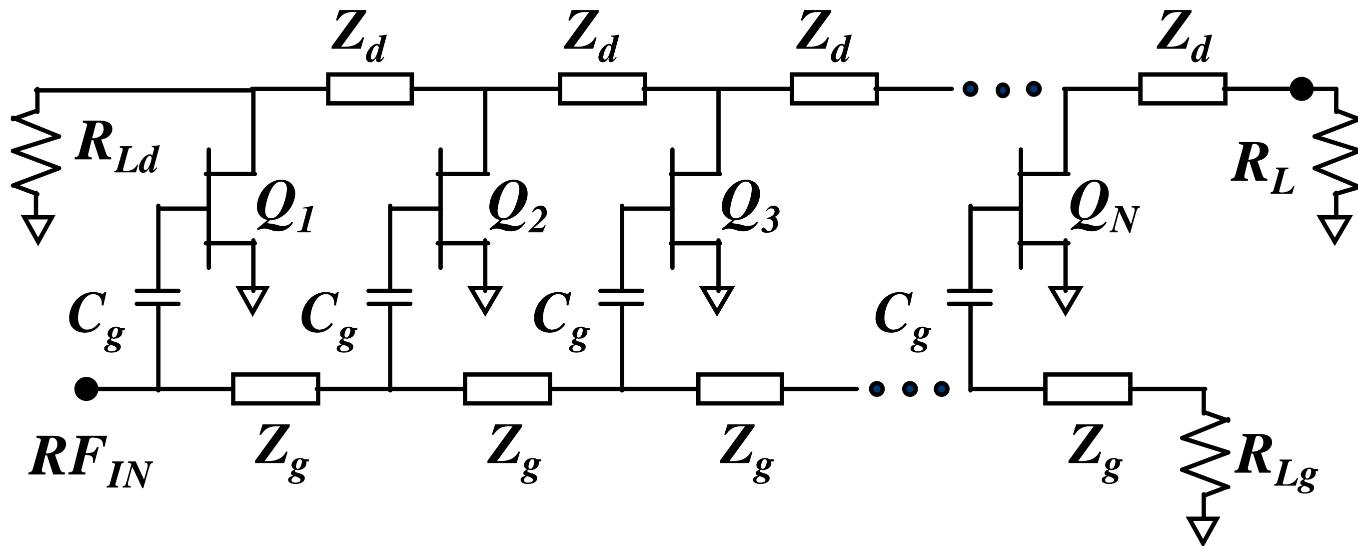
- So why does this matter ?
- Bandwidth limit for a 6V GaAs PHEMT is > 30GHz
- The efficiency tuned load target for a 0.25μm GaN HEMT at 18GHz and V_D = 35V is….

$$R_P = 120\ \Omega\text{-}mm \qquad C_P = 0.3\ pF/mm$$

- For 20dB return loss bandwidth is < 6GHz !
- This assumes an infinite order matching network!!

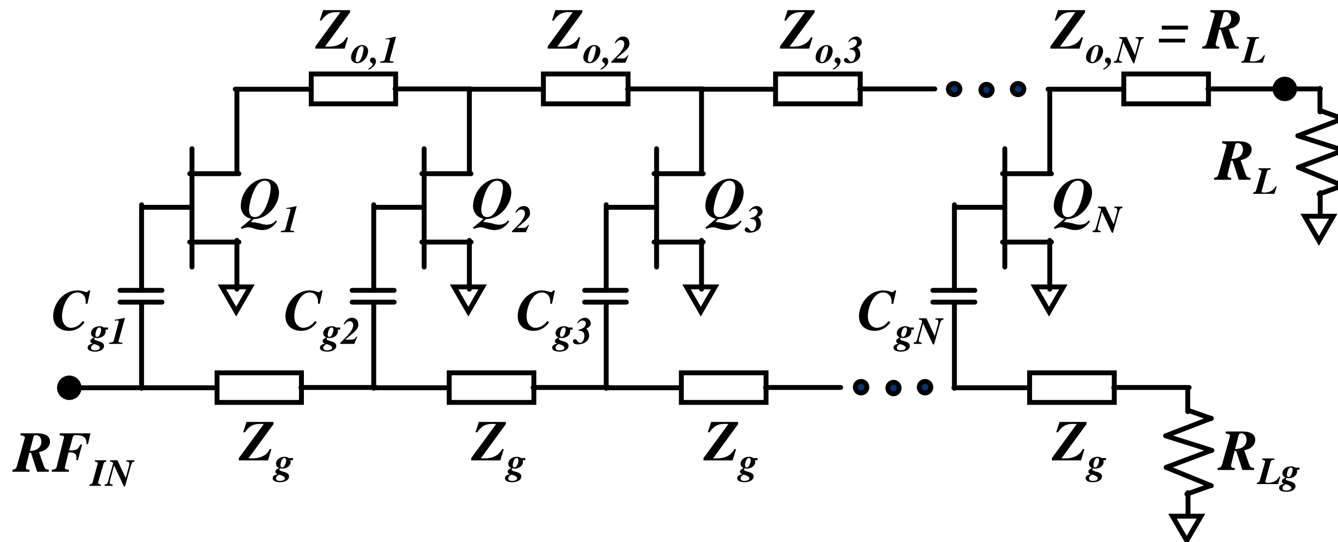
Dealing with Bode-Fano

- Bandwidth increases if C_P is reduced
- Fundamental idea behind the distributed amplifier
- Uniform distributed amplifier – ***<u>Not a good PA</u>***



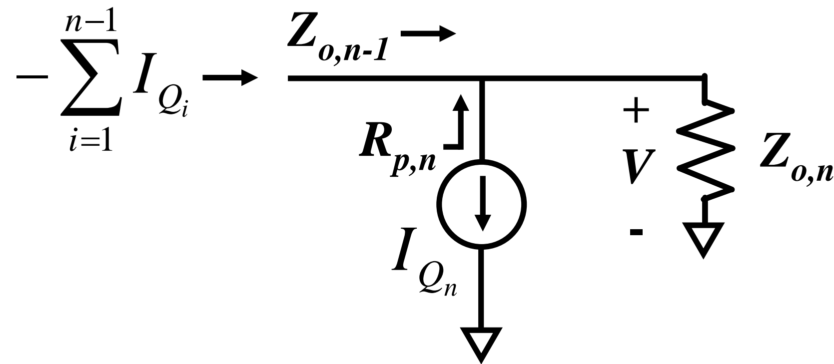
Dealing with Bode-Fano

- Power performance is improved with a non-uniform distributed power amplifier topology (NDPA) [2]
  - Output termination R_{Ld} removed
  - Output line $Z_{o,n}$ and gate capacitors $C_{g,n}$ are varied



Dealing with Bode-Fano

- So how are the drain line impedances varied?
- Simplified low frequency nth FET output model



- Summing the currents at the drain node

$$\sum_{i=1}^{n-1} I_{Q_i} + I_{Q_n} + \frac{V}{Z_{0,n}} = 0$$

Dealing with Bode-Fano

- Solve for $R_{p,n}$ and assume uniform drive and loading such that the current scales with periphery

$$R_{p,n} = \frac{V}{-I_{Q_n}} = Z_{0,n}\left(1 + \frac{1}{I_{Q_n}}\sum_{i=1}^{n-1} I_{Q_i}\right) = \frac{Z_{0,n}}{W_{Q_n}}\sum_{i=1}^{n} W_{Q_i}$$

- Normalize $R_p = R_{p,n}W_{Qn}$ and solve for $Z_{o,n}$

$$Z_{0,n} = \frac{R_p(\Omega \cdot mm)}{\sum_{i=1}^{n} W_{Q_i}}$$

Dealing with Bode-Fano

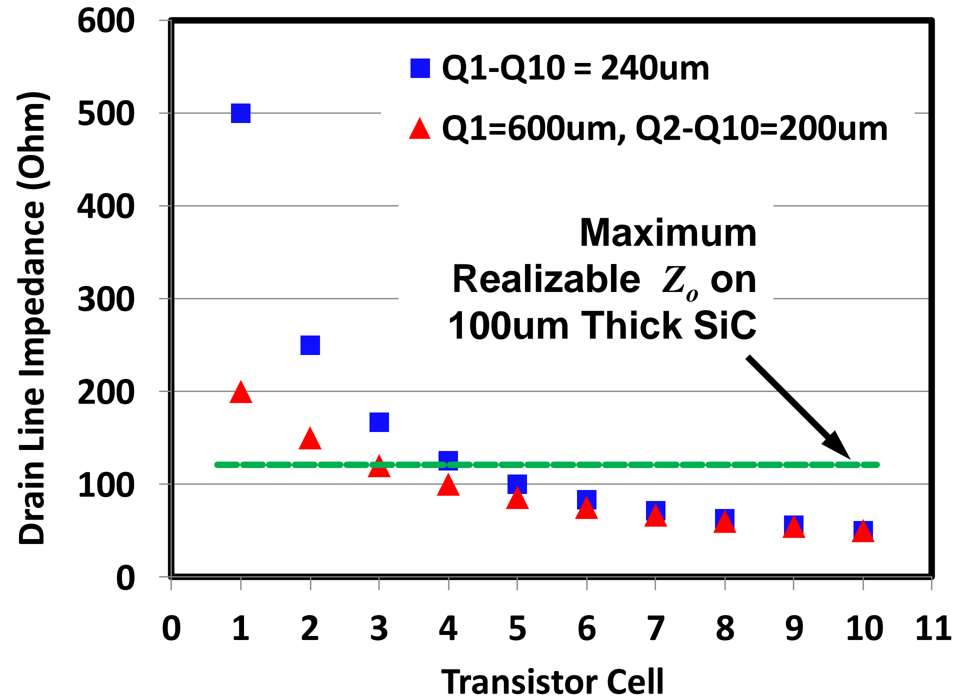
- The drain line impedance for the Nth FET will be,

$$Z_{0,N} = R_L = \frac{R_p(\Omega \cdot mm)}{\sum_{i=1}^{N} W_{Q_i}} \qquad or \qquad \frac{R_p(\Omega \cdot mm)}{R_L(\Omega)} = \sum_{j=1}^{N} W_{Q_j}$$

- This condition fixes the total periphery and therefore the expected output power capability of the amplifier
- Increase periphery (power) by increasing R_p (V_D) or decreasing the amplifier load impedance R_L

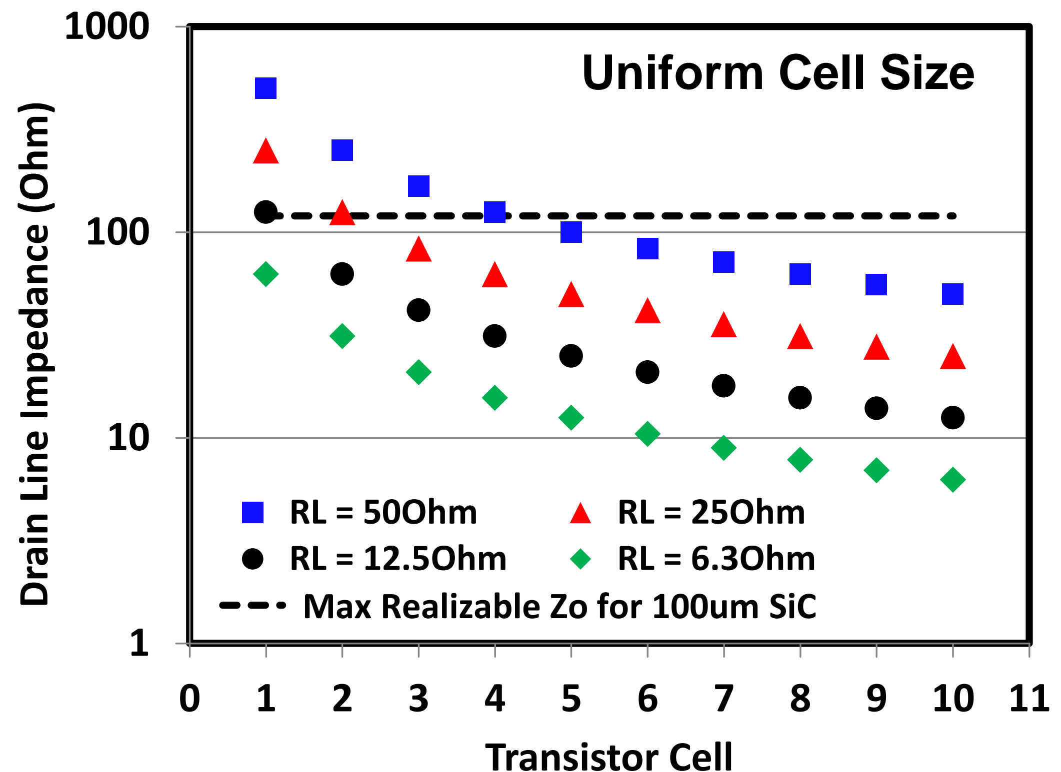
Dealing with Bode-Fano

- Consider the following example for $R_L = 50\Omega$
  - $N = 10$ FET cells
  - $R_P = 120\ \Omega$-mm
  - Total Periphery: 2.4mm
  - Power: 7-12W (3-5W/mm)
- Very high Z_o
- Q_1 size sets max Z_o [3]
- ***The first transistors are poorly loaded!***



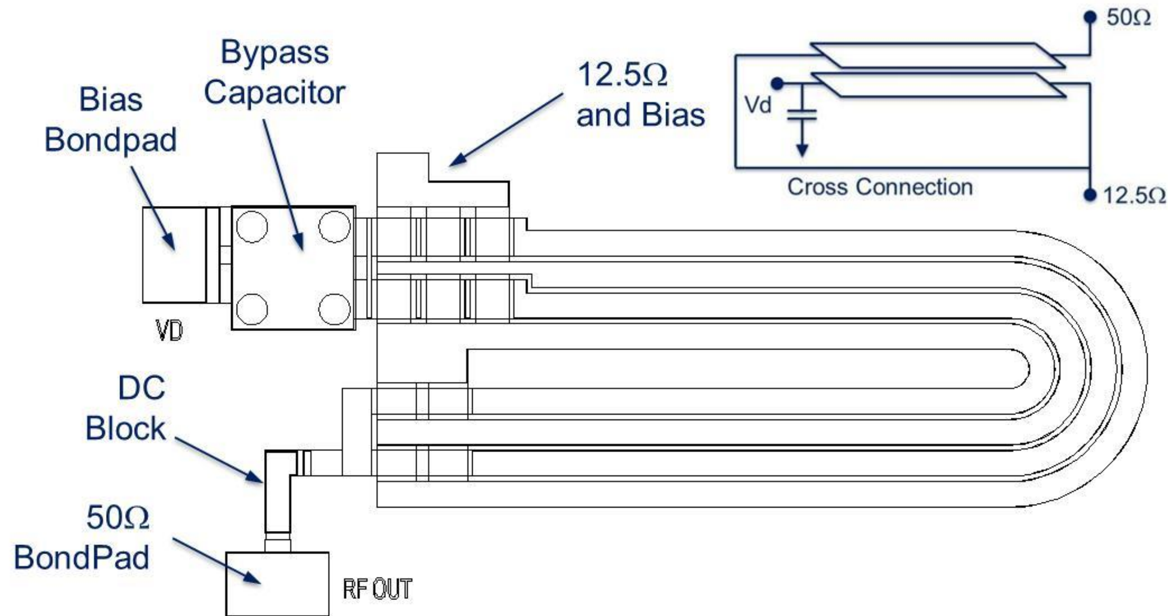
Dealing with Bode-Fano

- Reduce load impedance – Requires transformer
- Trade bandwidth for output power and realizability
- Power @ 3W/mm
  - $R_L = 50\Omega \Rightarrow 7W$
  - $R_L = 25\Omega \Rightarrow 14W$
  - $R_L = 12.5\Omega \Rightarrow 28W$



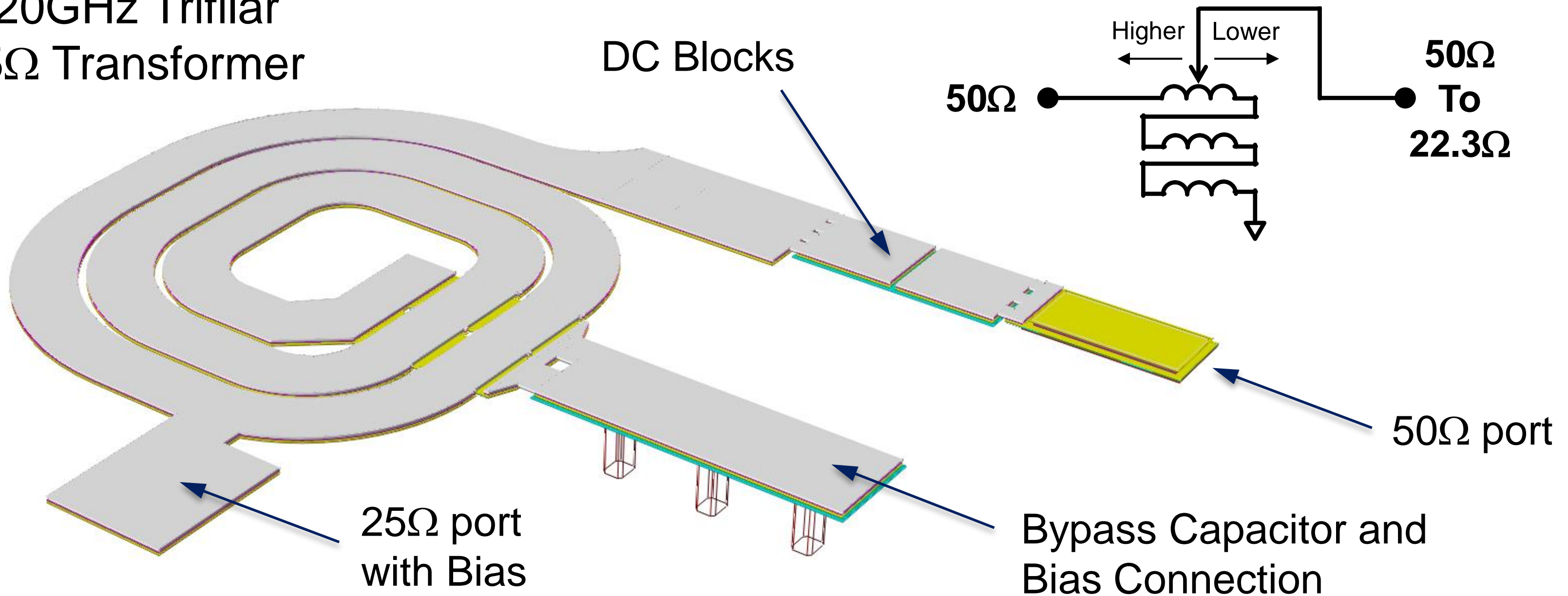
Dealing with Bode-Fano

- For a 4:1 impedance transformation (R_L=12.5Ω) a useful circuit is Ruthroff connected coupled lines [4]
- GaN on 100μm thick SiC realizations are capable of about 4:1 bandwidth [5]



Dealing with Bode-Fano

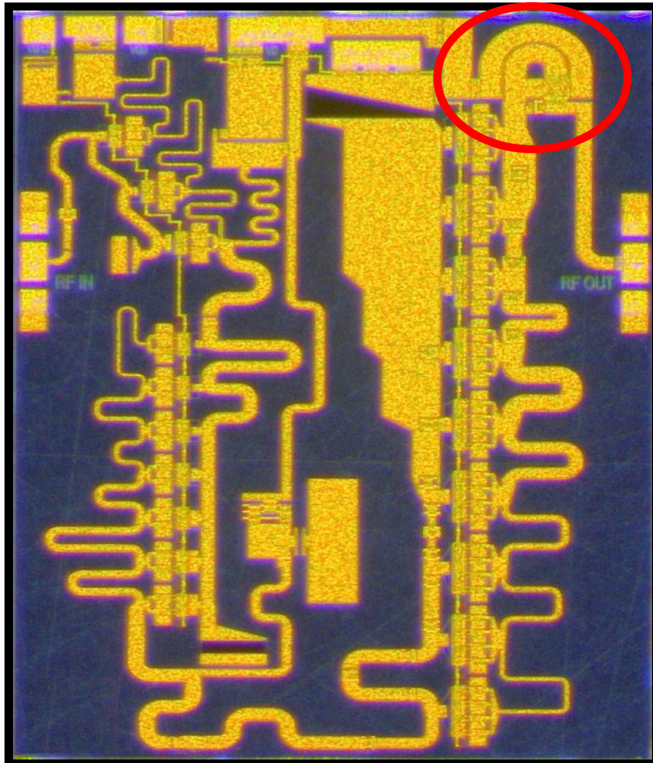
- Bandwidth can be traded for transformation ratio
- Trifilar transformer - up to 2.25:1 transformation
- Trifilar coupled lines on GaN ~ 10:1 bandwidth [6,7]



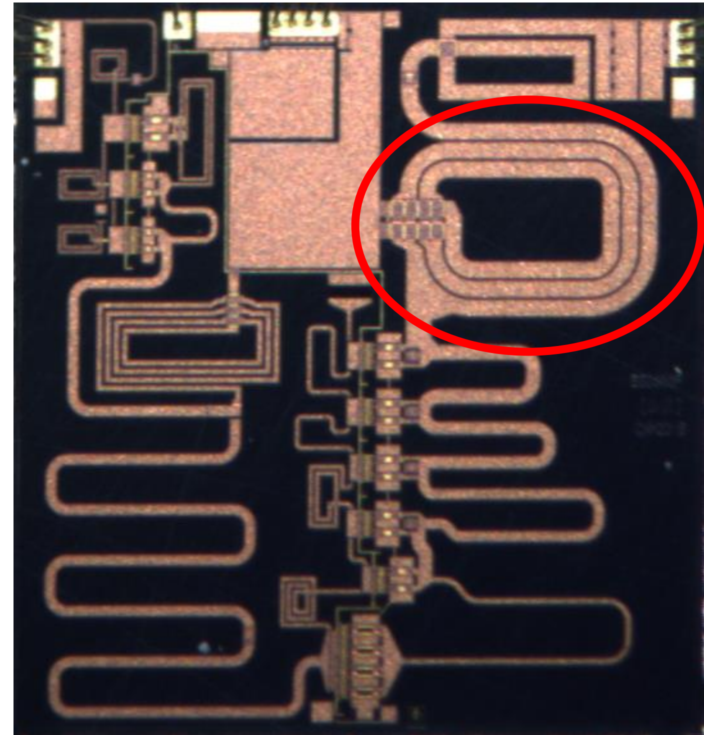
Dealing with Bode-Fano

- Transformer based NDPA MMIC examples

18-40GHz NDPA with a Ruthroff connected output transformer



1-8GHz NDPA with a Trifilar connected output transformer



Why is My Part So Hot?

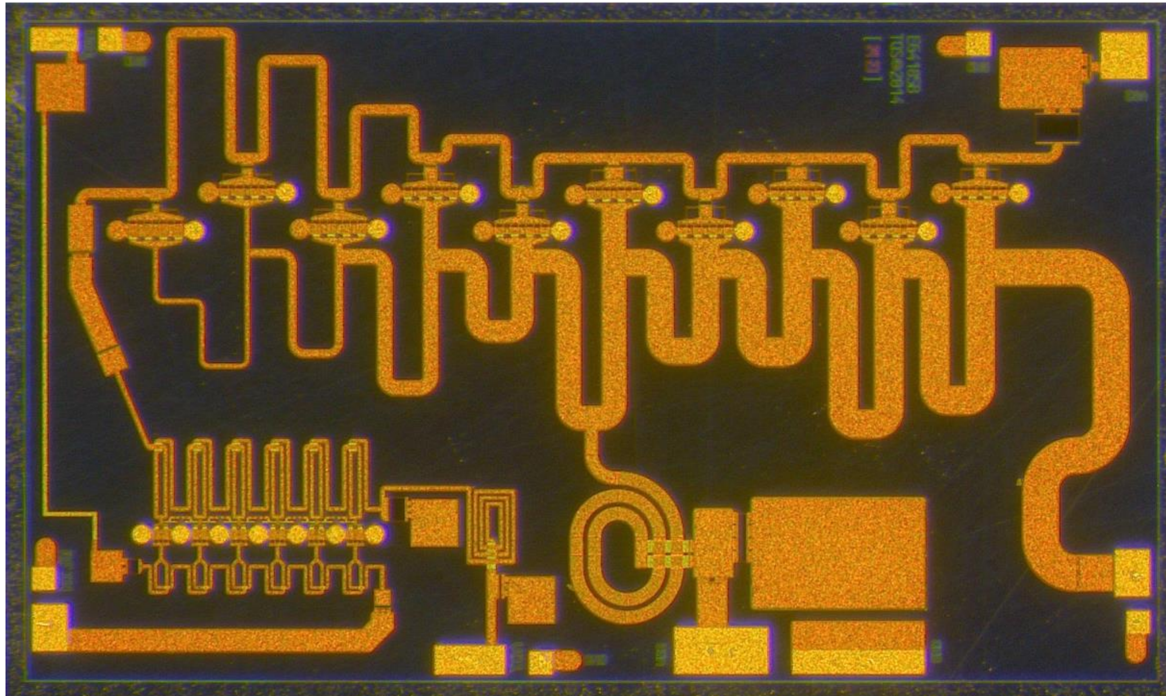
- Most GaN MMIC processes use SiC as a substrate
- Thermal conductivity of SiC exceeds that of copper
- Heat is transferred effectively to the back of the die
- The power density of GaN HEMTs 3-5X higher than a GaAs PHEMT of equal periphery
- The power added efficiency is however similar
- The problem: 3-5X more heat flux to be removed

Why is My Part So Hot?

- Thermal management burden is placed on the user
- Failure to remove heat ⇒ Higher MMIC base temp
- Today designers must practice thermal management
  - Increase gate pitch ⇒ Reduced RF performance
  - Increase cell separation ⇒ Die size and stability
  - Individual source vias (ISVs) ⇒ Die size
  - Tune for Max PAE ⇒ Reduced Power or linearity

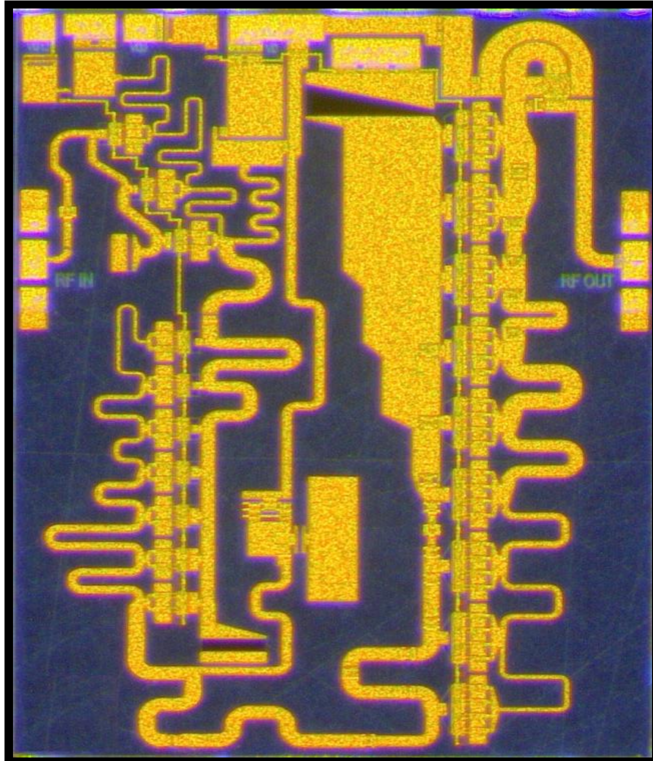
Why is My Part So Hot?

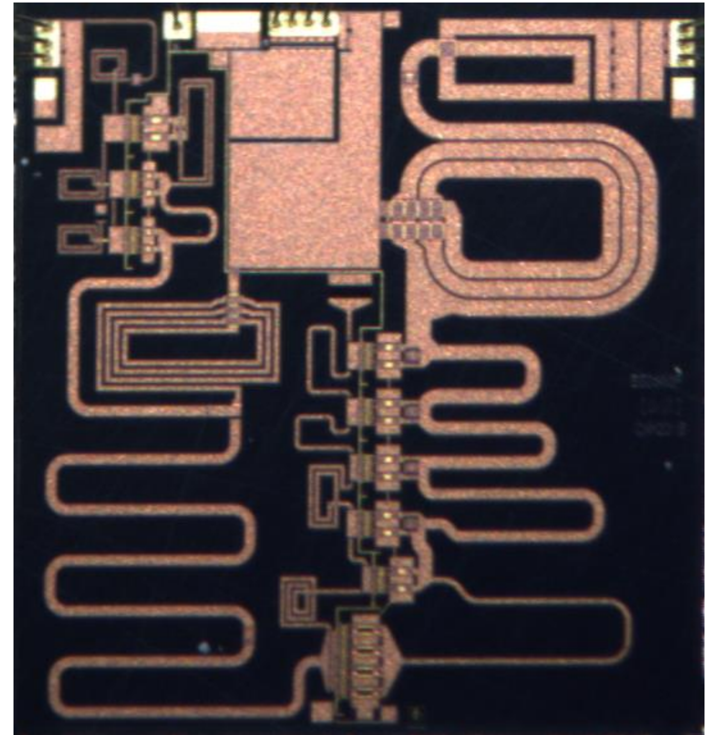
- An example of staggering the FET cells



Why is My Part So Hot?

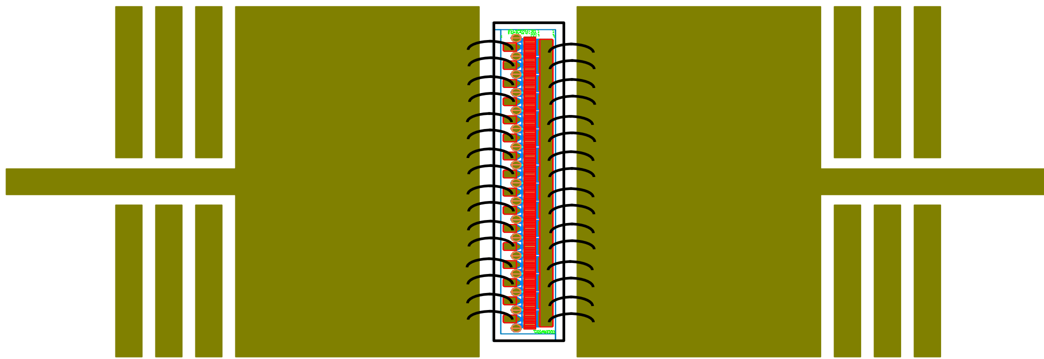
- Staggering the FET cells
- Using ISV FET cells

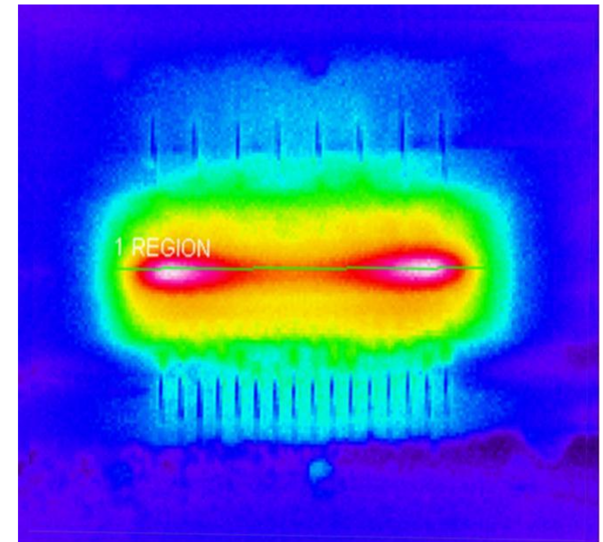




Why is My Part So Hot?

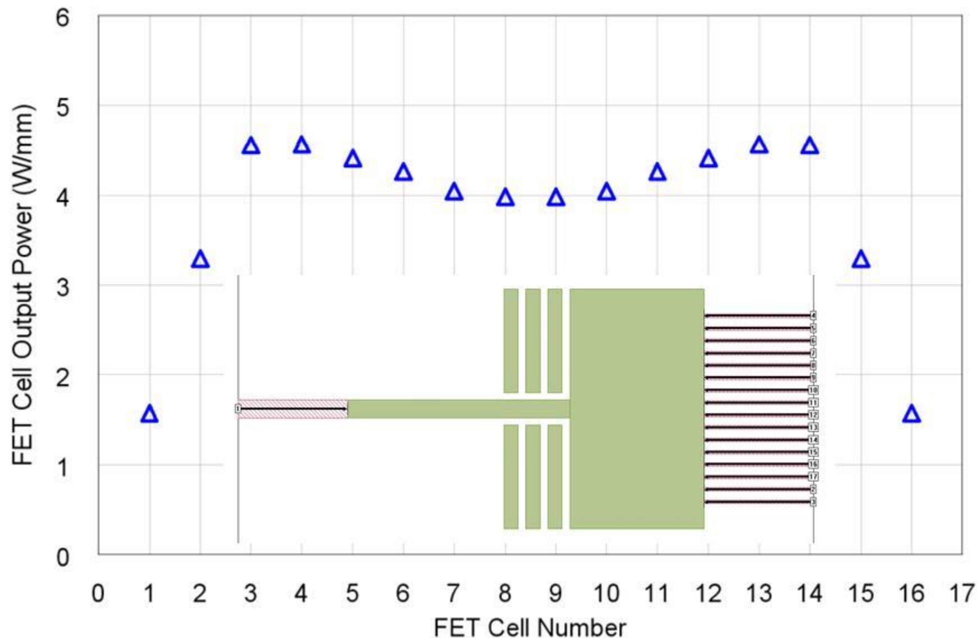
- An interesting example - power was reported power to be 1dB low for the 20mm FET die with loadpull prematch
- An unexpected temperature distribution was noted





Why is My Part So Hot?

- A detailed simulation revealed non-uniform drive and loading across the prematch connection ports
- Integrating over the 16 unit FET cells and normalizing to the maximum



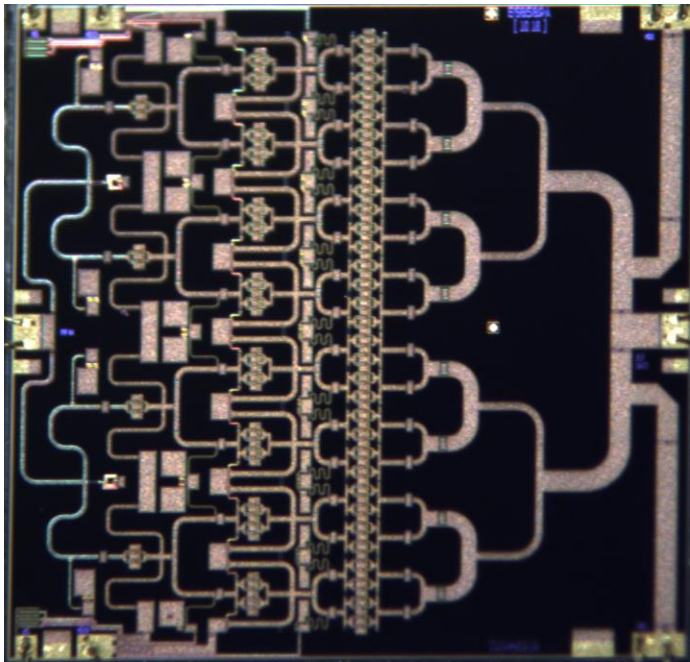
$$10\log\left(\frac{\sum_{j=1}^{16} P_j}{16x4.5}\right) = -0.9dB$$

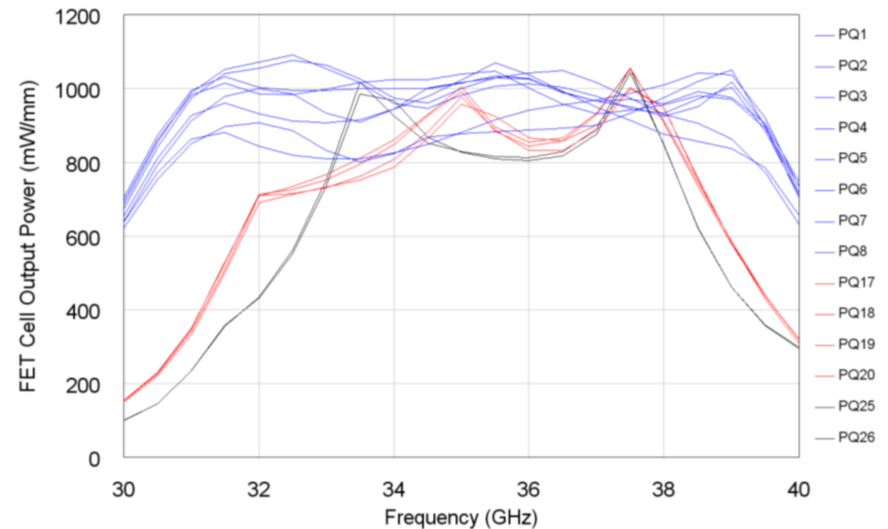
The Devil is in the Power Combining

- The odd temperature distribution for the 20mm FET is caused by asymmetries in the combining network
- Some sources of combiner asymmetry
  - Mutual inductance between parallel bond wires
  - Mode formation due to curves and bends
  - Coupling between microstrip lines
  - Sharing source vias between adjacent cells
  - Nonuniform temp. from adjacent cell heating

The Devil is in the Power Combining

- 3-stage 16-way combined GaAs Ka-band PA MMIC



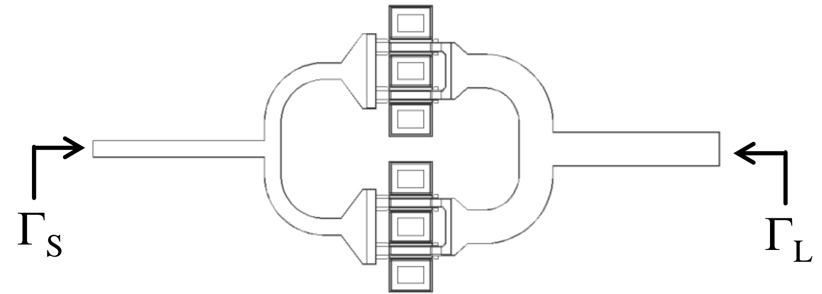


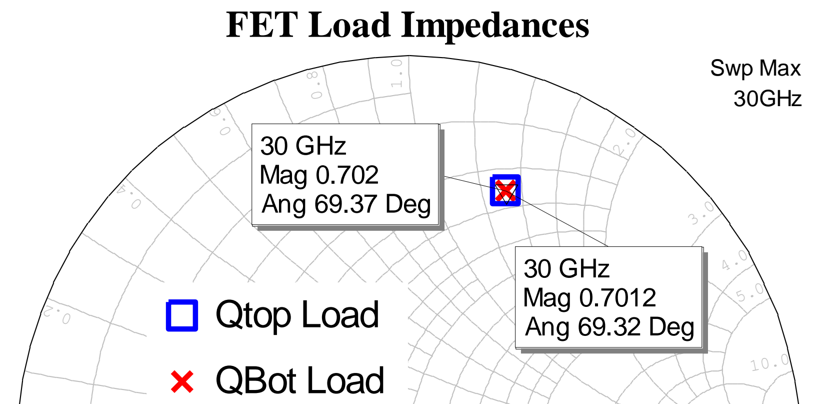
Half-Fold Symmetry Assumed

- 3rd Stage FETs
- 2nd Stage FETs
- 1st Stage FET`s

The Devil is in the Power Combining

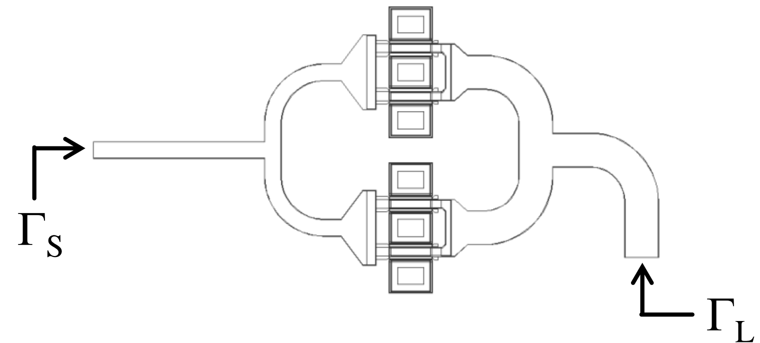
- Symmetric 2-way combiner – Power tuned Γ_S & Γ_L
  - EM Simulated Combiners
  - 4x50μm 0.15μm GaN HEMT
  - Pwr Tune Γ_L and Γ_S
  - Output Power: **31.7dBm**
  - Q_{top} Power: **3.82 W/mm**
  - Q_{bot} Power: **3.83 W/mm**

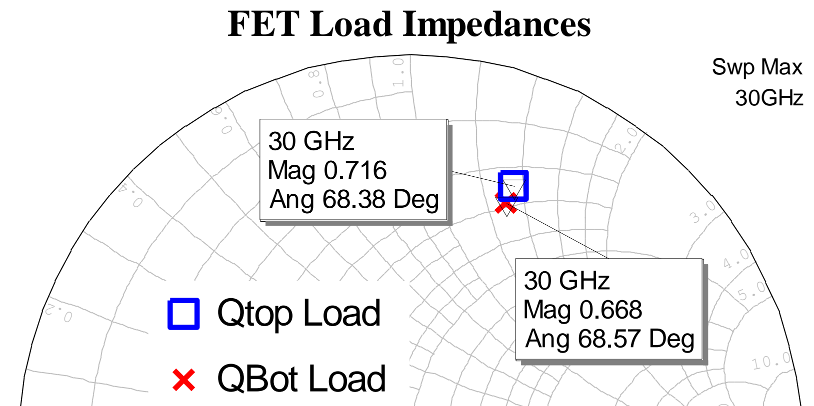




The Devil is in the Power Combining

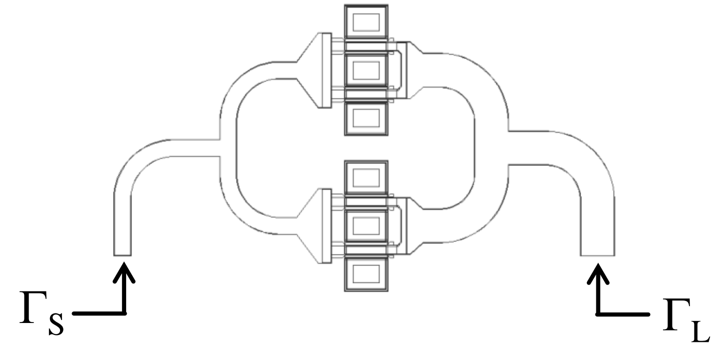
- Curved output line for connection to adjacent pair
  - EM Simulated Combiners
  - 4x50μm 0.15μm GaN HEMT
  - Pwr Tune Γ_L and Γ_S
  - Output Power: **31.6dBm**
  - Q_{top} Power: **3.74 W/mm**
  - Q_{bot} Power: **3.74 W/mm**

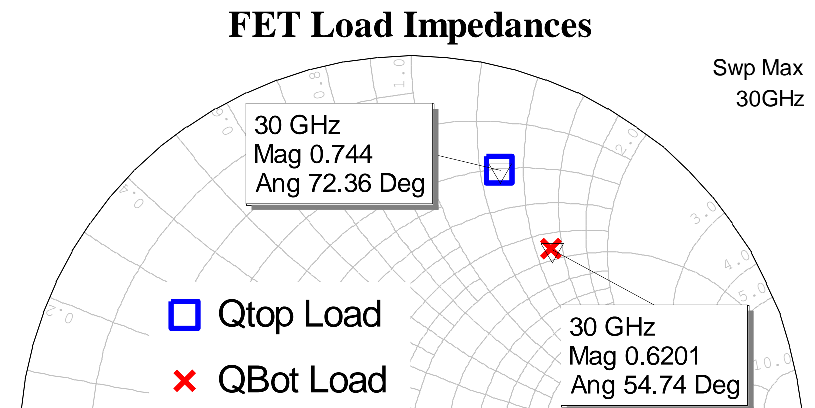




The Devil is in the Power Combining

- Curved input and output lines
  - EM Simulated Combiners
  - 4x50μm 0.15μm GaN HEMT
  - Pwr Tune Γ_L and Γ_S
  - Output Power: **30.2dBm**
  - Q_{top} Power: **2.75 W/mm**
  - Q_{bot} Power: **2.68 W/mm**



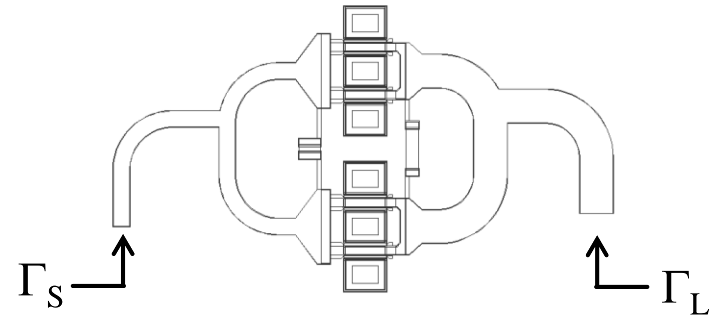


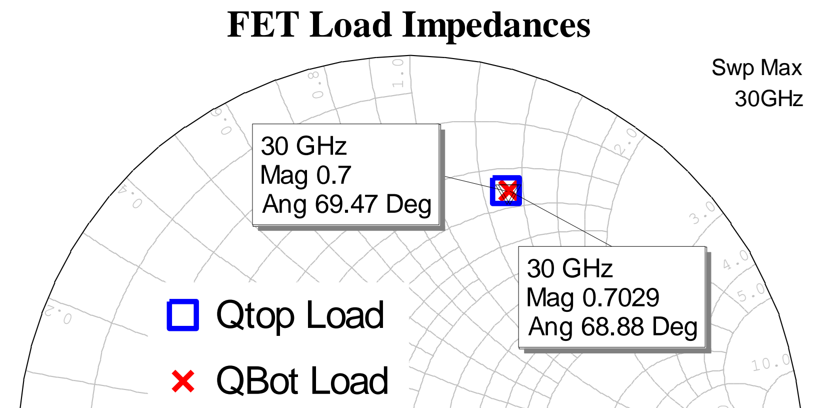
The Devil is in the Power Combining

- The output curve causes a minor degradation
- The input curve causes significant degradation
  - Current imbalance due to mode formation from curve
  - The input current imbalance is amplified by the FETs
- Fortunately this effect can be compensated for
  - Addition of odd mode suppression resistors or straps
  - Shifting the location of the tee junction

The Devil is in the Power Combining

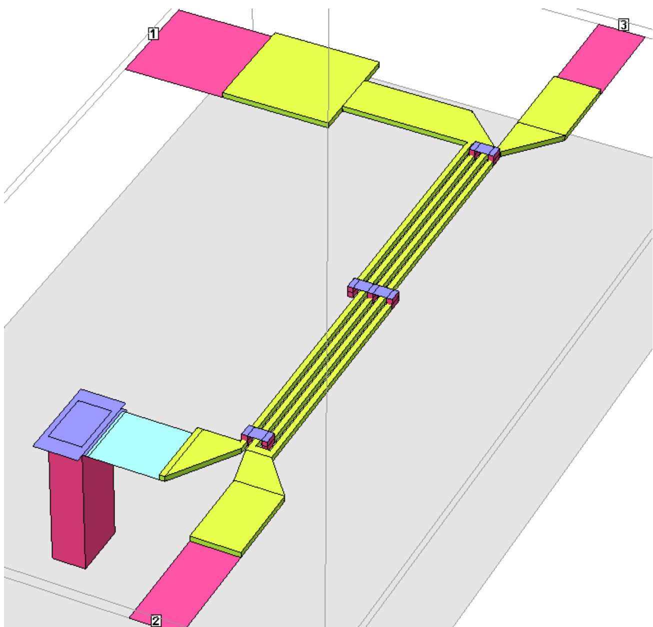
- Compensated curved input and output lines
  - Add Odd Mode Resistors
  - Offset Tee Junctions
  - Pwr Tune Γ_L and Γ_S
  - Output Power: **31.7dBm**
  - Q_{top} Power: **3.86 W/mm**
  - Q_{bot} Power: **3.78 W/mm**

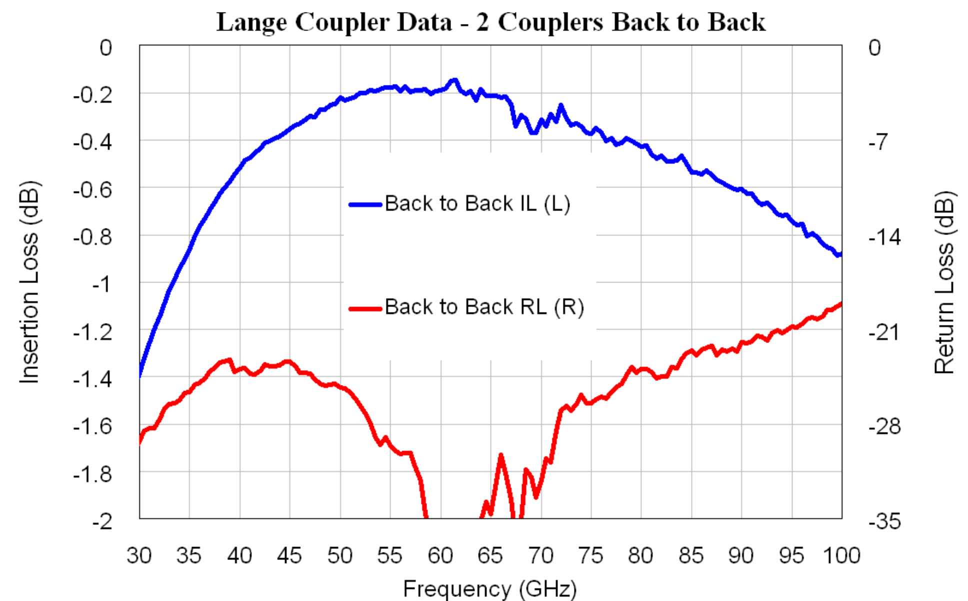




The Devil is in the Power Combining

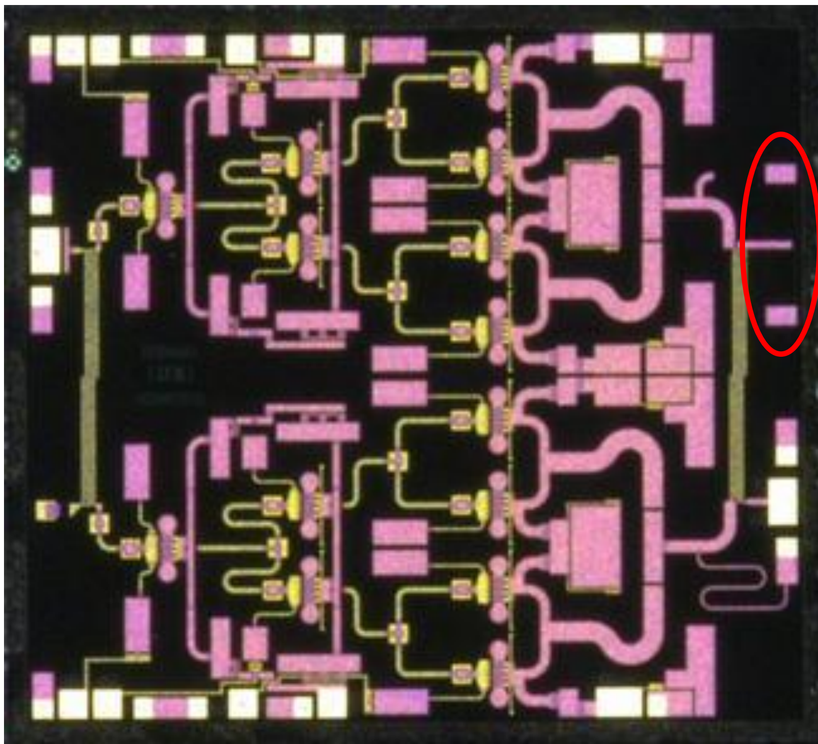
- Power combining two or more smaller amplifiers is another common approach
- MMIC Lange couplers work very well



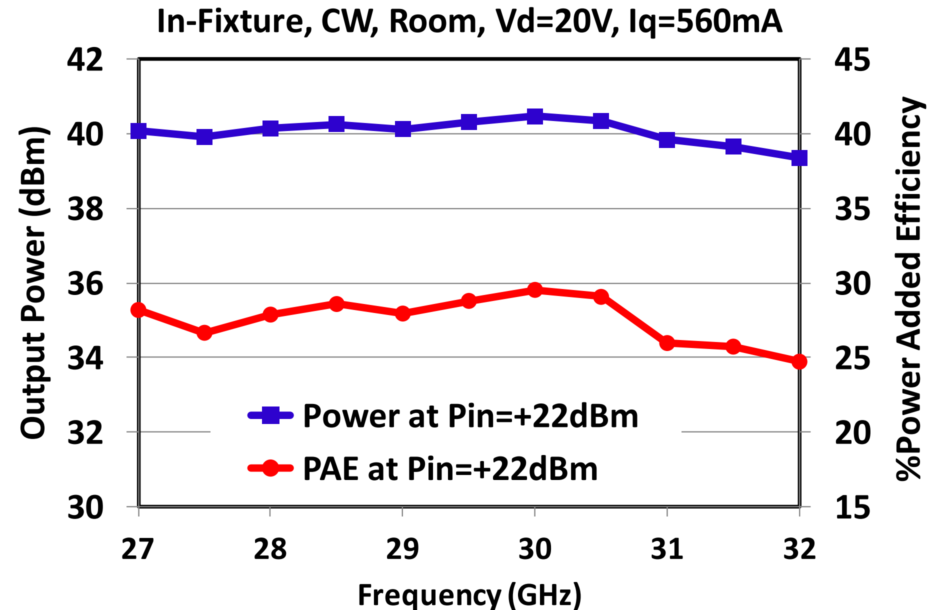


The Devil is in the Power Combining

- Ka-band GaN MMIC example – watch out for the output termination resistor!!! [8]

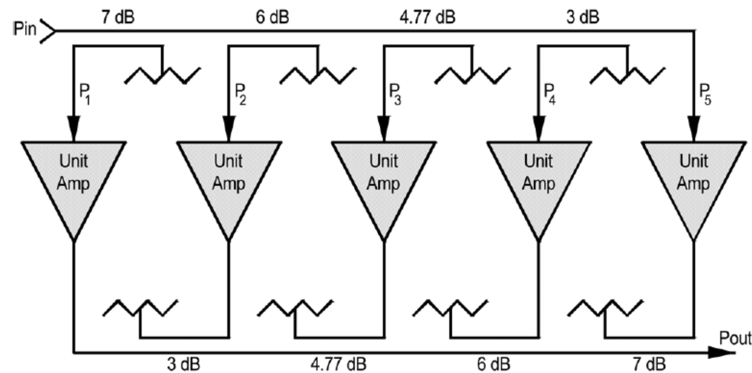


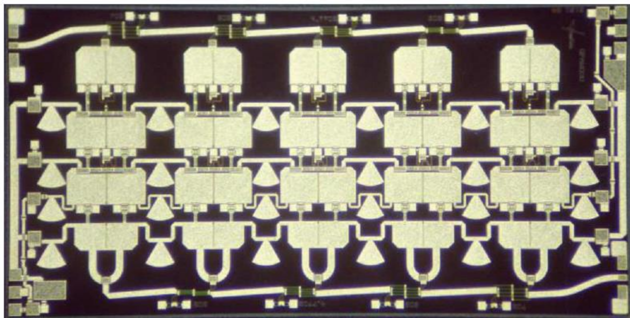
High Power 50Ω Termination (2.5W)

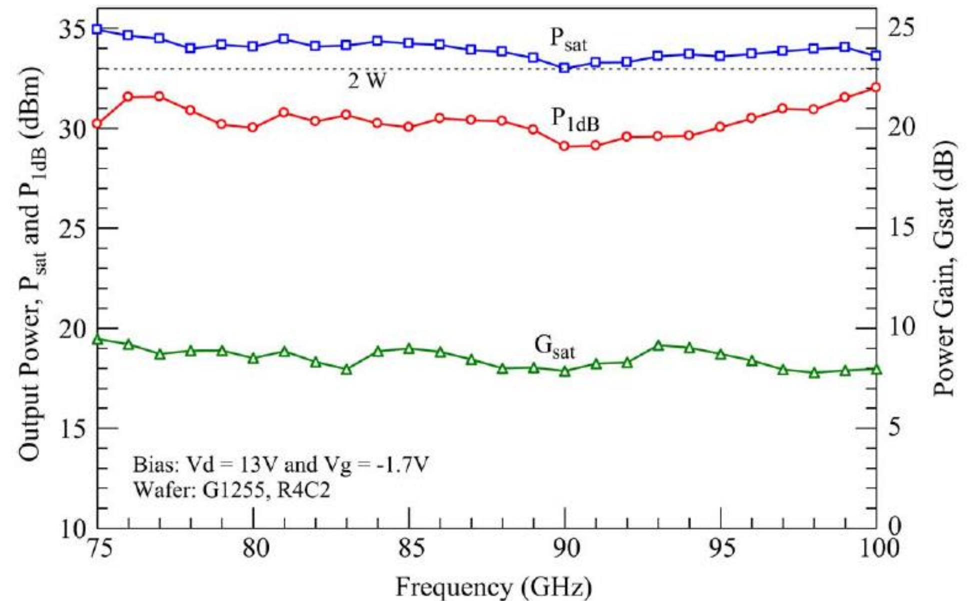


The Devil is in the Power Combining

- Recent results using traveling wave like combiners are very encouraging!! [9]





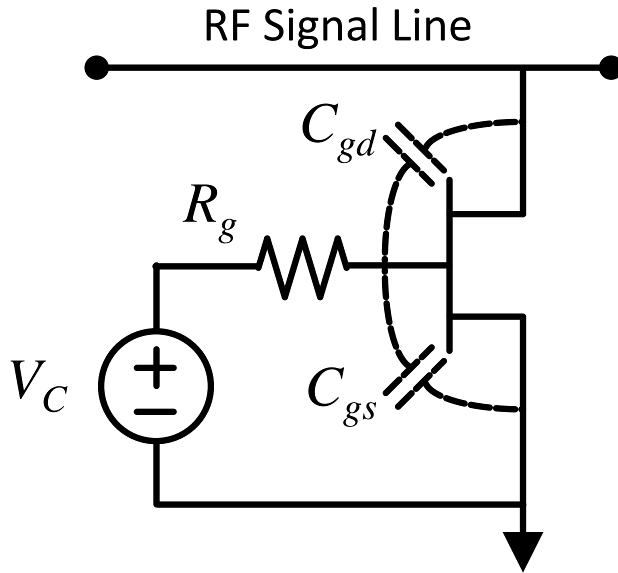


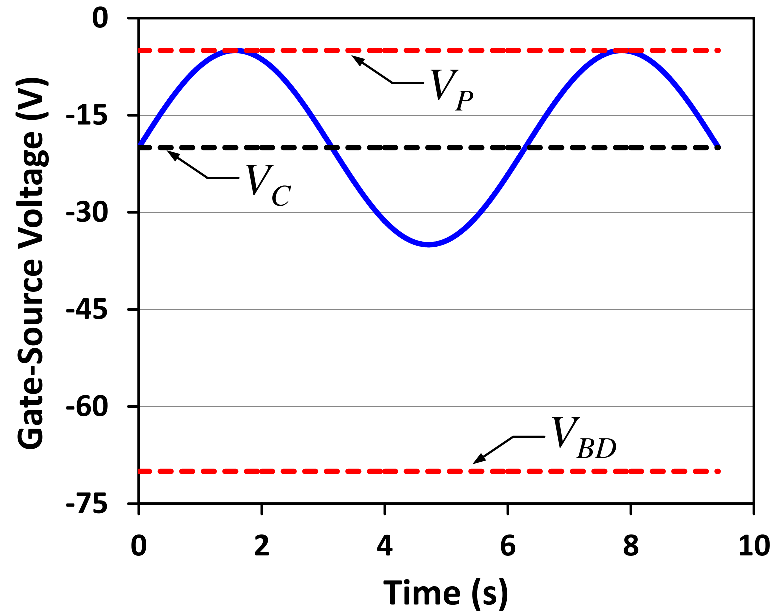
Nice RF Switch But High Control Voltage!

- GaN technology is well suited to RF control circuits
  - High breakdown voltage (V_{BD})
  - High current capability (I_{MAX})
- High control voltage is required, typically -20V to -40V
- Users struggle to build high speed driver circuits
- Lower control voltage range is often requested
- How does the circuit maintain power handling?

Nice RF Switch But High Control Voltage!

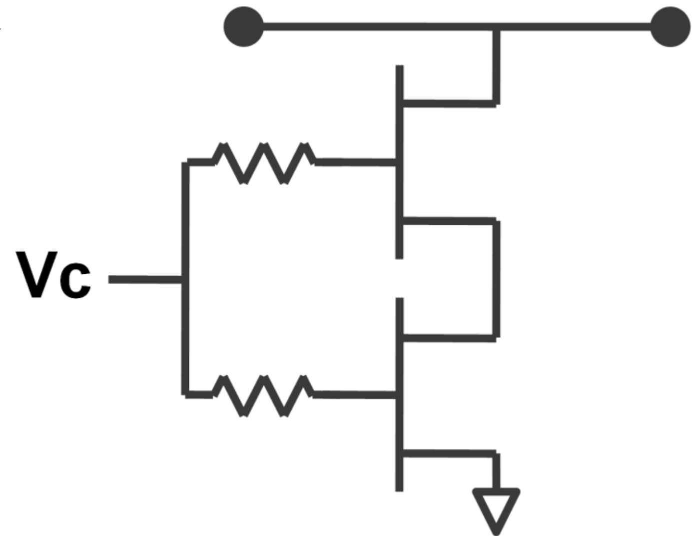
- Typical shunt switch FET circuit ($V_C = -20V$)
- Biased through high value gate resistor
- To increase power handling make V_C more negative





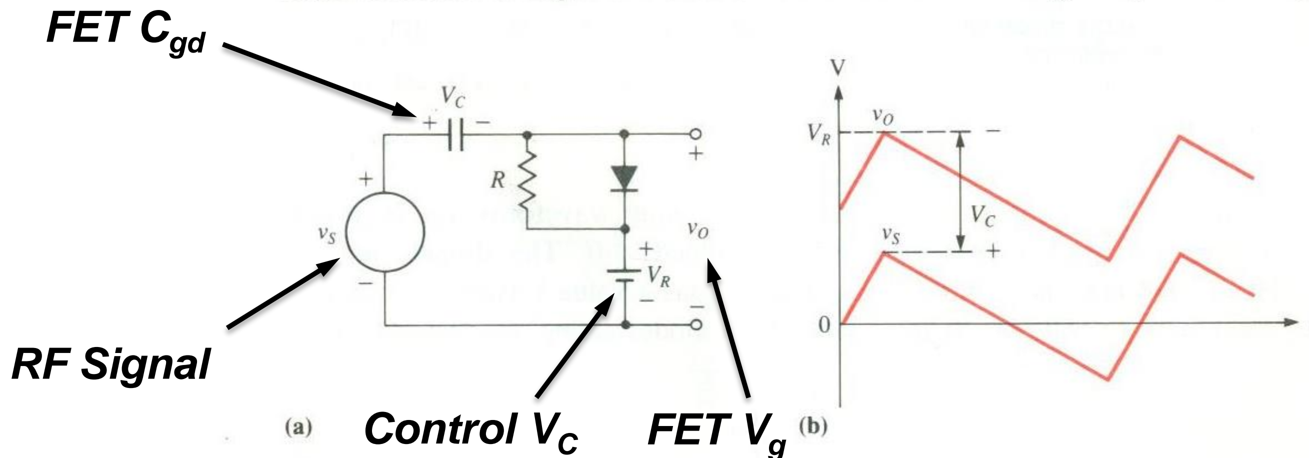
Nice RF Switch But High Control Voltage!

- A common approach is to stack "N" FET cells
  - Up to N^2 power handling increase
  - Up to N^2 increase in FET area
  - More parasitic capacitance
  - Some foundries integrate 3 gate fingers into a single channel $\Rightarrow$ "Triple Gate FET"



Nice RF Switch But High Control Voltage!

- Consider the diode clamp circuit shown below [10]

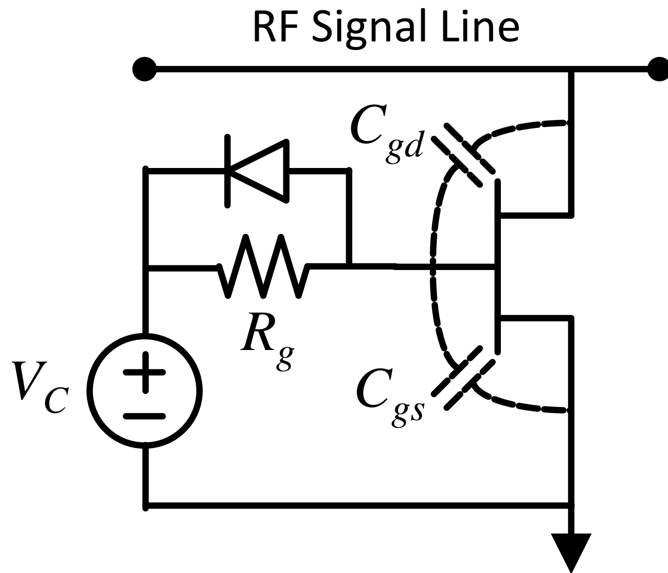

3.4 DIODE CLAMPING CIRCUITS

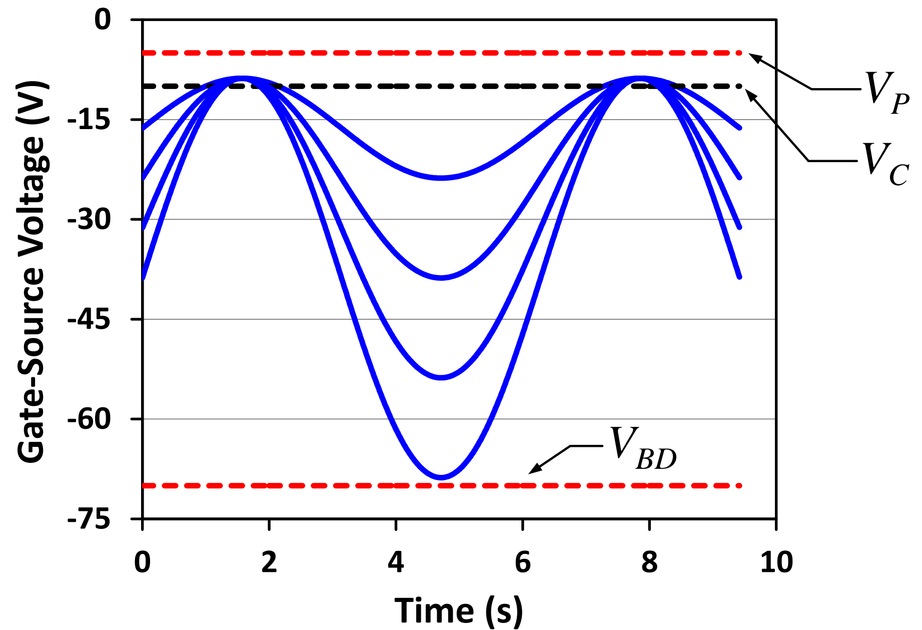
The circuit shown in Fig. 3.17(a) is known as a *clamp* because its function is to "clamp" or fix one edge of a periodic waveform (in this case the positive peak) to some reference voltage. The time constant *RC* must be long compared to the period

- Note the comment regarding the RC time constant, the clamping action will not occur at low frequency

Nice RF Switch But High Control Voltage!

- Add a small gate diode in parallel with R_g
- Schematically equivalent to a diode clamp circuit
- Now control voltage V_C can be made less negative!





Nice RF Switch But High Control Voltage!

- Simulations with & without the parallel diode

Shunt FET, Vc=-20V, 1GHz, 3GHz and 5GHz

0.0
-0.4
-0.8
-1.2
-1.6

Large Signal Loss (dB)

> 5X Higher $P_{0.2dB}$!!

Resistor Bias Circuit

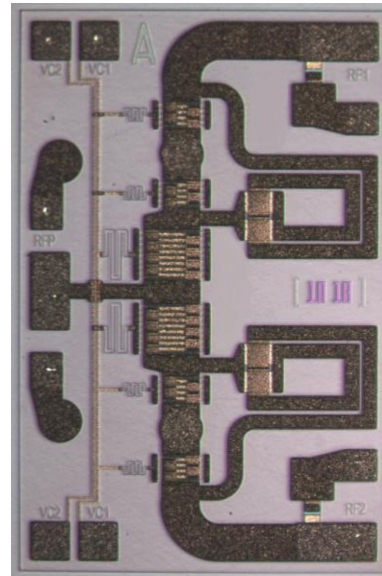
Diode Bias Circuit

20 25 30 35 40 45 50

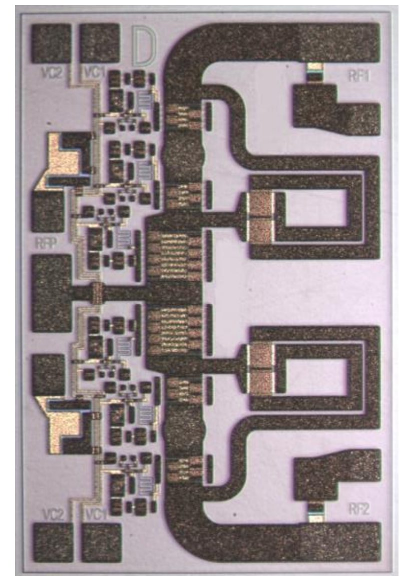
Input Power (dBm)

Nice RF Switch But High Control Voltage!

- A 40W GaN switch design was fitted with the diode circuit & processed along side the original
- 0.25μm GaN Switch FETs
  - Centered Gate
  - Single Field Plate
  - 100μm SiC
  - I_{MAX} = 0.95A/mm
  - V_P = -3.1V
  - V_{BD} > 55V



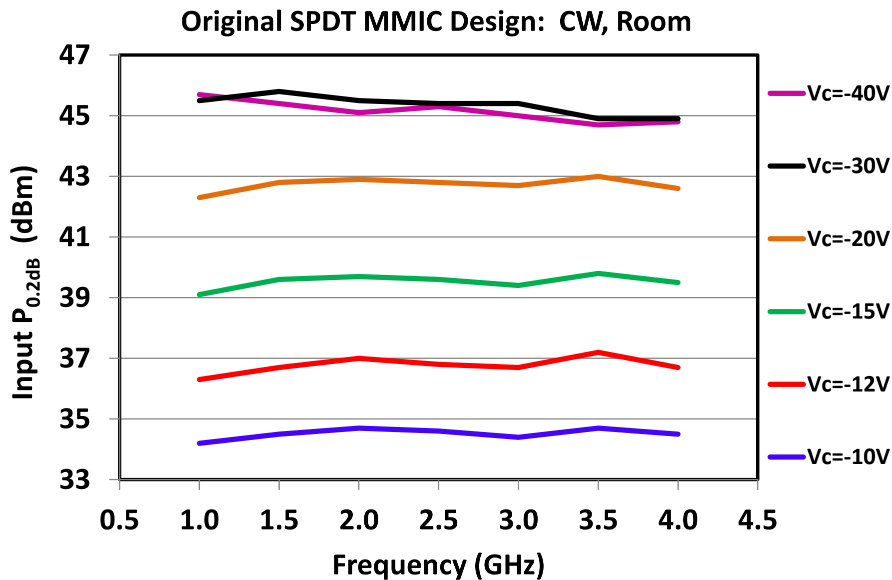
Original SPDT Switch

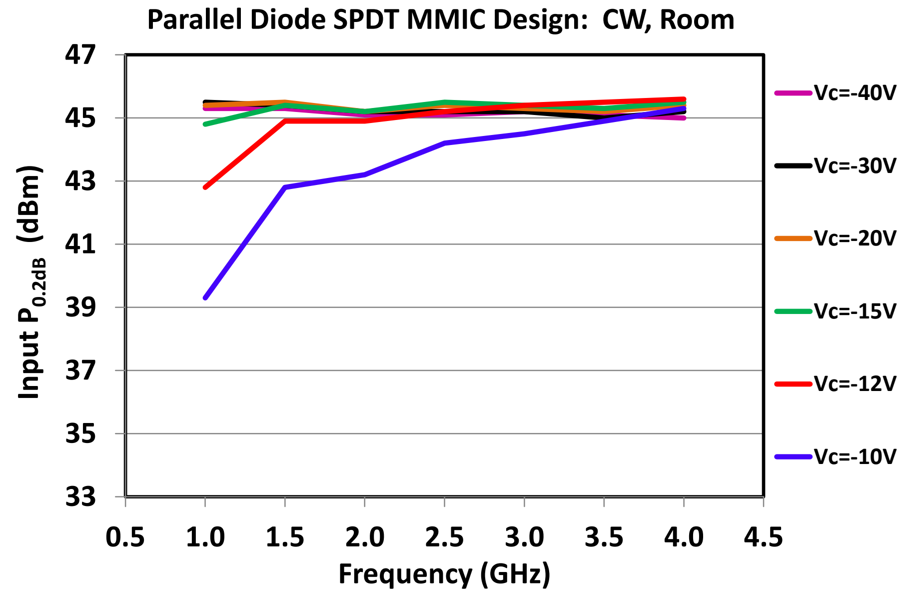


Retrofitted SPDT Switch

Nice RF Switch But High Control Voltage!

- Measured CW $P_{0.2dB}$ compression point [11,12]
  - Frequency response of clamp is evident
  - 10X increase in $P_{0.2dB}$ above 2.5GHz for -10V V_C





Concluding Remarks

- GaN MMIC technology is a real game changer
- The enabling characteristics do come with issues
- Hopefully this talk has illustrated some of the challenges associated with GaN MMIC design

Thank you for the opportunity to speak today!

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