

Quest for the Ultimate Nanoscale Silicon CMOS Transistor

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Abstract

As Moore's Law scaling of CMOS integrated circuits reaches physical limits, "beyond CMOS" technologies such as quantum dots, molecular transistors, and carbon nanotube transistors are being researched as possible CMOS replacements for the distant future. However, in the nearer term, significant technological improvements are still needed for what the ITRS Semiconductor Roadmap refers to as "Non-classical CMOS transistor structures." There are many of these 3-D and multi-gated non-classical structures which are being investigated by industry and academia.

In our work, we are collaborating with start-up American Semiconductor, Inc. to develop the new independent-double-gate (IDG) FlexFET CMOS transistor. By varying the bottom gate voltage of the FlexFET transistor, standby power can be dynamically changed over ten orders of magnitude, while the active power vs. speed tradeoff can be varied by a factor of two. Minimum sized transistors may be used to achieve ultra-low-power (ULP) in standby, while dynamic threshold adjustment is used to achieve high-performance in active.

NASA, DoD, and the aerospace industry are seeking compact, ultra-low-power electronics that are capable of reliable operation in extreme radiation environments, such as those found around Saturn and Jupiter. These Systems-On-Chip may contain not only digital processors, but MEMS microsensors, non-volatile memory, and RF communications circuits as well. FlexFET is suitable for these future spacecraft and satellite integrated circuits because it permits dynamically self-repairing circuits (compensated for cumulative ionizing radiation and hot-electron damage) which are tolerant of lifetime radiation doses in excess of 10Mrads. The double-gated mixed-signal/RF FlexFET technology is capable of integrating rad-hard communications, signal processing, and microsensor circuits on a single chip. The technology permits extremely low-power signal processing.

Some other non-classical transistors are Ultra-Thin-Body Fully-Depleted SOI, FinFET, and Vertical Pillar. We are comparatively investigating several of these new nanoscale transistors from their physics to their manufacturability, in the quest to find the ultimate nanoscale CMOS transistor structure that will permit *evolutionary* improvements of the existing worldwide CMOS manufacturing infrastructure.

Bio:



Dr. Stephen Parke earned the AA degree from Olivet Nazarene University in 1980, and the BSEE and MSEE degrees from Purdue University in 1982 and 1984, respectively. He interned with the IBM T.J.

Watson Research Center, then spent the first several years of his career with IBM Microelectronics in Essex Junction, VT, where he worked in semiconductor R&D on five generations of IBM's memory chip technologies. In 1989, he was awarded an IBM PhD Fellowship and began full-time study at the University of California at Berkeley. He fabricated and studied nano-scale silicon-on-insulator transistors, and received the PhD degree from UC Berkeley in 1993. He transferred to the IBM Semiconductor R&D Center in Fishkill, NY where he became a team leader in the IBM/Toshiba/Siemens TRIAD multi-cultural technology development project. In 1996, he left IBM for an entrepreneurial academic start-up opportunity at Boise State University. He was one of the first two ECE faculty hired in the newly created College of Engineering. He initiated several university/industry partnerships to design, fund, construct, and equip the Idaho Microfabrication Laboratory and was the director of this lab for the first few years after it opened in 1998. He became ECE Department Chair at Tennessee Tech University in 2006, where he implemented "The 20/20 Vision" for improved curriculum, research funding, lab facilities, and engagement with industry and alumni. In Fall 2010, he returned to Idaho to lead the formation of a new school of Engineering at Northwest Nazarene University, near Boise.

His research spans the areas of Multi-gated Nanoscale Silicon Transistors, Semiconductor Memories, low-power, radiation-tolerant integrated circuits, and flexible macroelectronics. His research has been funded by NSF, Air Force Research Lab, Missile Defense Agency, NASA, Wireless Systems, and American Semiconductor. He has published and/or presented 46 co-authored research papers, and is a co-inventor on 12 US patents, including the DTMOS and FlexFET transistors, which have been commercialized. He has been the primary advisor for 15 graduate students during the past eight years. He has a passion and aptitude for entrepreneurship, technology transfer and economic development activities. He is a co-founder of American Semiconductor, Inc. along with his former grad students and continues to serve on its Board of Directors. He is a registered Professional Engineer in the State of Idaho.

He has actively served the IEEE Electron Devices Society for over 15 years, for the past three years as Treasurer. He also served ten years on the IEEE EDS Education Committee, and as Chair of the Graduate Research Fellowship Committee. He was the founding Chair of the Boise IEEE EDS Chapter in 1998, which went on to win the EDS Chapter of the Year award two times. As a result of these activities, he received the IEEE Millennium Medal in 2000. He is a Distinguished Lecturer in the EDS.