

Bangalore is in a unique situation; explosive growth in silicon solution providers along with steady increase in Systems Solution / PCB players; even test capability is coming on board. The real handicap is now package knowledge and packaging capability. Package specification and selection is becoming a crucial function and let alone the design of it.

"We need to simulate not just the logic, but also the mechanical part of the design, the thermal part, and new packaging is required for new device types, such as for bio-chips." said Philips CTO Penning de Vries in his keynote speech given to a two-day conference organized by the Fabless Semiconductor Association in London recently. He went on to say it was clear that Philips' Nexperia platform approach to design would now have to step up to the SIP level. Read the full article in the URL given below.

<http://www.eet.com/news/latest/showArticle.jhtml?articleID=163101332>

We all have heard of SoC, SIP, SOP, ... and it is about time become knowledgeable in our own day to day workplace activities. We need to take the first step in the Thousand Mile journey and later walk fast, run and eventually an opportunity to lead. This definitely a Tall Order but we can educate each other and try to excel. The announcements made in this web site and future events are tailored towards that effort and looking forward to your support and feedback.

Best Regards
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B'ore CPMT Chair