ATE based System Level Test as an enabler for high volume heterogeneous 3D IC

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Abstract :

The current process for for many complex process based SOC devices includes a system level test insertion. This insertion, which can be critical to achieve acceptable quality levels typically catches faults that are only detectable in the mission mode of the device. The roadmap for most heterogeneous 3D-IC designs includes a processor die as part of the stack, along with memory and other functions. If the current test flow is employed for this type of device will radically increase scrap cost, since each processor that fails system level test will also result in scrapping good memory and other known good die. A solution to this problem is to utilize ATE with protocol aware capabilities to implement system level, mission mode testing at a wafer level, prior to device assembly. There are technical and economic challenges that must be managed to implement this strategy.

Speaker's Biography :

Gregory Smith is the Manager of the Computing and Communications Business Unit at Teradyne. He is responsible for product direction of the UltraFLEX platform and for alignment of product strategy to emerging trends in computing and communications devices. Greg is a graduate of the University of Pennsylvania and enjoys rowing in his spare time.