Through-Silicon Via Technology for Three-Dimensional Integrated Circuit Manufacturing

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Abstract:

Through-Silicon Via (TSV) is a key technology for enabling the benefits of three-dimensional (3D) integrated circuit (IC) integration, such as the reduction of package size and power consumption, and multi-functionality. 3D integration of electronic systems can be addressed in many different ways, and a large variety of TSV technologies have been proposed. All these approaches can be categorized by the position of the 3D interconnection in the interconnect hierarchy and fall into two categories: 3D-TSV interconnects at the level of on-chip electrical wiring and 3D-TSV interconnects at the bond pad level. This first type (3D-Stacked IC/3D-IC) typically uses approaches that integrate the TSV processing in the wafer fab and are generally referred to as via-first or via-middle TSVs.

This presentation will focus of recent achievements at imec in the field of via-middle TSV fabrication and it subsequent processing integration into advanced node CMOS devices.

Biography:

Yann Civale received his MSc degree from the Ecole Centrale Marseille in France in 2004 and his Ph.D degree in microelectronics from Delft University of Technology, in the Netherlands in 2008. In 2008, Dr. Civale joined imec in Leuven, Belgium where he has been involved in several projects related to 3D TSV integration and the author/co-author of more than 30 technical publications in the field. As lead integration engineer, his current focus is on high density 3D TSV interconnections and associated integration into advanced technologies node devices.