The Process Characterization of Insulated Au-Flash PdCu For The Challenging Wire Bonding Applications

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Abstract

With the success of developing insulated wire bond recipe in the conventional wire bond process for ball grid array (BGA) and quad flat package (QFP). The development of insulated wire bond process is moving further to explore into other areas of bonding applications with potential challenges on insulated Au-Flash PdCu wire.

At the same time, the characterization process was perform on the insulation coating thickness in order to establish an optimize insulation thickness. The thickness of the insulation layer becomes more critical when it apply into wider areas of bonding applications. In fine pitch and critical wire bond process, any variations to either the insulation coating layer itself or the bonding processes used could affect the overall stability and bondability of insulation wire. Series of assessments were performed to assess the performance of various insulation thicknesses in terms of wire bondability, electrical insulation and wire bond quality. Eventually, a new insulation thickness window in terms of break down voltage (BDV) was established that able to fulfill all the requirements.

One critical potential area of study for insulated wire would be in Ultra-Low-Loop (ULL) application down to 2mils loop height. Since at such low loop height, the critical loop bendings would occur at the bonded ball neck region which is subjected to the high energy effects during EFO sparking, this could result in regional peeling-off of the insulation coating on the wire due to the partial breaking down or weakening of the insulation layer and bending stresses incurred at the ball neck region. Thicker insulation coating may complicate ULL applications further as this would mean sharp bending through thicker coating material with little ductility. Uneven wire surface contact with the capillary internal walls also sets in and thus resulted in the regional insulation material peeling as illustrated in the paper. Various loop profiles were also studied to assess for any improvements to the ULL application.

Another challenging application of insulated wire would be in conventional stitch bond on bump process. The bumped ball smoothing action could result in excessive accumulation of insulation material at the capillary tip, thus causing fast-clogging of the capillary which means an increase in the production costs due to a shorter capillary life-span. This is even so when the insulation coating layer gets thicker. At the same time, insulation material residue that was left on the bumped ball surface prior to the 2nd bond adhesion could result in poor bondability and workability of the stitch bond on bump process.

Besides, the flexibility of the insulated wire which enables the criss-crossing wire layout has been fully adopted into a universal substrate concept for the ball grid array (BGA) packaging. The idea is to use one standard substrate design and caters to multiple devices / products. In this case, insulated wire bonds are assigned freely as device specific trace routings in substrates are not required. This idea able to reduce substrate design cycles and at the same time lowers the substrate unit cost. The development performed by NXP with the use of insulated wire has demonstrated good wire bond process feasibility without any major process issue.

In summary, the development on various wire bond technologies with insulated wire has widen the application of insulated wire. Detailed wire bond process optimization and characterization successfully improve the feasibility of new insulated wire bond technology. This indicates another great leap in the insulated wire bond application.

Introduction

Insulated Cu wire is a potential solution for ultra fine pitch wire bonding, offering good electrical isolation between the wires when they are in close proximity [2]. However, there are still a lot of opportunities for insulated wire to expand its application. As we try to fan out the insulated wire usage to broader applications, it is important to still keep in mind that cost savings is still the ultimate aim. The cost benefits that come with substrates standardization and package design flexibility must not be lower than the additional cost incurred due to greater bonding processing challenges. As such, these projects explore further the applications potential of the insulated wire and identify the areas that need continuous improvement and more extensive bonding process optimization.

Fig. 1: An application example with 2-tier and close wire proximity bonded with X-PdFlash
Insulated Au-Flash PdCu Wire Coating Thickness Assessment

The organic coating thickness is a critical parameter to determine the overall performance of the insulated wire. Thicker coating thickness offering good electrical isolation between the wires when they are in close proximity. The increase of coating thickness however, will induce wire bondability issue. The optimization of insulation coating thickness is the balance between electrical insulation and wire bondability performance and it is crucial especially for finer wire. Currently there is no direct method to measure the insulation layer thickness, but an indirect way was adopted which involves the measurement of insulation layer breakdown-voltage (BDV). Series of assessments were performed on Heraeus 0.7mil insulated X-PdFlash wire with different coating thickness ranged from (T-12)V to (T+32)V BDV to study the performance of various insulation thickness in terms of wire bondability, electrical insulation and wire bond quality. The study was performed on NXP’s TBGA electrical functional test vehicle with the reprogram of signal wires looping parameters in order to create physical wire contact between the adjacent wires at the wire span region. Wire bonded samples were later subjected to various output measurements including stitch pull strength and open short test (OST) to assess both the bondability and electrical performances. During sample wire bonding, no issue were encountered for all the wire sample with different insulation thickness except the thickest coating sample of (T + 32) V BDV. Massive NSOP problem were encountered during (T + 32)V BDV wire sample bonding. Analysis indicates that the NSOP was induced by the abnormal free air ball (FAB) problem. The improper formation of FAB is the result from the thicker coating which act as a barrier, preventing sufficient EFO energy to completely melt down the wire.

The stitch pull strength measurement for other coating thickness samples were taken as shown in Fig. 2. Based on the analysis, there is no significant difference of stitch pull strength of wire sample with different coating thickness ranged from (T-12)V to (T+20)V BDV. Since all the samples were wire bonded with the same wire bond parameters and no process issue such as NSOL and short tail encountered during the sample build, it indicates that the coating thickness window of (T-12)V to (T+20)V BDV has no significant effect on the 2nd bond performance. Further increase in the coating thickness however might cause the FAB formation and NSOP problems.

The OST test results for insulated wire with different coating thickness ranged from (T-12)V to (T+20)V BDV are shown in Fig. 3. As expected, the OST short failure rate increase with the reduction of coating thickness. A drastic increase of electrical short failure rate was observed when the coating thickness is below (T)V. On the other hand, no electrical short failure was encountered for coating thickness at (T+14)V BDV and beyond. Based on the assessment results, the coating thickness need to maintain as minimum as (T+14)V in order to obtain an effective electrical insulation for the wire to get into contact. Further assessment will be required to assess the bondability for coating thickness beyond (T+20)V in order to establish the manufacturing working window of +/- 5V for the coating process. At the same time, Heraeus is currently optimizing the wire coating process in order to improve the coating thickness consistency. The idea is to maintain a lower coating thickness window for a better wire bond process bondability and slower coating residue build up rate on the capillary, while maintaining a sufficient electrical insulation capability for the wire in close proximity.
Insulated Au Flash PdCu Wire Ultra-Low-Loop Feasibility Study

With the fast development of electronic devices in terms of functional complexity and dimension shrinkage, Ultra-low-loop (ULL) profile currently is being extensively applied in wire bonding area. However, ULL still remains challenging for gold or copper wire bonding in some applications. Wire mechanical properties are specifically targeted for different wire sizes such that it is able to achieve consistently low loop height in mass production, without over-stressing the neck during loop bending motions. Besides, wires with shorter heat affected zone (HAZ) are more suitable for ULL applications. During FAB formation, wire in HAZ recrystallizes, forming larger grains in wire, which makes wire less strong. During ULL formation, much of bending occurs in HAZ, so shorter HAZ is critical in providing lower and consistent ULL without neck damages.

As far as X-PdFlash wires are concerned, though there is no clearly defined HAZ for Cu or PdCu wires, but the additional insulation coating layer acts as a ‘barrier’ during loop bendings since there is very little ductility in the insulation material. Scratch or flaking surface damages on the insulation layer due to bending stresses will undermine the insulation capability of the wire. Hence in this study, various factors during looping were evaluated on the insulation layer surface damage severity.

0.7mil X-PdFlash wire produced by Heraeus was used, together with KNS Iconn LA wire bonder. ULL looping profile ULL4 was adopted. Under SEM inspection, obvious wire neck stretch could be seen as shown in Fig. 4 (top image), which was caused by over-stressing at the neck region due to insufficient wire pay-out during looping formation. Once more wire pay-out was added-in during Fold motion, such stretch mark was successfully eliminated as shown in Fig. 2 (below image). Loop height target of 2mils with minimal height variation was also attainable with two different BDV wires under this setting as shown in Fig. 5.

Fig. 4: Loop neck with (top) and without (below) neck stretch

Fig. 5: 2mil ULL loop height attainable with 2 different BDV wires

However under above settings, insulation layer scratches and flake-offs on the wire span surface were clearly observed under optical scope inspection and were also confirmed under SEM as shown in Fig. 6. The scratching or flaking is caused by the frictional drag between the capillary tip inner walls and wire surface along XY movement during looping formation. To avoid such insulation layer damage, Fold Z motion was increased. Once Fold Z was increased, scratches were greatly reduced. However it did not have obvious effect in reducing the flaking. So as long as the XY movement during looping formation exists, this frictional-drag causing the flaking is almost unavoidable.

Therefore in subsequent optimization studies, the Fold XY was totally removed, indicating that from base movement until the end of Fold Z movement, no XY movement was involved. Table 1 show some critical looping parameters applied without XY movement. The increase of negative loop factor has kept the loop height to around 2mils. Under
all settings studied, slight insulation layer scratches were still seen, but have been significantly reduced, as shown in Fig. 7.

<table>
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<tr>
<th>LOOPING PARAMETER</th>
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<tr>
<td>Fold XY</td>
<td>¯m</td>
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<td>Fold Z</td>
<td>Um</td>
<td>50</td>
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<tr>
<td>Loop factor</td>
<td>mil</td>
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Table 1: Critical ULL profile looping parameters optimization

Fig. 7: Significant improvement on the wire span surface before (left image) and after (right image) looping parameters optimization

Besides looping parameter optimization, the effect of other factors such as insulation layer thickness and capillary geometry were also studied. Two 0.7mil X-PdFlash spools with different insulation layer thicknesses in terms of BDV value were evaluated to compare differences in wire surface scratch/flaking severity. Higher BDV means thicker insulation layer and thus more difficult for the wire to make proper bendings to achieve the required loop shape and loop height. Under the looping parameters listed in Table 1, it can be seen that for thinner insulation layer with (T)V BDV, only slight flakings are observed, but for thicker insulation layer with (T + 14)V BDV, more severe flakings are seen, as shown in Fig. 8. To further relief the frictional-drag between the capillary inner walls and the wire surface, other alternatives need to be explored which includes having a dual IC capillary if the slight scratch/flaking as observed were to be totally eliminated.

Insulated Au-Flash PdCu Wire Stand-Off-Stitch-Bond Feasibility Study

Besides the challenge in ULL application for X-PdFlash, another potential challenge would be in die-to-die bonding application. Stand-Off-Stitch-Bond (SSB) process in K&S bonder is conventionally used in die-to-die bonding. The very first step for a successful SSB bonding is to achieve good and consistent bumped balls. The top surface of bumped balls must be smooth and large enough for subsequent stitch bond adhesion. Separation Height, Bump Height and Smooth Distance are some critical bump parameters during optimization. Slightly lower bump height could help make bump plateau larger; and slightly longer smooth distance could help make bump surface smoother. Bump images from these settings are shown in Fig. 9, and setting 1 was applied for bump in subsequent bonding test. Bump Ball formation with the conventional bump smoothing action potentially causes fast build-up of insulation coating material on the capillary tip and eventually fast-clogging the capillary. Insulation residue on the Bump Ball surface due to the smoothing action may cause difficulty in the stitch bond adhesion onto the bumped ball top surface and hence resulted in low stitch pull strength on bumped ball and very little stitch pull remains as shown in Figs. 10 and 11.

Fig. 8: Wire Span Surface ‘flaking’ severity differences between (T)V BDV(left image) and (T+14)V BDV(right image)

Fig. 9: Lower bump height and longer smooth distance in setting 1 was used which resulted in a larger and smoother bump plateau

Fig. 10: Stitch pull strength on bumped ball
Further bump smoothing optimization making use of ‘double smoothing’ improves slightly the minimum stitch pull on bump, as this process totally flattens the ‘bump plateau’ and minimizes the ‘plateau walls’ insulation contact surfaces (as indicated in Fig. 12) with the stitch bond. However the ‘double smoothing’ process means there is more capillary tip contact with the insulation layer while performing the smoothing action and so insulation build-up rate will be faster as well.

Also, a thicker insulation layer would most probably imply that even more insulation residue would reside on the bumped ball top surface and since the capillary tip smoothens over a relatively larger volume of insulation material, the build-up rate on the tip would be faster and hence shortens the capillary life-span. This would reduce the cost benefits that insulation wire has to offer on applications involving SSB process.

Series of the improvements were implemented which include the substrate material, substrate manufacturing process, design configurations, wire bond top plate design etc in order to realize the wire bond process of universal substrate. Wire bond parameters optimization was performed using 0.7mil insulated X-PdFlash from Heraeus and earlier TBGA insulated wire bond parameters were used as the baseline for the optimization. Initial wire bond assessment shows positive results with no process issue such as non stick on pad (NSOP), non stick on lead (NSOL) and wire short tail problems encountered. Both ball bond and stitch bond formations are good without any abnormality as shown in Fig. 15.
The assessment were repeated with the current production Pd coated Cu wire in order to compare the wire bond performance of 2 wire types especially on the 2nd bond performance. The stitch pull strength measurement indicates that the universal substrate has similar stitch pull strength performance as the earlier TBGA insulated wire bond. The minimum stitch pull strength passed the spec requirement for 0.7mil wire. While comparing with the Pd coated wire, a reduction of about 25% stitch pull strength can be observed on the universal substrate insulated wire as shown in Fig. 16. Further assessment will be performed in order to verify the wire bond recipe robustness with higher volume sample run as well as the package stress reliability performance.

Acknowledgments

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References


Conclusion

Besides the conventional wire bond process on BGA and QFP packages, a significant progress has been made by the insulated wire on other wire bond process applications such as the ULL, SSB and universal substrate. Through the various process, material and machine /tooling optimization, those applications are feasible with the use of X-PdFlash insulated wire. Further process fine tuning will be performed in order to establish the high volume manufacturing capability. One of the key factors to determine the robustness of insulated wire bond recipe on these new areas of applications is the insulation coating thickness. Through the wire coating assessment, we understand that the coating thickness needs to maintain at certain minimum thickness in order to obtain a complete electrical isolation. Thicker insulation, however will induce problems such as flaking during ULL bending, lower stitch pull in SSB process, faster capillary residue build up rate and improper FAB formation in severe case. Further optimization work currently in progress which target to reduce the coating thickness variation. This will help to maintain a lower coating thickness window for a better wire bond process bondability, while maintaining a sufficient electrical insulation capability for wire to be able to get into contact. Through these relentless efforts to improve both the insulated wire and its bonding process, more and more insulated wire bond application will be realized and feasible for high volume manufacturing environment.