Modeling Investigation of the Influence of Polycrystalline Grain Size on the Electrical Characteristics of Polysilicon Diode and Resistor

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Abstract
Grain size is a critically important aspect of polycrystalline materials. To realize a high performance polysilicon diode and polysilicon resistor, it is important to understand the deviation of the grain size, and the effect on the electrical properties of polycrystalline material. The correlation of polysilicon grain size with the polysilicon deposition temperature and the dopant type was studied through process simulation, and the effect of grain size variation on electrical performance of polycrystalline diode and resistor was modeled and simulated through device simulation. The electrical behaviours of the polycrystalline diode and polycrystalline resistor in term of reverse breakdown, capacitance and resistance have been investigated and shown to be a function of the grain sizes.

1. Introduction
The polycrystalline material is composed from small crystallize surrounded by grain boundaries, which act as carrier traps and affecting the transport of charge carriers. Grain size is a critically important aspect of polycrystalline materials, the barriers between grains can be different and the electrical properties of polycrystalline material is related to the grain boundaries and grain size.

One of the application of polycrystalline material is polysilicon diode. The polycrystalline silicon is also noted as polysilicon. The diode built in polysilicon is fully process compatible with a majority of processes. Being insulated from the substrate, it does not have any vertical parasitic current path unlike the silicon bulk diode, this makes polysilicon diode more suitable elements for stacking to enable the electrical current and voltage parameters to which the circuit is important to enable switching elements and current rectifying devices in semiconductor integrated circuits, thus the Darlington effect is avoided when excessive diodes are stacked together. [1] Hence it is suitable for Electrostatic-Discharge (ESD) protection device.

In addition to the use of transistors and diodes as switching elements and current rectifying devices in semiconductor integrated circuits, it is also quite common that electrical circuits have resistors incorporated into the designs and fabrications. Commonly, a resistor structure within an integrated circuit will provide an electrical load which assures proper operation of the circuit under the electrical current and voltage parameters to which the circuit was designed. Resistor can be made with polysilicon and it can be lightly doped to enable a high ohmic resistor. Due to the low doped nature, the resistance of the high ohmic polysilicon resistor is more sensitive to grain growth and the effect of the grain size, hence it was chosen to be a device of investigation in this studies.

The polysilicon is usually deposited with Low Pressure Chemical Vapor Deposition (LPCVD) by decomposition of Silane (SiH4) at low pressure. The deposition are limited to the temperature range of 540C to 640C because at higher temperature gas phase reactions will result in rough, loosely adhesion, and silane depletion. On the other hands, if the temperature is too low, the deposition rate would be too low for practical applications [2]. Grain growth and grain size can be maximized by amorphous silicon deposition followed by crystallization anneal or by recrystallization techniques. Changes in the structure of the polycrystalline silicon depend on the annealing conditions, and the initial structure formed during the deposition and dopant present in the polycrystalline silicon during annealing. The initial structure is determined by the deposition conditions, primarily by the deposition temperature.

This paper presents the correlation of polysilicon grain size with the LPCVD process parameters in term of deposition temperature and the dopant type by employing process simulation. The polysilicon grain growth and diffusion models were used to simulate the growth of the grain size. The grains in the polycrystalline material are assumed to be oriented as columns that extend through the wafer. The structure was characterized by the average grain size in the lateral direction. The grain size were examined and visualized through the simulation visual tool. The effect on grain size on electrical performance was established through device simulation.

2. Simulation Model
Typically, the polysilicon is deposited with LPCVD in the range of 540C to 640C. But in this simulation studies, the deposition temperature was simulated at 600C and at elevated temperature at 800C and 1000C respectively, in order to enhance the effect of the grain size and establish obvious correlation between the grain size and the electrical characteristics of the polysilicon diode and polysilicon resistor.

Figure 1 below shows the schematic diagram of the polysilicon diode and polysilicon resistor used in this modeling investigation. A polysilicon layer of 300nm was deposited over a thick Field Oxide (FOX) layer and fully isolated to silicon bulk. A blanket implant with low doped phosphorus N- was first implanted onto the polysilicon, which formed the center intrinsic region of the diode. The low doped high ohmic polysilicon resistor was also formed by this N- implant. The anode of the diode was made with high doped Boron P+ implant, else the cathode was fabricated with high doped Arsenic N+ implant.
Polysilicon has a micro-structure of small crystalline regions called grains. They are separated by grain boundaries which occupy certain spatial volume and are connected to form a complex network. The texture and morphology of the grain structure depend on the deposition conditions and on subsequent thermal treatment in which recrystallization can occur. Impurities inside the grain will diffuse differently than those in the grain boundaries. Dopant will also transport through grain and across grain boundary interfaces. In order to study the effect of impurities or dopants on grain growth, the polycrystalline film was doped insitu with high dopant concentration at 1 x 10^{21}atom/cm^3 during the LPCVD process, and the dopants of interest were boron, phosphorus and arsenic. The polysilicon deposition was also chosen to study the temperature effect on the grain growth.

The process simulation was performed through Taurus TSUPREM-4 which is a computer program for simulating the processing steps used in manufacturing silicon integrated circuits and discrete devices. [3] The simulated polycrystalline structure is shown in figure 2. The structure of polysilicon, FOX and bulk silicon are illustrated and the simulated grain size can be seen increasing linearly from the bottom of the polysilicon layer to the top of the polysilicon layer.

Device simulation was performed with Taurus MEDICI device simulation tool. It is a powerful device simulation program that can be used to simulate the behaviour of semiconductor devices. [4] The current-voltage behaviour of the polysilicon resistor and the current-voltage and capacitance-voltage behaviour of the polysilicon diode were the device characteristic of interest in this studies.

3. Result and Discussion

When polysilicon is doped, the grain growth rate is altered as a function of impurity doping concentration. Impurities have 2 opposing effects on the grain boundary migration rate. They might increase the vacancy concentration by shifting the fermi level and increase the grain boundary migration rate. Or impurities might retard the grain boundary migration due to segregation at grain boundaries and cluster formation in the grains.[5] In this studies, 4 groups of doping condition were compared, namely the undoped polysilicon, the phosphorus doped polysilicon, the arsenic doped polysilicon and the boron doped polysilicon at 1 x 10^{21}atom/cm^3 dopant concentration each, with similar polysilicon deposition temperature at 600C.

The behavior of dopants in polycrystalline material is strongly influenced by the boundaries between crystalline grains. Dopants atom tends to segregate from the interior of a grain to the boundaries, which provide paths for rapid diffusion. The rate of segregation depends on the rate of grain growth, while the number of diffusion paths along the boundaries depends on the grain size. Experimentally, it has been found that arsenic and phosphorous enhance grain growth in polysilicon in varying degrees. The presence of the n-type dopant in the layer enhances the recrystallization process. The grain growth is attributed to silicon self diffusion across the grain boundaries. As for boron, it has little effect on grain growth. This can be seen from the simulation result shown in figure 3. It is shown that the p-type doping with boron has a negligible effect on the recrystallization process, the grain size of boron doped polysilicon is seen to overlap with the grain size of undoped polysilicon with negligible change in grain size. The grain size in the arsenic and phosphorus doped polysilicon changed by several micron meter (um) with reference to the grain size of the undoped polysilicon. The presence of phosphorus and arsenic change both the grain boundary energy and silicon self diffusivity, which leads to a change in grain growth activation energy.
Grain structure is also sensitive to grain growth temperature. The effect on the grain growth with the polysilicon deposition temperature at 600C and elevated temperature at 800C and 1000C was simulated and the result is shown in figure 4. Practically, the polysilicon deposition temperature will not go up to these elevated temperature range, it was only for simulation purpose.

The result shows that the grain size does not increase significantly from 600C to 800C, but the grain size increase by several um with the deposition temperature at 1000C. The simulated grain size was in the range of 0.2um at 600C to 1um at 1000C. This seem to match with what was reported by Lysacek in his experiment that the primary recrystallization of the polycrystalline silicon layer was observed during high annealing temperature in the range from 900C to 1150C. [6] There is a change in morphological structure at high temperatures, the grain boundaries try to migrate, and grain growth is occurring. The average of grain size of polysilicon increases during high temperature processing. The grain size is strongly dependent on temperature. The grain size data from the process simulation on polysilicon deposition temperature was then used to simulate the effect of grain size on the electrical characteristics of polysilicon diode and polysilicon resistor, with higher temperature denote larger grain size. Figure 5 shows the effect of grain size on the Current-Voltage (IV) behaviour of the polysilicon resistor of which the resistance is derived from. Figure 6 shows the zoom in of the IV curve.

The zoom in IV curve reveal a minor resistance difference between 600C and 800C, with lower resistance at 800C compared to 600C, which matches with the degree of increase in grain size obtained from the earlier process simulation. From the IV curve, it is noticed that bigger grain size allowed for higher current which translates to lower resistance. The resistivity of polysilicon layer is defined by the number of free carriers and their mobility, which depends on the impurity atom diffusion behaviour and structural changes initiated by heat treatment. Larger grain size permits lower electrical resistivity as the resistivity is influenced by the changes in the microstructure due to grain growth. The resistance is inversely proportional to grain size.

Figure 7 shows the reverse breakdown behavior of the polysilicon diode with respect to the grain size. The leakage current is shown in logarithmic scale at y axis, and the reverse breakdown voltage is indicated at x axis. Breakdown occurred once the maximum electric field exceeded the critical electric field. It is shown that breakdown is lower with higher grain size. The electrical properties depends on the properties of grain boundaries, and the reverse breakdown voltage is roughly proportional to the number of grain boundaries and inversely proportional to grain size.
Another key electrical parameter guiding the usage of a diode is the capacitance, as it determines the operating frequency. The capacitance of the diode with respect to grain size was simulated as shown in Figure 8. From the simulation result, the capacitance seems to be lower with higher grain size. This result is yet to be verified on experimental wafers.

If the polysilicon deposition temperature is varied too much, the impurity incorporation behaviour and the grain size of the polysilicon might vary too much, leading to difficulty in controlling the device characteristics, as shown from the simulation result.

As the devices are used at the field application at various temperature condition, the electrical characteristics were also simulated at various temperature range at 25C, 90C and 150C. Figure 9 to Figure 11 show the response of resistance, reverse breakdown voltage and capacitance with respect to temperature at the large grain size condition. These 3 electrical parameters exhibit the positive temperature coefficient, with the increase in value as the temperature increases. The same positive temperature coefficient is observed when the grain size is lower. With this observation, it shows that the size of the polysilicon grain does not alter the temperature coefficient of the devices.
4. Conclusions

We have simulated the impact of dopants and temperature on the properties of the polycrystalline silicon layers specifically on the grain size. And the effect of grain size variation on the reverse breakdown voltage and capacitance of the polysilicon diode, and the resistance of the polysilicon resistor were modeled and simulated through device simulation, and have been shown to be a function of the electrical properties of the grain size.

References