Prediction of Electrostatic Discharge (ESD) Soft Error on Two-Way Radio Using ESD Simulation in CST and ESD Immunity Scanning Technique

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Abstract
Electrostatic Discharge (ESD) can cause ESD soft error failures such as radio reset. In this paper, a new methodology is developed to assess ESD risk at system level prior to PCB fabrication using 3D simulation. A Poynting vector theorem is used to calculate the accumulated incident power received by the sensitive IC which is identified through ESD immunity scanning test. The time-weighted-average peak power is to establish the criteria for ESD risk causing the soft error failure. Results from this paper will help electrical engineer to predict potential ESD reset failure at system level instead of the previously trial-and-error procedure.

I. Introduction
The ESD event creates high voltage and current in nanoseconds range. ESD transfers high energy to circuit device through moving the charge (electron) at lowest impedance path. Any electronic component which is located along this path is very susceptible to ESD, leading to a temporary or permanent damage of the system. The damage to a component is determined by device’s inability to withstand the energy level involved.

The electrostatic problem is divided into two categories
[1]:
(a) Component damage – This is a permanent damage. It is usually hard to see by eye and requires test instrument to observe the damage from outside. By doing decapsulation, it is possible to see the physical damage inside the IC. This is called hard failure. During ESD event, the circuit may be partially damaged but it still fully functional. However with repeated ESD from external source and internal heating of component, the damaged component is finally resulting in lasting failure to the circuit operation.
(b) Function disruption – This is classified as a temporary failure with no damage to component. It is also referred to as the soft failure. The failure is caused by energy disturbance to the circuit. The failure can be recovered by resetting the equipment manually.

To identify the susceptibility level of components to ESD damage, three types of ESD models are developed according to ESD Association (ESDA) and Joint Electron Device Engineering Council (JEDEC). They are (i) the Human Body Model (HBM), (ii) the Machine Model (MM) and (iii) the Charged Device Model (CDM) [2]. However, these models are unable to ensure the component does not cause a failure at system level. To achieve better product reliability, the ESD sensitivity level at system level is tested using test method called IEC 61000-4-2 standard. The test is completely inadequate from HBM test that only focused more on ESD robustness at component level. The ESD requirement at system level is higher than component level. Fig 1 shows the requirement of HBM and system level.

![Fig 1: Different level of ESD robustness required for HBM and system level [3]](image)

The biggest challenge faced by electrical engineer today is to find a method identifying the possible root cause of soft error failure. Upon the design completion of very complex PCB, the actual radio is directly built for product testing, which includes ESD system level test. The ESD test is measured based on the radio conditions (PASS and FAIL) after ESD zapping. ESD failure is detected during the prototype and re-occurred on the next prototype. The issue is investigated based on individual knowledge and experiences to identify the possible root cause of failure. Various approaches were identified to tackle the issue including changes on mechanical parts and circuit design. Without any tool to guide the investigation, different approaches were executed at different stages to determine significant improvement in order to meet product specification (at ±8kV and ±15kV for contact discharge and air discharge respectively). This condition requires more prototypes to overcome the issue.

Without knowing the root cause of the failure, the electrical engineer tends to over-test the radio by multiple pulse zappings to the externally exposed contact. This can overstress the components and potentially destructive the radio. There is possibility that internal circuit of IC break down in CMOS configuration. This creates doubt of what is actual discharge voltage (failure level) causing the radio loss function or upset. The effort of fixing the issue can be a nightmare and causes the failure to occur again and again.

Today finding a new method in estimating potential ESD failure at design stage remains a challenge. Hence a new approach using the system diagnostic technique such as ESD immunity scanning and 3D simulation is done to predict ESD soft error failure at design stage. This paper illustrates the detail of methodology of ESD soft error prediction.
2. Methods

The aim of the paper is to eliminate the process of fixing the failure through conventional method which practices “trial-and-error”. This method implements a temporary solution and can create failure occurrence in future. Thus the elimination process is done by detecting potential ESD soft error failure delivered to ESD sensitive component in 3-dimensional (3D) simulation. By referring to the limit, electrical engineer is able to assess potential ESD failure during PCB design and provides early solution for ESD robust design in order to prevent the ESD failure occurring after actual radio being built.

The background of this paper is to apply the dosimetry principle in determining the energy dosage received by object that exposed to the electromagnetic (EM) fields according to the formula below [4]:

\[
S_{av} = \frac{1}{T} \int_{0}^{T} S(t) \, dt 
\]

(1)\[
S_{av} = \frac{1}{T} \sum S_{i} \, t_{i} 
\]

(2)

\( S_{av} \) – Average Poynting vector
\( S_{i} \) – Value of samples Poynting vector over time
\( t_{i} \) – Sampled time. During \( t_{i} \) the value of \( S_{i} \) must be different from zero and remain constant for the whole \( t_{i} \)

By applying the concept of dosimetry, the exposure of the sensitive IC to ESD in the electromagnetic field is used to calculate the time-weighted-average power density (Ptwa). This is the same as Sav above. Ptwa is calculated as a cross product of electric field strength (E) and the magnetic field strength (H) using “Poynting vector” in equation (7). This is illustrated in Fig 2 where the Poynting vector (incident power) is generated from 15 positions of field probe on IC pins. The average incident power over a given time period is calculated using equation (9) to express the power density in units of W/m².

At time \( t_{n} \),

\[
\vec{P}_{n} = \vec{E}_{n} \times \vec{H}_{n} 
\]

(1)\[
|E_{N}| = \sqrt{E_{Nx}^{2} + E_{Ny}^{2}} 
\]

(2)\[
|H_{N}| = \sqrt{H_{Nx}^{2} + H_{Ny}^{2}} 
\]

(3)\[
P_{n} = |E_{N}| \cdot |H_{N}| \cdot \sin \theta_{N} 
\]

(4)\[
P_{n} = \sum \xi_{n} P_{N} = \sum \xi_{n} |E_{N}| \cdot |H_{N}| \cdot \sin \theta_{N} 
\]

(5)

\( |E_{N}| \) – Magnitude of electric field
\( |H_{N}| \) – Magnitude of magnetic field
\( E_{Nx} \) – Electric field dominates at X axis
\( E_{Ny} \) – Electric field dominates at Y axis
\( H_{Nx} \) – Magnetic field dominates at X axis
\( H_{Ny} \) – Magnetic field dominates at Y axis
\( P_{N} \) – Incident power density delivered to sensitive IC pin \( N \)
\( P_{twa} \) – Time weighted average power density
\( P_{n} \) – Incident power density
\( \Delta t_{n} \) – Time interval between sampling (ns)
\( t_{n} \) – Actual time at different probe positions

Time Weighted Average Power Density

\[
Ptwa = \frac{\sum_{n=1}^{N} P_{twa} \cdot \Delta t_{n}}{t_{n}} 
\]

(6)\[
Ptwa = \frac{P_{1} \Delta t_{1} + P_{2} \Delta t_{2} + \ldots + P_{n} \Delta t_{n}}{t_{n}} 
\]

(7)

\( \theta_{N} \) – Angle between \( E_{N} \) and \( H_{N} \)

At the end of the paper, a limit of allowable time-weighted-average power density distributed to IC is defined. This is able to predict ESD failure if the power density close or above the limit. The methodology is divided in two stages: (i) 3D simulation and (ii) ESD measurement. This is shown in Fig 3. The methodology is conducted according to the process flowchart as in Fig 4. The following items are the key processes of methodology in completing the paper.

(a) To identify ESD susceptibility level of radios with verified ESD pulse in different radio condition.
(b) To have area of focus in modeling and simulation in identifying a parameter change as criteria of ESD failure.
(c) To perform a parametric study in considering a parameter for ESD failure detection in simulation.
(d) To establish a criteria for ESD soft error prediction. The process is separated into four parts
(a) Validate ESD pulse as per IEC 61000-4-2 standard in simulation and measurement. The validated ESD pulse is used to perform ESD susceptibility test in identifying radio susceptibility level which measured based on ESD failure level (in kV). The test is conducted in two types of radio; (i) Radio with well function and very susceptible to ESD (original radio) (ii) Radio with well function and low ESD susceptibility (improved radio).

(b) Identify sensitive IC that most susceptible to ESD using ESD immunity scanning measurement. With radio turn on, the “Open” radio condition is used to find area of IC with ESD failure which occurred at the lowest ESD discharge voltage from transmission line pulse (TLP) source.

(c) Model and simulate radio in “Open” condition on original and improved radio in order to measure the electromagnetic field intensity using E-field and H-field probes as well as calculate "time-weighted-average incident power (Ptwa)" delivered to sensitive IC. This forecasts level of RF energy exposure to the sensitive IC that can potentially causes ESD failure to the radio.

(d) Calculate “Ptwa” as criteria of ESD soft error failure prediction. A region of unacceptable incident power delivered to the IC is used as a limit to access the potential ESD soft error failure in future product.

In Step 1, the ESD pulse is simulated by zapping ESD gun model to ground directly as shown in Fig 5. This generates ESD pulse in double exponential shape with zero impedance. A square discharge voltage is applied to ESD gun circuitry resulting in the generation of double exponential waveform at tip of the gun. The verification is to measure ESD current using current probe, CT-6 validate the pulse compared with measurement and comply with IEC61000-4-2. The setup is shown in Fig 6. This step is important before it is used for ESD susceptibility test and simulation.

In step 2, identifying ESD failure level is performed through ESD susceptibility test which uses 2 types of radios in 2 conditions up to 12kV of ESD discharge voltage as shown in Fig 7. The goal of this experiment is to measure...
the ESD susceptibility level. The test is conducted in 3 stages: (i) Close housing (ii) open housing (iii) open housing without digital shield and sensitive IC.

![Test on "close housing" condition with shield](image)

(a) Test on “close housing” condition with shield

![Test on "open housing" condition with shield](image)

(b) Test on “open housing” condition with shield

![Test on "open housing" condition without shield and sensitive IC](image)

(c) Test on “open housing” condition without shield and sensitive IC

Fig 7: ESD test on two-way radio

Step 3 is conducted to identify sensitive component to high field strength using ESD immunity scanning as shown in Fig 8. The test is setup on “open housing” without digital shield. The field probe injects maximum discharge voltage of Transmission Line Pulse (TLP) on the surface of components. Once ESD failure occurs, the scanner started injecting the point at minimum TLP voltage until the radio has failed. The field probe is moved to a next point and this process is repeated on the entire radio. All failures detected by Failure Detection (FD) module are recorded and plotted. The color mapping shows the sensitive component with different failure level.

![Smart Scanner](image)

Fig 8: ESD Immunity Scanning (Smart Scanner)

Once the ESD pulse has been verified and ESD susceptibility level identified, the modeling of complete radio is started. The critical part of this session is to model the entire metal part of the radio. This includes PCB/flexes, electrical components and mechanical parts. Other components like LCD module, speaker, antenna and keypad are excluded as they are relatively less susceptible. The full radio is modeled including ESD Gun using symmetry boundary condition with ground plane which is defined as a perfect electrical condition (PEC). The process is referred to as step 4 in Fig 9.

![Model Chassis](image)

(c) Model Chassis

Fig 9: Monitor E & H-Field using Field probe

In 3D Full wave modeling, ESD pulse signal is injected or excited to GCAI contact. The current generates electromagnetic field on the conductor surface. The field strength of E-field & H-field is captured on the sensitive IC using E-field and H-field probes. The positions of field probe are defined as shown in Fig 10. The field density is measured in A/m (H-field) and V/m (E-field). The strong field density is shown as red hotspot where more ESD current passing to particular area. The distribution of H & E field strength allows seeing the ESD current spread in PCB. This is crucial for sensitive component. This is captured in step 5.

![E & H field probes assign on MAKO IC](image)

Fig 10: E & H field probes assign on MAKO IC

In step 6, a new parameter for ESD prediction is defined. This parameter refers to “Time-weighted-average power density delivered by the sensitive component during ESD event. The amount of incident power density is quantified
through ESD simulation and measurement. As there is no IBIS model available for the IC, both of simulation and measurement is performed without the IC. This creates an open circuit and high impedance at IC pins.

The measurement is performed using the measurement setup shown in Fig 11. With the removal of the physical MAKO IC, created an open circuit on the PCB, shielded cable with pogo pin in contact with the IC pins captures the “voltage over time” on the oscilloscope through a high impedance probe. A grounded copper tape is used to cover the component area on the PCB and acts as shielding.

In actual measurement, the following equations are used to calculate the $P_{twa}$. This illustrates as shown in Fig 12.

$$V^2 = \sum_{i=1}^{15} V_i^2 = V_1^2 + V_2^2 ... V_{15}^2$$  
$$P_N = \frac{V^2}{R}$$  
$$P_n = \sum_{i=1}^{N} \frac{P_{n, i}}{A} = \sum_{i=1}^{N} \frac{V_i^2}{RA}$$

$V =$ Magnitude of voltage from oscilloscope
$V_N =$ Voltage at the probe position, N which has area of $2\pi r^2$
$P_n =$ Total of incident power over area of probe, A at time $t_n$
$A =$ $2\pi * r^2 = 2\pi * 1 * 1 = 0.0000628 m^2$
$R =$ 1MΩ from high impedance probe

Thus, time-weighted-average power density defines as

$$P_{twa} = \frac{\sum_{n=1}^{N} P_{n, \Delta t_n}}{t_{n(m)}} = \frac{P_1 \Delta t_1 + P_2 \Delta t_2 + ... P_n \Delta t_n}{t_{n(m)}}$$

$\Delta t_n =$ Time interval between times (ns)
$t_{n(m)} =$ Actual time at different probe positions in measurement

In the last step of the process, an ESD limit criteria is established to predict ESD soft error failure at PCB and flex design stage. The validation is performed to verify the limit using three sampling radio unit in simulation and measurement. The counter measure is not covered in this paper. Through the ESD prediction, it allows engineer to review and improve the design to achieve the peak average power much lower than the defined limit for better ESD performance.

4. Result and Discussion

From ESD pulse verification experiment in step 1, the simulation results are closely correlated to actual measurement as well as IEC 61000-4-2. The result comparing ESD pulse is illustrated as in Fig 13. The simulated peak current waveform is measured as 3.71A at 1.6ns which agree with the actual measurement and IEC standard. The rise time of initial peak also match reasonably well between simulation and measurement figures. However the current levels are slightly different at 30ns and 60ns. The differences are summarized in Table 1. Overall the shape of three graphs indicates that simulation ESD pulse conforms to actual of specification.

![Fig 12: Graph of $P_{twa}$ for different radio models](image)

<table>
<thead>
<tr>
<th>Table 1: Comparison of rise time and current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse Type</td>
</tr>
<tr>
<td>-------------------</td>
</tr>
<tr>
<td>IEC Standard</td>
</tr>
<tr>
<td>Simulated</td>
</tr>
<tr>
<td>Measured</td>
</tr>
</tbody>
</table>

In step 2, the ESD system level test is performed to obtain the radio susceptibility level using contact discharge mode. This mode is chosen as ESD failure is more repeatable.
compare using air discharge mode. The ESD failure is determined based on the failure symptoms as shown in Fig 14. The display prompts “Fail 001” or LCD becomes blank whenever the ESD reset failure occurs. These symptoms are a temporary failure where the radio would function normally by manual turn off and on.

(a) Pass          (b) Fail 001 (c) Fail with Blank Display

Fig 14: ESD Failure symptoms

The following results show that the failure happens at all GCAI pins including ground pin.
(a) Close housing - By exciting the ESD pulse at the external GCAI pin, the result of ESD system test is captured in Table 2 where the failures occurred starting from 5kV.
(b) Open housing with shield - The failures symptoms are observed from 6kV up to 13kV as shown in Table 3.
(c) Open housing without shield shows similar trend to result of ‘open housing’. The results are tabulated in Table 4 and 5. It was observed that the failures occurred starting at 6kV for original radio and 10kV to 11kV for improved radio.

Table 2: Results on bad radio at “Close housing” with shield

Table 3: Results on bad radio at “Open housing” with shield

Table 4: Results on bad radio without shield

Table 5: Results on improved radio unit without shield

From result in (a) and (b), it was discovered that the ESD performance of the radio is not affected by the radio assembly structure. Overall the results show the ESD failure started occurring at range of 5kV to 6kV on original radio while the improved radio happened at higher level from 10kv to 11kV. This concluded that the design of original radio is able to stand 5kV for original radio and 10kV for improved radio.

In step 3, the area of focus is the digital circuitry. This is described as in Fig 15. The immunity scanning is performed on top and bottom side of PCB after the shield on digital circuitry has been removed. In Fig 16, the result shows that the ESD failures near to the ICs which are located in red spot area. Meanwhile the TLP level falls between 300V to 6kV. The low TLP indicates that the IC has high susceptibility to ESD disturbance.

To understand how the ESD failure occurred on the sensitive component, 3D simulation is executed to identify a parameter that change with the electromagnetic fields strength change. Thus the focus of investigation is in quantifying the incident power delivered to the sensitive components. The 3D simulation is performed using two models; (1) Original radio with direct path of ESD from GCAI pins to PCB via the flexible circuit (2) Improved radio with two paths using metal ground to divert the ESD current immediately to system ground so that minimal ESD
energy delivering to the components on PCB. Fig 17 illustrates the models with different path of electromagnetic (EM) fields.

![EM propagation path directly to PCB](image1)

(a) Direct ESD path to component on fail radio

![EM propagation path divert to ground](image2)

(b) Divert ESD directly to ground on pass radio

Fig 17: Models with different ESD pulse paths

The distribution of surface current resulting from 5kV firing is shown in Fig 18a and Fig 18b. The H-field distributes in entire space of the radio depending on the amount of ESD current passing through the surface of area. This shows that the energy from tip of the ESD gun travels through flex and delivers to the IC. The reduction of field strength is contributed by the metal ground which diverts the ESD energy so that the ground potential is raised in parallel to the ESD reaching the MAKO pins that corresponds to the GCAI pins. The metal ground also distributes the Ptwa to other less sensitive components on the PCB.

![Hot spot on failed radio (PCB rev 3) at 5kV](image3)

(a) Hot spot on failed radio (PCB rev 3) at 5kV

![Hot spot on pass radio (PCB rev 5) at 5kV](image4)

(b) Hot spot on pass radio (PCB rev 5) at 5kV

Fig 18: H-field distribution on MAKO IC at 2.2ns

The composite effect of different field intensity (field strength) at the 15 position of MAKO pins is used to calculate incident power density at the IC. At any tn, the incident power density, \( P_n \) is presented as Poynting vector which measure in W/m². The total power density is determined based on the power measured at 15 of physical positions (N) of E-field and H-field probes that use to quantify the field density of E-field and H-field on MAKO IC pin.

The total of incident power density for original and improved radio is computed and plotted as in Fig 19. The incident power density reaching the MAKO IC pins shrink as most of ESD energy being diverted to the ground plane through the metal bar on the improved radio.

![Graph of Poynting vector for different radio models](image5)

Fig 19: Graph of Poynting vector for different radio models

The graph of \( P_n \) is noisy. Applying filtering using “time-weighted-average power density (Ptwa)” it would be easier to see the power improvement of the improved radio delivered to the MAKO IC. The equation (14) is used to express the power density. In Fig 20, the graph of incident power density of improved radio is decreased by almost half of original Ptwa graph.

\[
Ptwa = \frac{\sum_{n=1}^{N} P_{n} \Delta t_{n}}{t_{n}(s)} = \frac{P_{1} \Delta t_{1} + P_{2} \Delta t_{2} + \ldots + P_{N} \Delta t_{N}}{t_{n}(s)}
\]

\( P_{n} \) - Incident power density delivered to sensitive IC pins \( n \)

\( \Delta t_{n} \) - Time interval between times at IC pins \( n \)

\( t_{n}(s) \) - Actual time at diff probe positions in simulation
By referring to actual ESD test tables at early result, there are three graph limits defined as a baseline to assess potential ESD soft error failures. The graphs shown in Fig 21 are the power distributed to MAKO IC causing the radio began to fail.

(a) ESD specification limit at 8kV – The simulation graph A illustrates Ptwa of ESD spec limit which define to meet the system level requirement of IEC 61000-4-2 standard.

(b) ESD failing threshold limit at 5kV – This is a limit where the radio starts failing ESD test above 5kV which shown in Table 3. The simulation graph B shows Ptwa of original radio at 5kV.

(c) ESD failure threshold limit at 9kV - This refers to first failure observing on the improved radio. This illustrates as graph C.

Note that as the actual radio software is not included in the radio modeling, the graph of specification limit is not indicating of any ESD soft error failure. Hence the graph of threshold limit is required to point out the simulation of actual radio failure as shown in graph B.

Below are criteria for passing ESD in simulation
(a) Any graph of at least 8kV, Ptwa density of radio must fall below the spec limit to pass ESD test.
(b) The closer to spec limit, the higher is the risk of ESD failure.
(c) Delta of Ptwa-peak at XkV must equal or less than 15% of total delta of Ptwa-peak, h between graph A and B. The XkV has to more than 8kV.

It is important to highlight that this criteria only apply to any design with present of MAKO IC populated on 12-layers PCB. Any two-way radio design with non-MAKO IC, new criteria requires to be established.

By having the criteria of ESD failure of original radio as a baseline, prediction of ESD failure is achieved as shown in Fig 22.

(a) ESD at 8kV – The graph D is fallen below the spec limit, graph A. This explains the incident power reaching at MAKO IC pins are reduced consistently compared the graph A. Beside the delta of Ptwa-peak at 8kV is 2%. This simply explains the improved radio has possibility to pass ESD test. The graph D refers to no ESD soft error failure being observed during ESD test where the radio works as normal without any function disruption. This is proven in ESD test on Table 5.

(b) ESD at 11kV - The Ptwa density of improved radio at 11kV has fallen below the spec limit. Nevertheless the delta of Ptwa-peak at 11kV is 42%. This is more than 15% criteria delivered to MAKO IC. Hence 11kV will likely fail ESD.

The concept of prediction of ESD failure based on the peak of Ptwa is now applied in measurement. In Fig 23, the measurement graph H, J and K reflects the actual Ptwa of the improved radio at 8kV, 9kV and 11kV respectively. In Fig 23(a), the delta of Ptwa-peak at 9kV shows as 40%. This is 10% higher than the simulated value due to differences of components exist in measured radio compared in simulation model. Fig 23(b) shows the delta of Ptwa-peak at 8kV is
25% which lower than the limit. This is proven that the graph J predicting as ESD passing. Whereas for the graph K in Fig 23(c), the delta at 11kV is 70% which is above the limit and this causes the radio failing the ESD test.

This explains that the huge incident power density reaching at MAKO IC (ESD sensitive component) likely causing the ESD failure as the power is more than the MAKO IC can withstand during ESD event.

1. The trend of peak Ptwa graph show close correlation between simulation and measurement based on the percentage of delta Ptwa and potential ESD failure. However there are differences on the actual magnitude of Ptwa and rise time.

2. The simulation model does not include software of the radio. Hence it cannot tell ESD soft error failure. Therefore, physical ESD test is required to define ESD failure threshold at least once. In consequence PCB cycle (pass), ESD prediction is done through the simulation ESD failure threshold (limit).

3. With the spec limit at 8kV, passing ESD test with high margin requires the percentage of delta to be below 15% at higher kV example 11kV or above.

Table 6: Comparison of delta Ptwa in simulation and measurement for potential ESD failure prediction

<table>
<thead>
<tr>
<th>ESD Discharge Voltage (kV)</th>
<th>Delta of Ptwa-between-peaks &amp; potential ESD failure</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Simulation</td>
</tr>
<tr>
<td>8kV</td>
<td>2%</td>
</tr>
<tr>
<td>Pass ESD</td>
<td>Pass ESD</td>
</tr>
<tr>
<td>9kV</td>
<td>15% - “Threshold”</td>
</tr>
<tr>
<td>Fail ESD</td>
<td>Fail ESD</td>
</tr>
<tr>
<td>11kV</td>
<td>40%</td>
</tr>
</tbody>
</table>

The same approach is used for actual measurement. It is found that the trend of simulation graph is similar to actual graph. However there are differences.

(a) Magnitude of Ptwa density – The hypothesis is the absolute Ptwa value of measurement is higher than simulation is likely due to the aggregation of power at MAKO pins via electronic components other than those present in simulation model. Note that the simulation model does not contain active and passive component models except those that are connected between the external source (GCAI pins) and MAKO IC.

Table 6 shows differences in Ptwa between peaks. The pattern is similar but the absolute value is difference. Thus, this phenomenon needs further research.

(b) Rise time - The hypothesis is the rise time of actual measurement is lower than simulation due to higher capacitances present in those electronic component other than present in simulation model. The differences are shown in Table 7.

The prediction of potential ESD failure in simulation is summarized in Table 6.
Table 7: Differences between simulation model and actual measurement

<table>
<thead>
<tr>
<th>Part Description</th>
<th>Quantity on Actual Radio</th>
<th>Quantity on Simulation model</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>GCA1 LCD &amp; Main flex</td>
<td>3</td>
<td>2 - Excl LCD flex</td>
</tr>
<tr>
<td>Plastic housing</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Antennas Chassis</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Metal Retainer</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Components on GCA1 flex including zener diode</td>
<td>24</td>
<td>24</td>
</tr>
<tr>
<td>Components on Main flex</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>Passive &amp; Active SMD components on PCB except BGA IC</td>
<td>3378</td>
<td>969 - Includes RLC component &amp; Active Components connect GCA1 pin to MAKO IC</td>
</tr>
<tr>
<td>BGA IC</td>
<td>8</td>
<td>0 - No IBIS model exist</td>
</tr>
<tr>
<td>Cables on PCB</td>
<td>17</td>
<td>17</td>
</tr>
<tr>
<td>Board-to-Board Connection</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Metalcore between Chassis to PCB</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>Battery</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Mechanical parts such as LCD module, Keypad, speaker, antenna, volume knob</td>
<td>28</td>
<td>0</td>
</tr>
</tbody>
</table>

4.0 Conclusion

The prediction of ESD failure in 3D simulation has been achieved at radio system level. This completed by introducing a limit of allowable incident power sending to the sensitive component (MAKO IC) during ESD event. By simulating the delivered power using the Poynting vector to calculate the “time-weighted-average power” density allows quantifying the incident power at the sensitive IC. The limit is defined as a delta of peak Ptwa between the ESD failing thresholds of original and improved radio must equal and less than 15%. With this prediction, it permits electrical engineer to assess the potential risk of ESD failure and consider possible layout improvement to divert the ESD energy away from the IC of interest through better grounding or adding zener diode in strategic areas.

The differences between model and actual radio may due to the modeling simplification below:
(a) The radio model did not include IBIS models for seven ICs and other active component. This caused inaccurate total of incident power density reaching at MAKO IC pin.
(b) Changing the bending shape of flex model from arc to 90 degree bending may cause inaccurate digitizing calculation.

By simplifying the model, the meshing size is reduced by 2X and improved the simulation time from 15 days to 3 days. As the differences are affecting the delta of Ptwa between peaks, further work is strongly required to improve the simulation model and achieve better correlation result between simulation and measurement.

Future Works

There are three areas to be explored in future to achieve better correlation between simulation and measurement.
1. Include model of actual components and IBIS into simulation
2. Study the mechanism between exposure to ESD electromagnetic and the software outcome is still unknown.
3. Study the differences in Ptwa between peaks

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References