Junctionless Sub-Micron Silicon Wire Device Fabricated by Atomic Force Microscope Lithography and Electrically Characterized for Gas Sensing Application at Room Temperature

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Abstract
Fabrication of junctionless sub-micron silicon wire based device using atomic force microscope lithography was presented in this article. The fabricated device consisted of two adjacent probing pads which served as probing pads during electrical characterization. This adjacent probing pads were connected with two parallel sub-micron silicon wires. P-type silicon-on-insulator wafer was used as a raw material in the experiment. The sub-micron silicon wires width between 207 nm and 233 nm was successfully fabricated by means of the aforementioned technique. The fabrication process was conducted in the temperature between 21 °C and 27 °C and relative humidity between 50 % and 70 %. The process was operated in contact mode using standard commercial atomic force microscope without any modification. In addition, 9.0 V of applied voltage and 2 μm/sec of writing speed were used to perform the fabrication process. The fabricated device was realized using wet chemical etching process which involved the usage of tetramethylammonium hydroxide and hydrofluoric acid solution. The bare device was electrically characterized using semiconductor parameter analyzer and the signal was recorded in form of current-voltage characteristic. From the current-voltage characteristic, the fabricated junctionless sub-micron silicon wire device behaved as a resistor where there was a current flow from one contact point to another. To prolong the functionality of the fabricated junctionless sub-micron silicon wire device, the device was tested under gaseous environment at room temperature. Carbon dioxide and nitrous oxide gas were chosen as target gases in the experiment. These two gases were classified as oxidizing agents and act as holes donor to the sub-micron silicon wire device. The current of the fabricated device was decreased upon exposure to both target gases compared with before target gases exposure. In other words, the device resistivity was increased when the target gases were introduced to the fabricated device. Furthermore, the target gases behaved as a chemical gate to the junctionless sub-micron silicon wire device in this study. In addition, applying the target gases (holes donor) to the p-type junctionless sub-micron silicon wire was comparable to applying positive gate voltage to the p-type semiconductor which caused depletion of mobility carrier and reduced the p-type device current. Therefore, the decrease of current value of junctionless sub-micron silicon wire device was expected and observed for this study. In term of sensitivity, the sensitivity of fabricated junctionless sub-micron silicon wire device was 65 % and 57 % when the device was exposed to 9 sccm of carbon dioxide gas and 8 sccm of nitrous oxide gas, respectively. The response and recovery time was observed to be less than one minute for both target gases study.

1. Introduction
Junctionless gated resistor attracts great attention of researchers because of several advantages such as the ability to eliminate ultrafast annealing process which is very costly, allow shorter channels fabrication, avoid the use of an ultrashallow source or drain junction and reduce the imperfection effect of the semiconductor/insulator interface because the current transport is in the bulk semiconductor [1] [2]. A junctionless based devices allows single species of a same dopant concentration in source, drain and channel. In other word, a junctionless device is a device without any junction [2]. Therefore, junctionless based devices differ from those ancient devices which based on the junction formation such as diode, junction field effect transistor (JFET), bipolar junction transistor (BJT), metal oxide semiconductor field effect transistor (MOSFET) and metal semiconductor field effect transistor (MESFET) [1]. Junctionless based device is first patented by Julius Edgar Lilienfield in 1925 in a form of transistor which allows device conductivity to be modulated by controlling the carrier density using a gate [1]. In order to fabricate a junctionless gated resistor, high doping concentration is needed to assure high current flow and good contact resistance between source and drain. Unfortunately, high impurity increases the scattering effect and limits the carrier mobility [1]. Meanwhile, low doping concentration provides another advantage such as low ‘off’ current and less scattering effect [1] [3]. However, the mobility in lightly doped device is limited by phonon scattering [1]. Research on junctionless gated resistor have been reported such as by [1], [2], [4], [5], [6] and [7]. However, there are a few major differences between this study and the reported research such as device structure, device features and device testing. Further details on the device structure, features and testing for this study can be obtained in Section 2 and Section 3.

Atomic force microscope (AFM) is well known as a powerful tool for obtaining topographical image surfaces with atomic resolution [8] and widespread tool in the research laboratories [9]. AFM tool offering many advantages such as simple, ease of operation, fast and cost effective [9] [10] [11] [12], ability to operate in various conditions [12] [13], maskless lithography [14] and ability to observe real-time result for surface characterization [12] [15]. AFM techniques can be classified into two general groups which are bias-assisted and force-assisted nanolithography [12]. In this study, bias-assisted class
technique has been used to pattern structure on the sample surface which known as local anodic oxidation technique. This applied bias is used to generate localized electric field with a distance of nanometer gap between the AFM tip and the sample to produce desired pattern structures [12].

The gas sensing materials are currently dominated by semiconducting metal oxide materials as reported by [16] due to their physical and chemical stability. However, this materials require high operating temperature for target gases detection [16]. Meanwhile, silicon based device such as porous silicon [17] and silicon nanowires [18] [19] have been reported able to detect target gases at room temperature. Therefore, a development of silicon based device as a gas sensing device is proposed in this study in reflex to the advantage of silicon based device as a gas sensing material which able to detect target gases at room temperature.

In this study, junctionless sub-micron silicon wire device in form of a simple resistor has been prepared by means of AFM local anodic oxidation technique. The device was used for carbon dioxide (CO$_2$) and nitrous oxide (N$_2$O) gas detection at room temperature. The physical characterization of the device was done through AFM while the electrical characterization was done through semiconductor parameter analyzer (SPA).

2. Experimental

This study involved the use of P-type [100] crystal orientation silicon-on-insulator (SOI) (SOITEC), standard atomic force microscope (SPI 3800N; SII Nanotechnology Inc.) and precision semiconductor parameter analyzer (HP 4156C, Agilent) as the main material and equipments. The research was also supported by the use of tetramethylammonium hydroxide solution (TMAH, 25 %) for etching purpose and other electronic-grade chemicals for cleaning purpose. For the device testing, two gases were chosen as target gases which were CO$_2$ and N$_2$O gas. The target gases flow rate were controlled using mass flow controller (SmartTrak® 100 Mass Flow Meters & Controllers, Sierra) during testing procedure. Generally, the experimental process was categorized into two main groups which were device fabrication and device characterization.

The device fabrication process was divided into four steps which were cleaning process, oxidation process, silicon etching process and oxide removal process. For the fabrication process, the ready-to-use SOI wafer which doped with $10^{15}$ cm$^{-3}$ of boron concentration and had an initially 100 nm single-crystal silicon layer on top of 200 nm of buried oxide and bulk silicon substrate was used. Prior to the device fabrication, the SOI wafer was first cut to the desired size approximately 1 cm x 1 cm and cleaned using the standard cleaning process. After cleaning process, the fabrication process was performed using standard AFM based on the local anodic oxidation technique in a contact-mode. The overall gold-coated AFM probe tip with 13 kHz resonant frequency and 0.2 N/m force constant was used for the device fabrication and surface characterization process. The fabrication process was also supported with several important parameters such as temperature, relative humidity, applied voltage and writing speed. The temperature and relative humidity were set up to between 21 °C and 27 °C and between 50 % and 70 %, respectively. Meanwhile, the applied voltage and writing speed were set up to 9 V and 2 μm/sec, respectively. At this stage, a very thin of oxide layer which less than 4 nm of desired pattern was produced on top of the silicon layer. This oxide layer will serve as a masking layer for the next step i.e. silicon etching process step. The silicon etching process was performed after AFM local anodic oxidation with the used of TMAH solution. The solution was heated up to 65 °C. This process is necessary to structure the silicon layer to the desired pattern depending on the oxide pattern. The sample with oxide pattern was immersed into the heated TMAH solution for 20 s to remove the uncovered oxide silicon area and left the oxide-covered silicon area. The buried oxide layer of SOI wafer will serve as a stop layer during this process. After silicon etching process, the thin oxide layer which served as masking layer was removed using 2 % hydrofluoric acid. The sample was immersed for 30 s and this process was performed at room temperature.

The characterization of the fabricated device was divided into two categories which were physical characterization and electrical characterization. The physical characterization was performed using AFM after each step of the fabrication process. The same procedures during oxidation process were applied and the same probe tip was used for the physical characterization process except for the used of applied voltage. No voltage was applied in the physical characterization process to avoid modification of the patterned structure. Meanwhile, the electrical characterization was performed using SPA onto the final bare device and onto the tested device in the presence of target sample. Furthermore, the electrical characterization process was performed at room temperature for both bare device testing and target sample testing. For the gas testing, the gas flow rate was set to 9 sccm and 8 sccm for CO$_2$ and N$_2$O gas, respectively. In addition, the exposure time of the target gases was set to 1 minute for both gases.

3. Results and Discussion

Fig. 1 shows the AFM image of SOI wafer after cleaning process. The surface roughness (Ra) of the sample was horizontally and vertically measured. The Ra of the sample was 1.230 x 10$^{-2}$ nm and 1.844 x 10$^{-2}$ nm (the measurement not shown here) for horizontal and vertical measurement, respectively. This value was absolutely low compared with 0.241 nm silicon surface roughness as reported by [15]. The AFM image of the device structure after local anodic oxidation process is shown in Fig. 2. In this study, device with two parallel silicon wires was fabricated by the aforementioned technique. The two parallel silicon wires were connected to the two adjacent contact pads. These contact pads served as probing pads during electrical characterization. The oxide height obtained in this study were 3.30 nm and 3.48 nm, from left to right (the measurement not shown here). These value is
greater than obtained by [15]. They observed only 2.8 nm of oxide height which fabricated with greater applied voltage (-10 V) and slower writing speed (1 μm/sec) compared with this study.

Fig. 1 An AFM image of SOI wafer after cleaning process.

Fig. 2 An AFM image of oxide pattern after local anodic oxidation process.

Fig. 3 An AFM image of device structure after silicon etching process.

Fig. 3 shows the AFM image of device structure after silicon etching process. At this stage, the uncovered silicon area (without oxide layer on top) was etched away and left the covered silicon area (with oxide layer on top). Therefore, the thickness of the patterned silicon wire should more than 100 nm (as per SOI specification in Section 2) including patterned oxide layer. In this study, the obtained wires thickness (height) after silicon etching process were 101.89 nm and 103.24 nm (left to right, the measurement not shown here) including the thin oxide layer on top of the silicon layer. An expansion of wire width after silicon etching process compared with after oxidation process was expected due to the undercutting process. The undercutting process is due to the etchant itself which is an anisotropic etchant. This etchant cause a lateral under-etching at the interface of silicon [100]/silicon oxide [111] [20]. Furthermore, the etch rate of [100] crystal planes is faster than [111] crystal planes and produces a trapezoidal shape of the silicon nanowires as reported by [21]. In this study, the average etch rate of Si [100] is approximately 5 nm/s calculated using Equation (1) where ER is referred to average etch rate (nm/s), D is referred to etched structure depth (nm) and t is referred to etch time (s).

\[ ER = \frac{D}{t} \]  (1)

Fig. 4 shows an AFM image of device structure after oxide removal process. This process is necessary after silicon etching process to remove the thin oxide layer on top of the silicon layer. Furthermore, this process helps to promote chemical species adsorption on the silicon wire surface as reported by [22]. The obtained silicon wires thickness (height) after oxide removal process were 98.15 nm and 99.36 nm (left to right, the measurement not shown here). This step confirms that the top silicon layer was perfectly etched during silicon etching process. This is because the measured silicon wire thickness (after oxide removal process) was close to 100 nm. Furthermore, a reduction in wire thickness after this process shows that a few nanometers of patterned oxide layer was successfully removed compared with after silicon etching process. The wires width and length and pad dimension of the fabricated device were measured after oxide removal process. The wires width obtained in this study were 233.4 nm and 207.8 nm (measured left to right wire) while the wire length was 10.77 μm. The pad dimension was approximately 6.2 μm x 7.7 μm.

Fig. 4 An AFM image of device structure after oxide removal process.

Electrical characterization of bare device was performed using SPA to measure the current-voltage (I-V) properties of the fabricated device. For this study, two sets of device (with the same structure) were prepared and used for the
electrical testing. The reason behind this because of the used of two target gases as target samples during electrical testing. Each device was dedicated to each target gas and separately tested. Fig. 5 shows the I-V characteristic of two set of bare devices, namely as device C (dedicated for CO$_2$ gas testing) and N (dedicated for N$_2$O gas testing). The I-V characteristic of device C and device N are shown in Fig. 5a and Fig. 5b, respectively. From the plotted graph, both devices exhibits difference I-V characteristic even though both devices possess the same structure. Device N exhibits an Ohmic contact trend with greater current value was observed for higher applied voltage. In addition, the current value of Device N was observed to be greater than Device C. Different graph trend was observed for Device C with lower current value compared with Device N. Furthermore, the current value of Device C was dropped when higher forward voltage was applied to Device C as seen in the graph. Noted that both devices were fabricated and tested at different time but the same parameters were applied for both fabrication and testing process. However, detail electrical characterization for the fabricated devices was not pursued in this study.

Electrical characterization of the devices in the presence of target gases was performed using SPA. The target gas was allowed to flow into a closed chamber consisting of the fabricated device inside there. Furthermore, the gas testing was conducted at room temperature. The parameters for the gas testing was included in Section 2. The device response to the exposed target gases was analyzed by plotting the sensitivity graph as a function of time. In addition, the device sensitivity was calculated using Equation (2) where $\Delta I$ is the current changes before and after gas exposure, I is the current acquired before gas exposure and $I_g$ is the current acquired after gas exposure.

$$\text{Sensitivity (S)} = \frac{(I - I_g)}{I} = \frac{\Delta I}{I}$$  

Fig. 6 Response graph of (a) Device C upon exposure to CO$_2$ gas (b) Device N upon exposure to N$_2$O gas, for 1 minute exposure time.

Fig. 6 shows the response graph of the device C and device N upon exposure to CO$_2$ and N$_2$O gas, respectively, for 1 minute exposure time. The response graph for Device C upon exposure to CO$_2$ gas is presented in Fig. 6a while the response graph for Device N upon exposure to N$_2$O gas is shown in Fig. 6b. From the response graph, both device C and device N showed a drastic change in $\Delta I/I$ value. In other word, the $\Delta I/I$ value was decreased upon exposure to both target gases. The $\Delta I/I$ value was increased back when no target gases were allowed to flow in the testing chamber. The response graph shows that both Device C and Device N were able to recover to the initial state (as before gas exposure).
The same author would also like to thank to UTHM scholarship, research funding and other facilities.

Acknowledgments

The author (M.T. Asmah) would like to thank to MOSTI MALAYSIA, CEDEC USM and SMMRE USM for the scholarship, research funding and research facilities. The same author would also like to thank to UTHM MALAYSIA for the workspace and other facilities.

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