IEEE Western Australia Section

Communication Society

An Introduction to the State Key lab of ASIC and System in China

Dr Yun Chen
Fudan University – Shanghai, China

Monday, 09 June 2014 @ 10:00AM – 11:00AM

Venue: **Billings Room 3.04, 3rd floor. Electrical & Electronic Engineering Building**
University of Western Australia, Crawley

This seminar is open to the public and admission is free to all IEEE members and non-members.

Abstract:

Approved by the National Planning Committee, the ASIC & System State Key Lab was set up in 1992 with a loan totalling US$1.6 million from the World Bank. The lab passed the national evaluation in September 1995 and re-evaluation in 2002. So far it is the sole national key lab that specializes in IC Design research in China. The lab has sixty full time members. Among them around 70% are under the age of forty-five and over 70% have a PhD Degree. Taking advantage of the multi-subjects edge and centring on the key issue of the close relationship between IC and China's IT development, the lab has launched research projects on specialized IC Design methodology and breakthrough technologies of IC systems on the basis of microelectronic technology, CAD and circuit system theory methodology. Its objective is to solve the edgy theoretical problems and key technological difficulties during the manufacturing process of system and IC, to develop chip technology with the autonomous intellectual property rights for the advanced electronic system, to become one of the most important bases for IC Design research, industrial development and talents cultivation. In this talk, Dr Chen will give an introduction of the Lab.

Biography:

Yun Chen received a M.S in UESTC in 2003 and a Ph.D. degree in Microelectronics from Fudan University, Shanghai, China in 2007. Since December 2007, she has been a member of the faculty of the state key lab of ASIC & system of China, Fudan University, where she is an associate researcher in the group of Professor Xiaoyang Zeng. From 2010 to 2011, she was a visiting scientist at KU Leuven and worked three months in IMEC, where she focused on the design and development of various wireless chips. Her research interests include coding theory, wireless communications, and communication ICs, Signal Processing in Communication and VLSI design in the Broadband Power Line Communications. Some of her past projects include ultra-throughput and low power LDPC and turbo decoder VLSI architecture, multi-mode base band mapping in the multi-core platform and long-echo channel estimation in DTMB (Digital Television Terrestrial Multimedia Broadcasting) standard. She has experience in taping out and testing more than 25 chips and is now one of Chinese standard setters for Power Line Communication and UWB. All these chips are about FEC or signal processing in communications. Some of her works have been published in IEEE transactions on circuits and system I and IEEE transactions on communications.