IEEE
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Quantum Topological states in nanostructured InAs/GaInSb superlattices

A Seminar of the IEEE WA joint EDS/SSCS/IPS Chapter

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Venue: **Billings Room 3.04, 3rd floor. Electrical & Electronic Engineering Building**
University of Western Australia, Crawley

This seminar is open to the public and admission is free to all IEEE members and non-members

Abstract:

Band-gap engineering of type-II InAs/GaInSb superlattices (SL) is an established approach for developing high-performance infrared photodetectors and lasers. In this talk, I will discuss how the technologies of nanostructurally engineered SLs can be applied for creating the topological states of novel materials such as Dirac semimetals (DSM) and topological insulators (TI). In particular, the experimental realization of a temperature-stable Dirac semimetal in zero-gap SLs will be presented [1]. The experimental InAs/GaInSb SLs are modeled using an eight-band k·p method in the envelope function approximation and synthesized by molecular beam epitaxy, which provides monolayer accuracy for growing single-crystals on large area substrates [2]. DSM and TI materials attracted significant interest in recent years as they are considered viable alternatives for potential applications in energy efficient electronic and photonic devices. The DSM and TI based on InAs/GaInSb SLs could provide a new development platform for these devices, taking advantage of the mature technologies of conventional semiconductors.

[1] M. Patrashin, N. Sekine, K. Akahane, A. Kasamatsu and I. Hosako, "Dirac semimetal states in engineered zero-gap InAs/GaInSb superlattices", Physica Status Solidi B 256(6), 1800726 (2019) DOI: 10.1002/pssb.201970024
[2] M. Patrashin, K. Akahane, N. Sekine, I. Hosako, "Molecular beam epitaxy of strained-layer InAs/GaInSb superlattices for long-wavelength photodetectors", J. Cryst. Growth 477, 86–90 (2017).

Biography:

Mikhail Patrashin received the Ph.D. degree in semiconductor device physics from the Institute of Radio-Engineering and Electronics, Russia, in 1995. He joined the National Institute of Information and Communications Technology (NICT), Tokyo, Japan, in 2004. He is a Senior Researcher in the Frontier Research Laboratory, where he is involved in the design, MBE growth, fabrication and characterization of nanostructured materials and devices based on compound semiconductors.