

Cleveland

Contact

Publication of the Cleveland Section of the Institute of Electrical and Electronics Engineers.

Call for Papers International Conference on Metrology Trends and Applications in Calibrations and Testing Laboratories

Jerusalem, Israel, May 16-18, 2000

by Vincent Lalli

All interested participants, please submit a paper on the theme of Metrology: Trends and Applications in Calibration and Testing Laboratories. The deadline for the 250-word abstract is December 1, 1999. The actual conference dates are May 16-18, 2000, to be held in Jerusalem, Israel.

Send your abstract to arrive by the deadline to: Secretariat, ISAS International Seminars, P.O. Box 34001, Jerusalem, Israel 91340. You may telephone for further information to 972-2-6520574, or FAX to 972-2-6520558. You may also e-mail to: isas@netvision.net.il.

Calendar of Events

Mark your calendar. You won't want to miss these!

October

7 PES/IAS will sponsor a tour of Ford Engine Plant #2 in Brookpark, OH. Optional lunch will follow at the Bomber Squadron restaurant. Contact Steve Phillips, (216) 368-6248 or via e-mail: smp2@po.cwru.edu for reservations, by October 4.

10 IAS meeting on "Position Estimation in Induction Machines Using High Frequency Signal Injection and Magnetic Saliency Information— a Sensorless Control Technique." Speaker: Barb Kenny, NASA.

Meeting location: Hofbrau Haus, 1400 East 55th Street, Cleveland, OH.

Optional lunch, \$7.50 (German Buffet), 11:30 a.m. Contact Carl J. Dister, IEEE IAS Section Chairman via e-mail: Carldister@ieee.org or by phone: (440) 255-2977 X 739.

Electric Deregulation

by Allen G. Morinec

Welcome to the Future of Electric Restructuring in Ohio. Beginning January 1, 2001, Ohio consumers will be able to choose their electricity supplier. The supplier they pick will generate the power, while their current electric company will distribute it to them through existing wires.

The Public Utilities Commission of Ohio is playing an integral role in developing competition while ensuring a level playing field for both consumer and marketer. This website outlines some of the terms, questions and policies being used in the process of restructuring Ohio's \$11 billion electric utility industry.

The PUCO updates the latest information on their web site [HYPERLINK http://www.puc.state.oh.us/ CONSUMER/restructuring/index.html](http://www.puc.state.oh.us/CONSUMER/restructuring/index.html). In the coming weeks, this site will be continually updated to provide timely and accurate information about electric restructuring in Ohio. The Public Utilities Commission of Ohio is dedicated to the success of electric restructuring and will continue to work with Ohio's consumers to provide a smooth transition into electric competition.

Additional topics located at the PUCO web site include:

- Corporate Separation Proposed Rules
- Education Plan Workshop Notes
- E-mail Feedback
- Regional Transmission Entity Questionnaire
- Stranded Costs RFP
- Final Bill Analysis prepared by LSC
- Electric Restructuring Timeline (PDF)

You can reach PUCO, The Public Utilities Commission of Ohio, at: 180 East Broad Street, Columbus, Ohio 43215. Or phone their Consumer Hotline: 1-800-686-PUCO. All information believed accurate but not guaranteed.





More Domain Names and Trademark Infringement

by Michael Garvey

Last month, we introduced some ways in which people use internet domain names similar to other people's trademarks. We focused on "pseudo-cybersquatters". Here are some cases involving other types of uses of similar domain names.

In a noncompeting siphoner case, Feinberg used the domain name "gunsareus.com" in the URL for his gun shop, "We Are Guns". Feinberg's shop had previously been known as "Guns Are Us" and later "Guns are We". The changes were made in response to objections by Toys 'R' Us.

The court found no likelihood of confusion with Toys 'R' Us, stating that the marks are different and the goods are very different. The opinion, however, suggests that the outcome might be different if the someone used "gunsrus.com".

The court also found no dilution. The court stated "While it is conceivable that the proliferation of trade names ending in 'R' Us, unassociated with plaintiffs, might cause blurring, this case is nowhere near such a situation." The court also stated "the differing product areas, absence of the single letter 'R' in the name, and peculiarities of an internet domain name make any association with Toys 'R' Us products extremely unlikely."

In a competing siphoner case, Jews for Jesus is an outreach ministry which owns common law rights in the mark JEWS FOR JESUS and a federal registration for the mark JEWS FR JESUS.

Brodsky is a vocal opponent of Jews for Jesus. Brodsky established a website at "www.jewsforjesus.org", which included a brief statement challenging the principles of Jews for Jesus and featured a hyperlink to Outreach Judaism, another opponent of Jews for Jesus. The court found in favor of "first come, first served." A federal trademark registration shows legitimate ownership of a trademark.

The Gillette Company apparently feels that the best defense is a good offense. Its home page is located at "www.gillette.com", but using "gilette" or "gilete" or "gilett" will send a user to the same home page. Of course, as Toys 'R' Us found out, you can't get all of the domain names.

Generally, use of a domain name that is similar to the trademark of another will be judged by the same standards that apply to more traditional uses. Possibly, because domain name registration is made without respect to the goods and there can be no duplication of domains, domain names will be even more closely scrutinized.

Undoubtedly, folks with copious free time and greed will devise schemes not addressed here. We can only hope that their ill-gained success can be overcome by a combination of technological and legal means.

Michael Garvey is a patent attorney at Pearne, Gordon, McCoy & Granger.

Cleveland Engineering Society October Events

E-Business, A "Tales from the Trenches" Breakfast, featuring Len Pagon, New Media; Kevin O'Brien, CAMP ECRC and Sean Mitchell, Millennium CAD & Paper Supply. 7:30-9:30 a.m. at the Cleveland South Hilton Inn, I-77 and Rockside. Sponsored by the Information Technology Division. Cost: \$20/CES members; \$25/affiliate members; \$30/non-members. Includes program and breakfast.

15 Cleveland Urban Setting Designation Breakfast Seminar, featuring a panel discussion. 7:30-9 a.m. at the Cleveland South Hilton Inn, I-77 and Rockside. Sponsored by the Environmental Division. Cost: \$20/CES members; \$25/affiliate members; \$30/non-members. Includes program and breakfast.

19 "Y2K: Will U.S. Banking be in Compliance?" Includes a tour of the Federal Reserve Building, featuring Gerald Anderson of the Federal Reserve. 11:45 a.m. to 1:45 p.m. at the Federal Reserve Building, Superior at 6th Street. Sponsored by the Senior Division. Cost: \$12/CES members and spouses; \$13/affiliate members; \$15/non-members. Includes program and breakfast.

21-22 CES & CWRU Career Fair at Thwing Center, Case Western Reserve University. The fair encompasses business, healthcare and non-profits, engineering, science and technology.

27 "Making Successful Decisions in a Complex Environment: A Workshop", featuring Darrell Smith of Picker International. 6:00-8:00 p.m. at the Unified Technologies Center, Woodland Avenue. A Management of Technology Lecture Series Dinner. Cost: TBA (but will be under \$30). Includes program and dinner.

27 Mechanical/Electrical System Architecture in Aging: Remodeled Healthcare Facilities, featuring a panel of professionals. 7:30-9:30 a.m. at Cleveland South Hilton Inn, I-77 and Rockside. Cost: \$20/CES members; \$25/affiliate members; \$30/non-members. Includes program and breakfast.

Contact the Cleveland Engineering Society, (216) 361-3100, or visit www.cesnet.org for additional information and registration.



CPU Performance Improvement 1: Pipelining

by Steve Belovich

The History

Pipelining is a computer architecture implementation technique in which the execution of adjacent machine instructions is overlapped in time. Pipelining has been and continues to be the main technique for creating fast central processing units (CPUs). The idea of CPU pipelining has been around for about 40 years, appearing mostly on large computers such as mid-range multi-user machines. During the past ten years, silicon fabrication technology has allowed pipelining to be used effectively on smaller machines such as microprocessors.

Pipelining is one of the few CPU speedup techniques that is completely invisible to the programmer. The programmer cannot tell if the machine instructions are executed in pipelined manner or are executed in a purely sequential manner. Other popular speedup techniques, such as compiler optimizations, eager branch executions, instruction prefetching, etc., depend heavily on the compiler and the programmer's cooperation. Pipelining requires no change to compilers, linkers or programming techniques and yield is a tremendous performance improvement.

The Technique

In an auto plant, one assembly-line area produces the engine and passes it to the next area, which attaches it to the chassis. The chassis/motor combination is passed to another area which assembles the body. The chassis/motor/body combination is then passed to the next area for interior assembly and so on. Each of the assembly line areas performs a specific, fixed set of tasks on the items placed before it. The type of car may differ, but the set of allowed operations at each assembly-line area does not. Each assembly line area also expects certain things from the preceding area. The chassis area expects to be supplied with engines, not body parts. Likewise, the interior assembly area expects that all necessary body parts will be correctly assembled. If these expectations are not met, the entire assembly line can come to a screeching halt (and somebody will lose his job). Also, the entire assembly line can move only as fast as the slowest step.

A pipelined CPU divides the execution of machine instructions into small, discrete steps or stages. Each stage performs a fixed task or set of tasks on the machine instructions. Each stage expects that the tasks done by the preceding stage have been correctly and completely performed. The time required to do the tasks at each stage is less than the time it would take to completely execute the machine instruction. Collectively, these stages are called an instruction pipeline or just a pipeline. A

CPU which executes instructions in this manner is called a pipelined CPU.

A Simple Non-Pipelined CPU

A simple, non-pipelined CPU also executes instructions in discrete steps or cycles. Although the quantity and function of each step varies from machine to machine, the basic ideas remain the same. Figure 1 shows the basic steps of instruction execution in a non-pipelined, "LOAD/STORE" CPU. This simple CPU is taken from the pedagogical DLX architecture, proposed by Hennessy and Patterson in Computer Architecture A Quantitative Approach (Morgan Kaufmann, 1990). A "LOAD/STORE" CPU performs all of its operations on register operands. The register operands are read from memory by "LOAD" instructions and are written back to memory by "STORE" instructions.

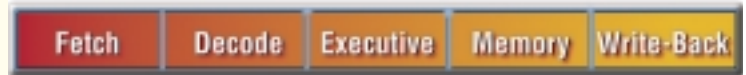


Figure 1: Instruction Execution for a Simple CPU

The first step is the "FETCH" step, which reads the instruction to be executed from memory. The program counter (PC) register contains the address of this instruction. The second step is the "DECODE" step. This step identifies the instruction to be executed and fetches any register-resident operands. The third step is the "EXECUTE" step. This step performs an arithmetic or logical operation on the register-based operands. The fourth step is the "MEMORY" step. This step reads (LOADs) or writes (STOREs) operands from/to memory as required by the instruction. The address of the memory reference is computed within the execution step. The fifth and final step is the "WRITE-BACK" step. This step writes the result of the execute step into a register. Note that a subsequent machine instruction may store this result somewhere in memory. As shown in Figure 1, all steps must be completed for a given machine instruction prior to starting the next one.

A Simple Pipelined CPU

Figure 2 shows what happens if the instruction execution steps are overlapped. In this case, once the fetch step is completed for the i -th instruction, the fetch step may be started for the $i+1$ st instruction. Likewise, the decode, execute, memory and write-back steps be performed for the $i+1$ st instruction immediately after completing work on the i -th instruction.

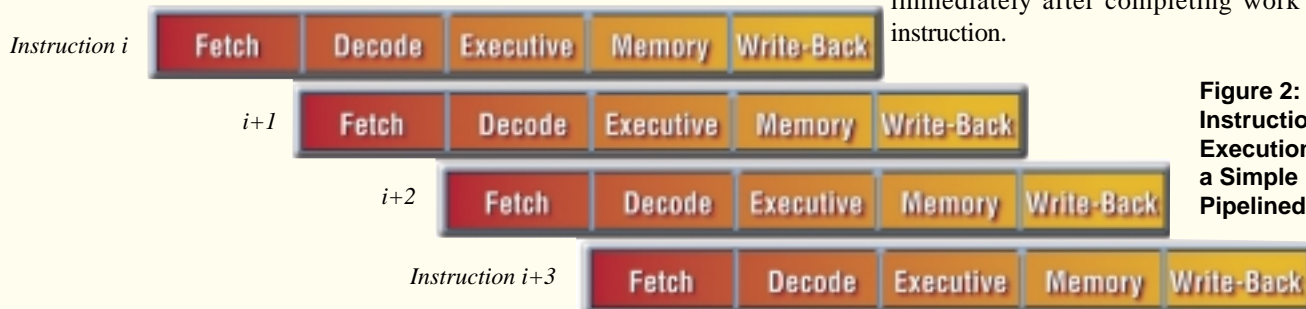


Figure 2: Instruction Execution for a Simple Pipelined CPU



Table 1 shows the time it takes for each of the five steps in the execution sequence for a machine instruction. The non-pipelined DLX requires 92 ns per instruction for an instruction execution rate of 10.9 MIPs. The pipelined DLX requires 30 ns per instruction per step, since instructions can travel the pipeline only as fast as the slowest stage will allow. With pipelining, instructions will exit the pipe (i.e., be executed) at the rate of 33.3 MIPs. This is a performance increase of 306%.

	Non-Pipelined DLX (ns)	Pipeline DLX (ns)
Fetch	30	30
Decode	8	5
Execute	14	10
Memory	30	30
Write-Back	10	5
Total Execution Time	92	30

Table 1: Performance Comparison Between Non-Pipelined and Pipelined DLX CPU

Pipeline Problems

As with nearly everything in life, pipelining is not free. A great deal of additional hardware is required to implement it relative to a non-pipelined CPU. The greatest challenge is hazards, which are situations that cause the pipeline to stall (i.e., stop). When a pipeline is stalled at the i -th instruction, instructions $i+1$, $i+2$, etc. are also stalled. When the hazard is cleared, the pipeline may be restarted. Hazards can severely degrade performance and they require careful design to reduce their impact.

Structural Hazards

Hazards fall into three classes: Structural, Data and Control. Structural hazards occur when the hardware cannot support all the simultaneous needs of the instantaneous instruction mix. An example of this is when two consecutive instructions need a special floating point unit which may not itself be fully pipelined. The second floating point instruction must wait until the first one has been completely processed by the functional unit. The pipeline will stall until this happens. Additional hardware can reduce structural hazards, but the expense can be considerable.

Data Hazards

Data hazards occur when the $i+1$ st instruction needs a result that will be computed by the i -th instruction, or even the $i-1$ st instruction. Since the results of the i -th instruction and/or the $i-1$ st instructions may not yet be ready, the $i+1$ st instruction (and all subsequent instructions) must wait until the results are ready. Data hazards may be reduced by “forwarding” (or bypassing), where the results of ALU operations are immediately recycled back to the ALU inputs for additional processing.

Data hazards may also be eliminated by pipeline scheduling (or instruction scheduling) whereby the compiler alters the order of instructions to reduce the inter-instruction dependencies. The drawback of this approach is that the complexity of the compiler increases. Since software is the major delay factor for most jobs, this can cause additional problems. Nevertheless, this technique for avoiding data hazards remains popular. This technique was first used in the 1960s.

Control Hazards

Control hazards happen when a BRANCH or JUMP instruction requires one or more results that will be computed by the preceding instruction(s). Like data hazards, the pipeline must stall until the results are available. The stalls here, though, are usually longer and hence reduce overall performance more than do data hazards. Control hazards may be reduced by finding out whether or not the branch will be taken earlier in the pipe and by computing the destination address of the branch earlier.

“Predict-not-taken” is a scheme in which the branch is assumed not to be taken and the hardware continues under this assumption. If this turns out to be wrong, the pipeline stalls and instruction execution continues with the instruction immediately after the branch target. “Predict-taken” is an obvious alternative scheme which requires advance computation of the destination address. Software can also help by rearranging the instruction order so that there is a greater separation between the destination address and branch decision and the branch execution. Clearly this solution is not possible in all cases.

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Cleveland Section

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The "Contact" is published eight times per year: September, October, November, January, February, March, April and May. The deadline for Newsletter articles is the 10th of the previous month.

Power Engineering Society and Industrial Applications Society Will Sponsor: *Tour of Ford Engine Plant #2* *Thurs., October 7, 1999*

The IEEE Power Engineering Society (PES) and Industrial Applications Society (IAS) will sponsor a joint tour of Ford Engine Plant #2 on Thursday, October 7th, 1999, from 9:00 to 11:00 a.m. in Brookpark, Ohio. The group is planning an informal lunch at the Bomber Squadron afterwards, at members' own expense.

The tour will focus on the assembly of the engines using the latest technologies in automation and robotics. Join us to see how the main engine components are manufactured and machined. An automation engineer will be available after the tour to answer technical questions.

The tour will be limited to 30 people. Please contact Steve Phillips at CWRU to make a reservation by October 4th, 1999. Steve can be reached at (216) 368-6248 or via e-mail: smp2@po.cwru.edu.

Directions: Take I-71 to Snow Rd. Head west on Snow Rd across the overpass. At the first light, turn right into the hourly employee parking lot. Proceed right again to Gate #10 guardhouse. The guard will direct you to the lobby.

WHAT: PES/IAS Joint Tour of Ford Engine Plant #2
Program is free

WHEN: Thurs. Oct 7th, 1999
Tour 9:00-11:00 a.m.
11:00 am lunch at Bomber Squadron (*at your own expense*)

WHERE: Ford Engine Plant
18300 Five Points Rd., Brookpark, Ohio