High Performance Digital Fractional-N Frequency Synthesizers

IEEE Distinguished Lecture
Lehigh Valley SSCS Chapter

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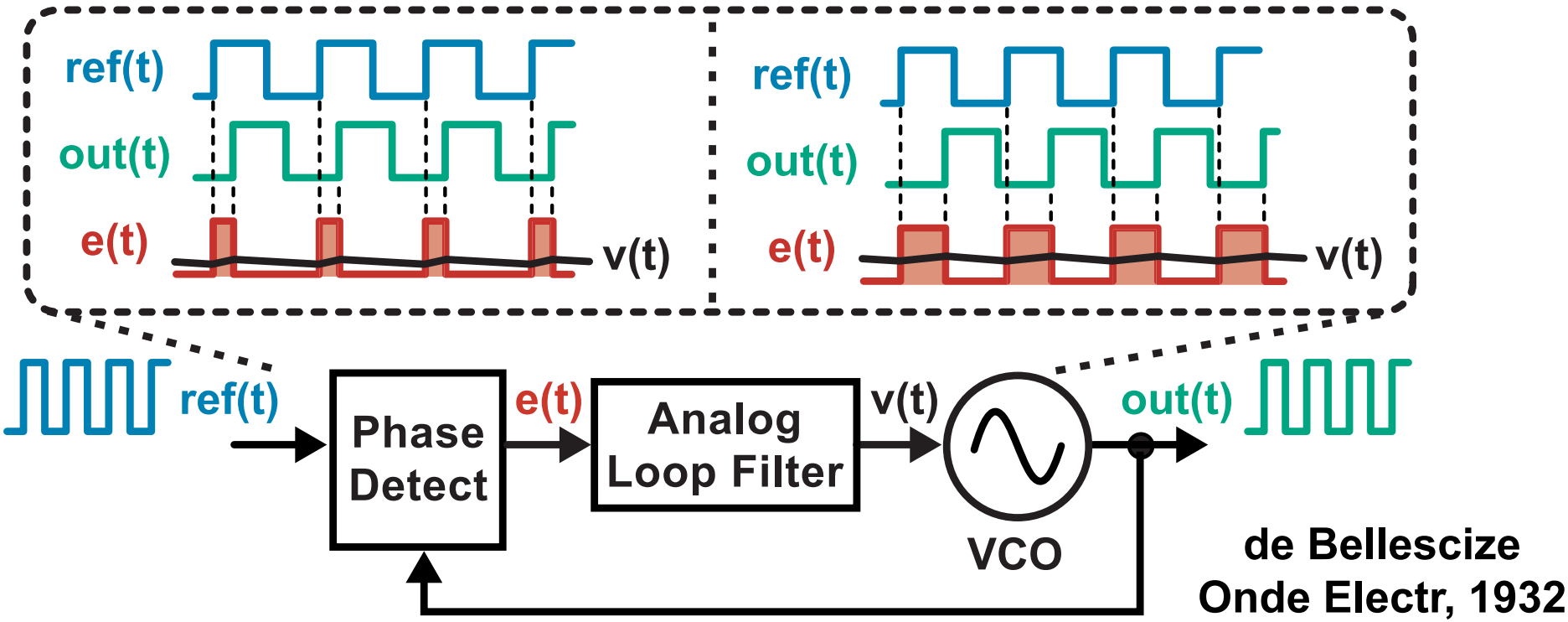
Why Are Digital Phase-Locked Loops Interesting?

- **PLLs are needed for a wide range of applications**
  - **Communication systems, digital processors, …**
- **Performance is important**
  - **Phase noise/jitter is often a limiting factor**
- **Standard analog PLL implementations present issues**
  - **Analog blocks pose design and verification challenges**
  - **The cost of implementation is becoming too high …**

Can digital phase-locked loops offer excellent performance with a lower cost of implementation?

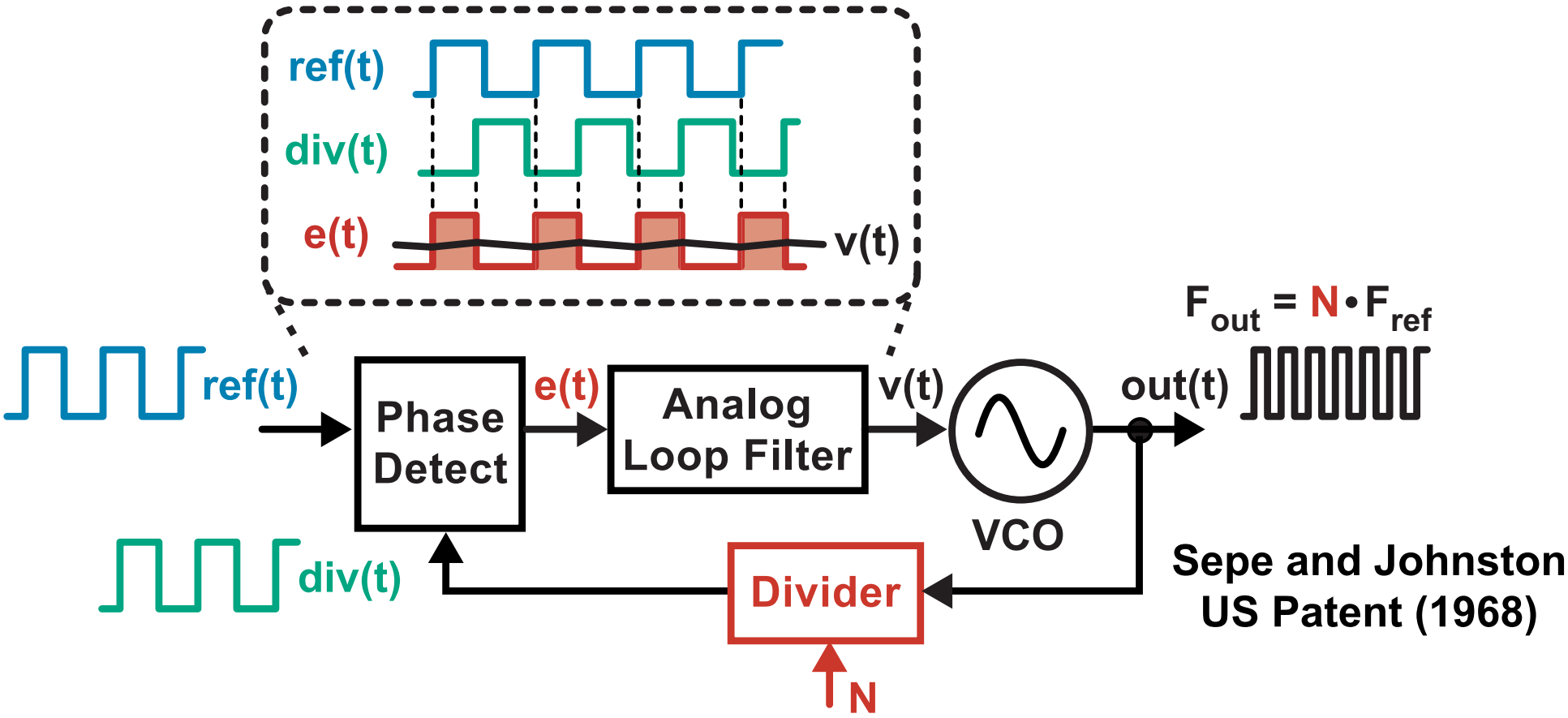
Just Enough PLL Background …

What is a Phase-Locked Loop (PLL)?



- **Voltage Controlled Oscillator (VCO) efficiently provides oscillating waveform with variable frequency**
- **PLL synchronizes VCO frequency to input reference frequency through feedback**
  - **Key block is phase detector**
    - Realized as *digital gates* that create pulsed signals

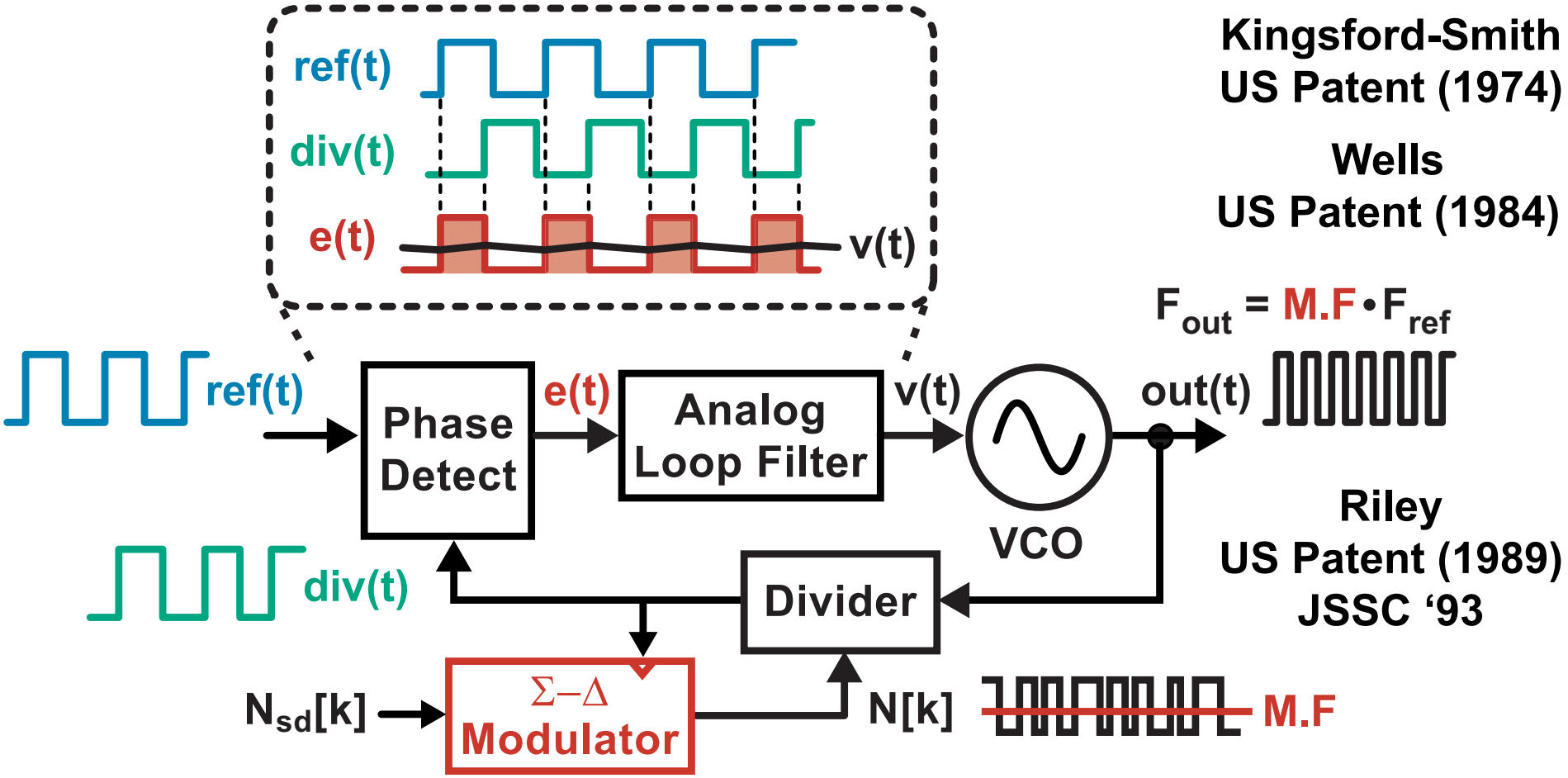
Integer-N Frequency Synthesizers



- Use digital counter structure to divide VCO frequency
  - Constraint: must divide by integer values
- Use PLL to synchronize reference and divider output

Output frequency is digitally controlled

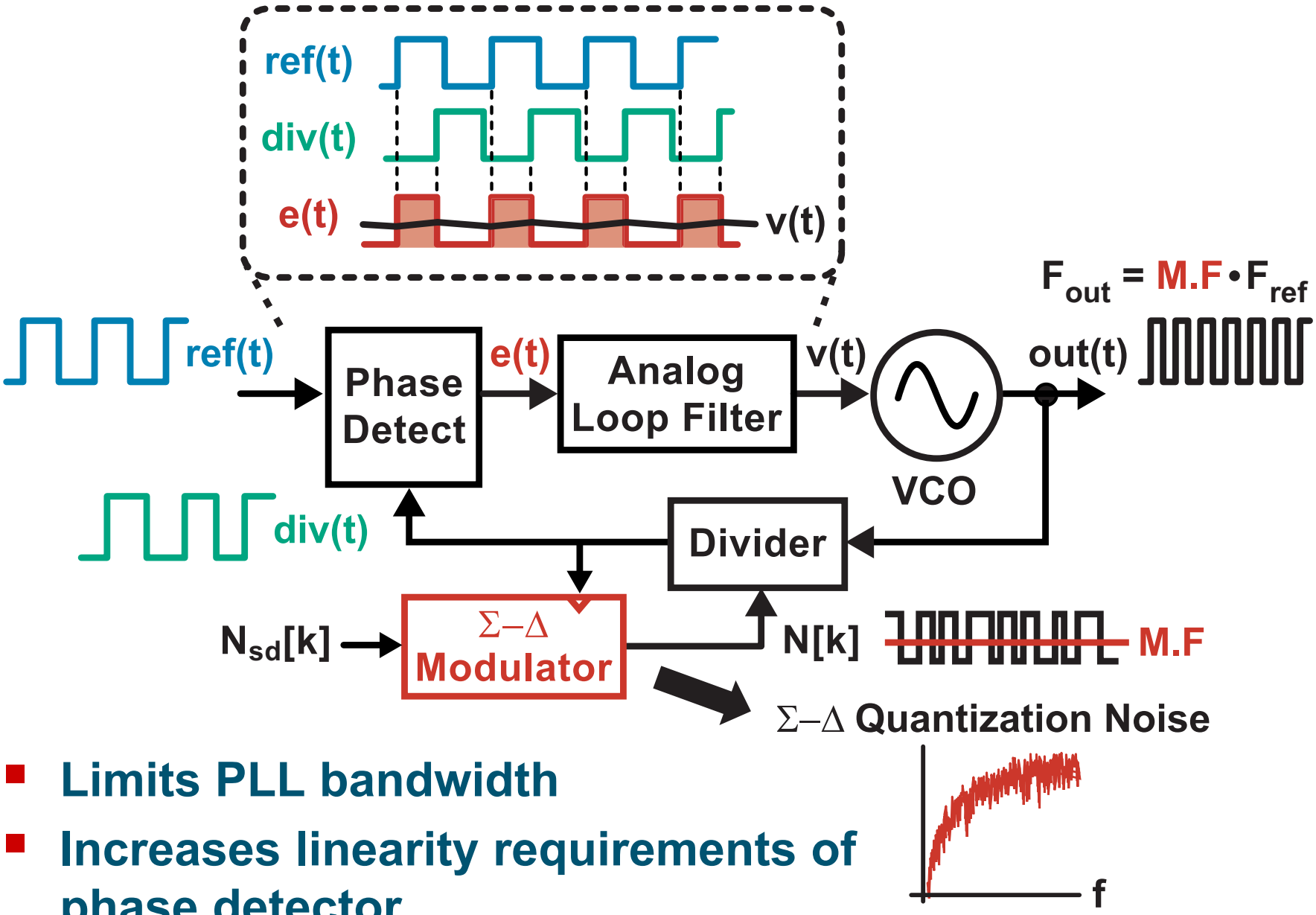
Fractional-N Frequency Synthesizers



- Dither divide value to achieve fractional divide values
  - PLL loop filter smooths the resulting variations

Very high frequency resolution is achieved

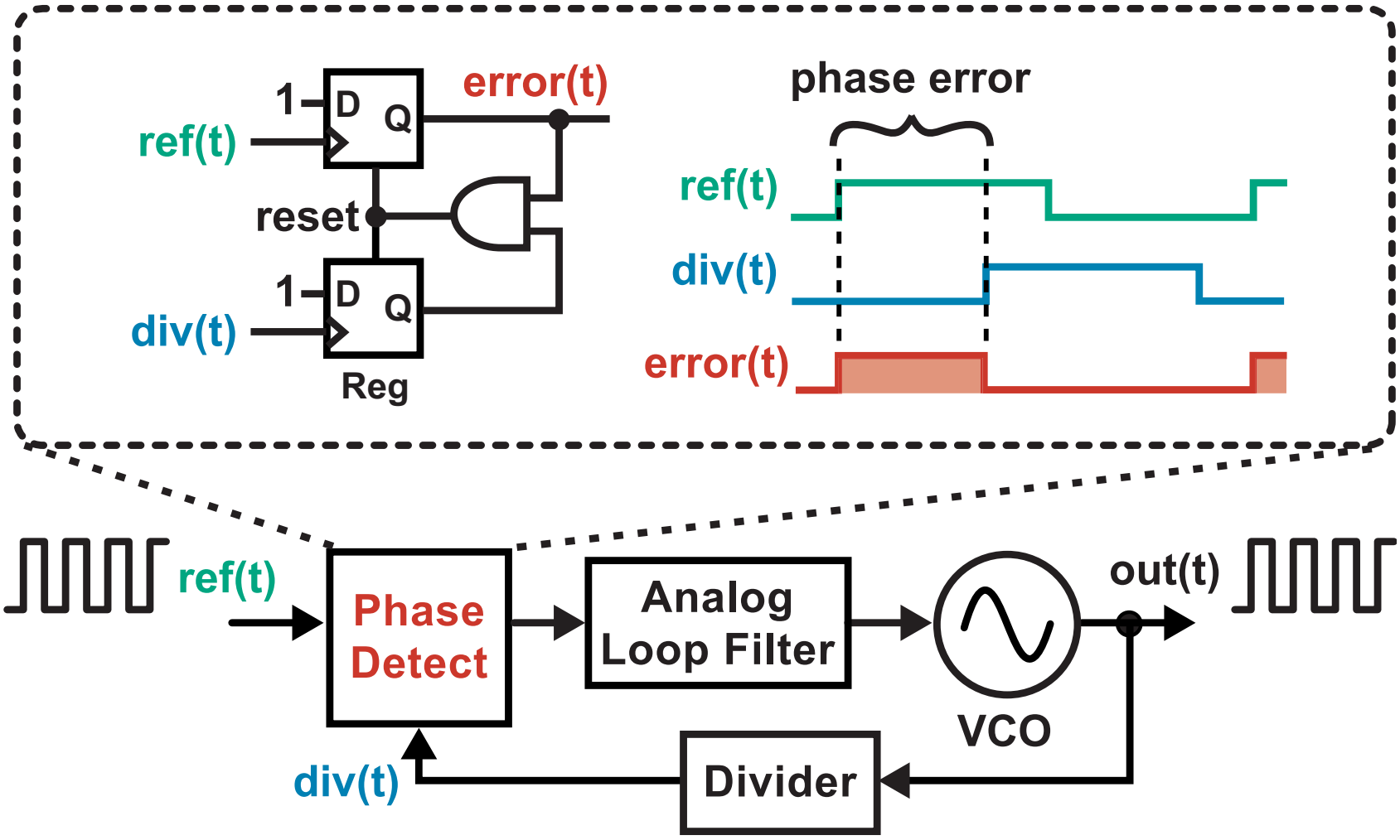
The Issue of Quantization Noise



- Limits PLL bandwidth
- Increases linearity requirements of phase detector

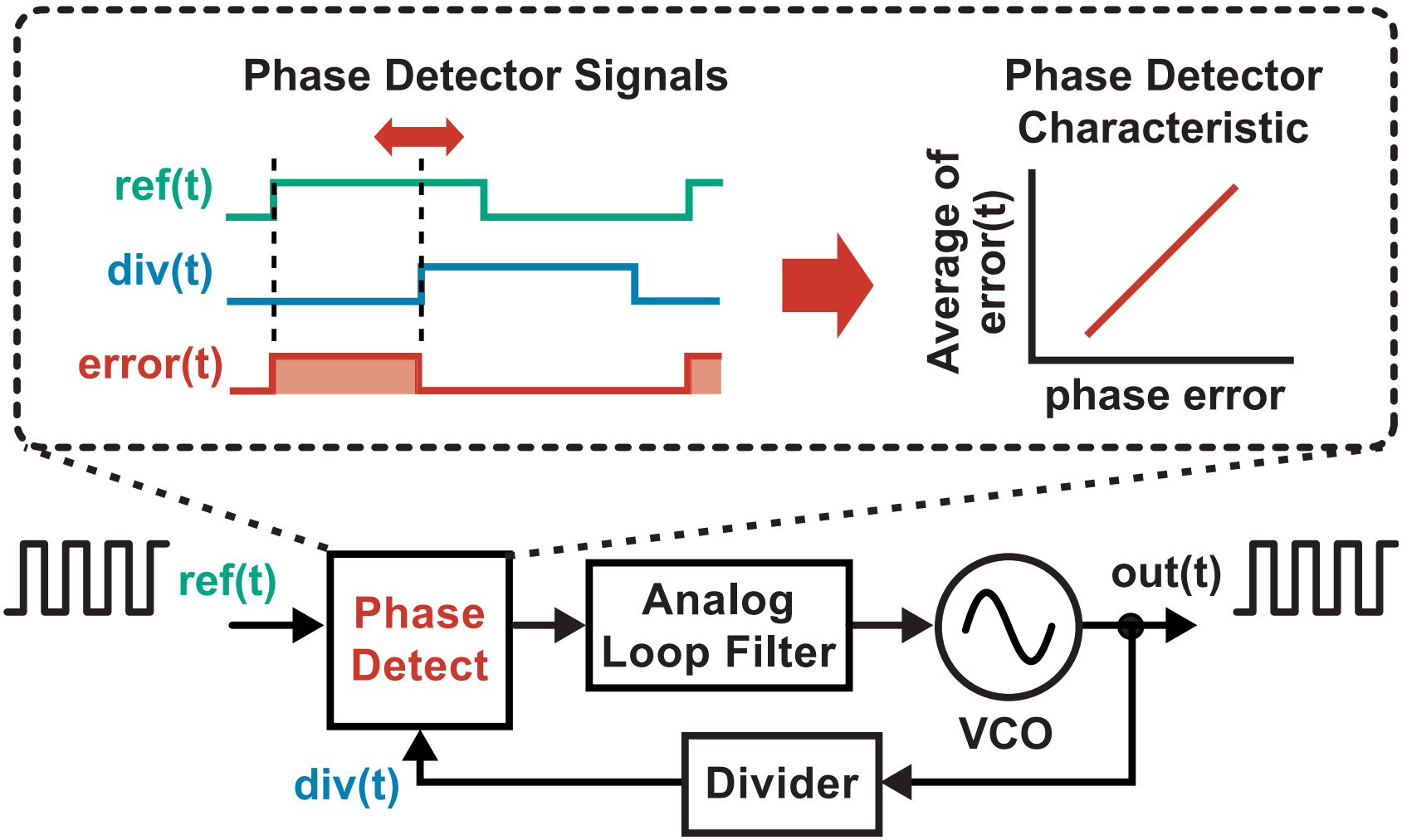
Striving for a Better PLL Implementation

Analog Phase Detection



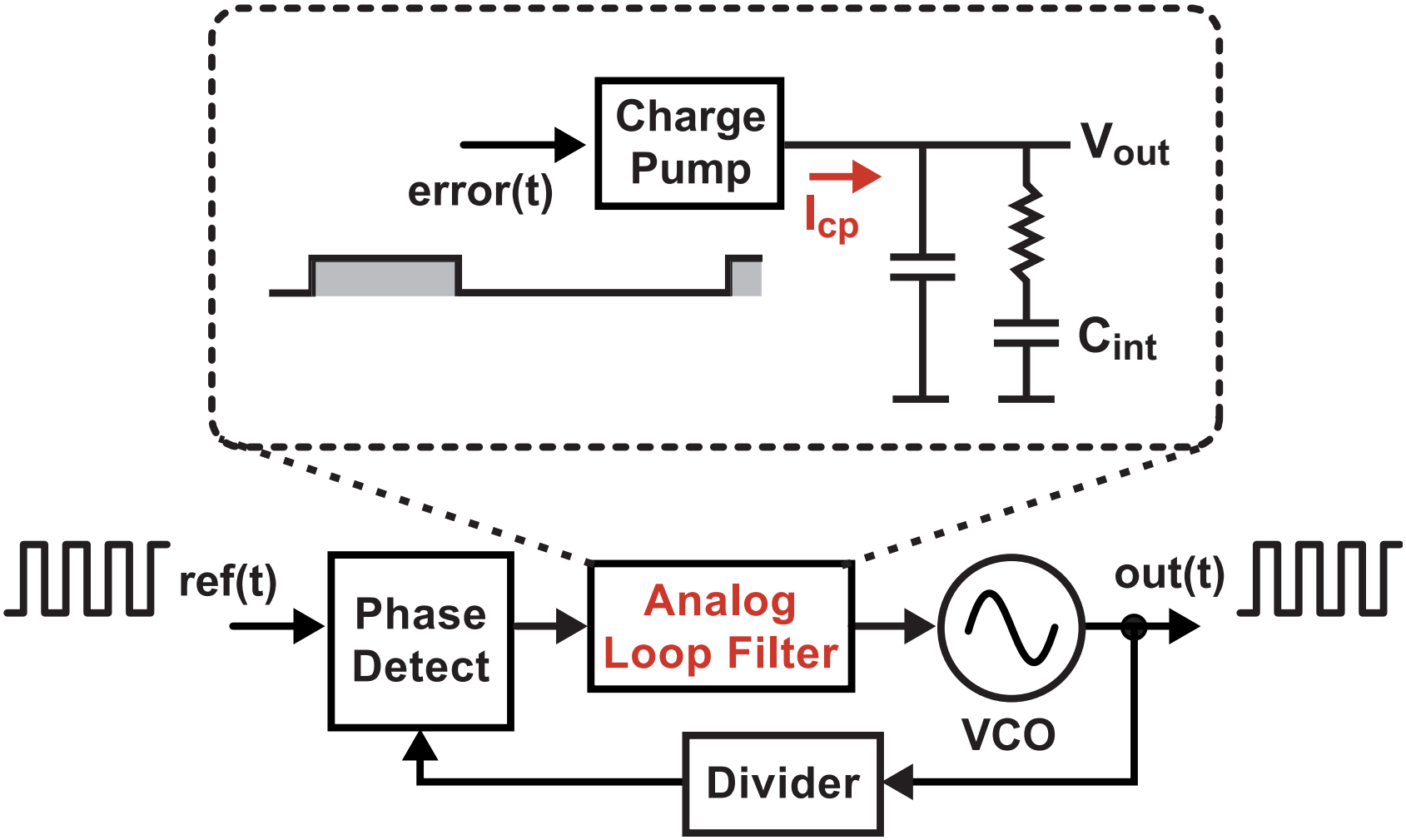
- Pulse width is formed according to phase difference between two signals
- Average of pulsed waveform is applied to VCO input

Tradeoffs of Analog Approach



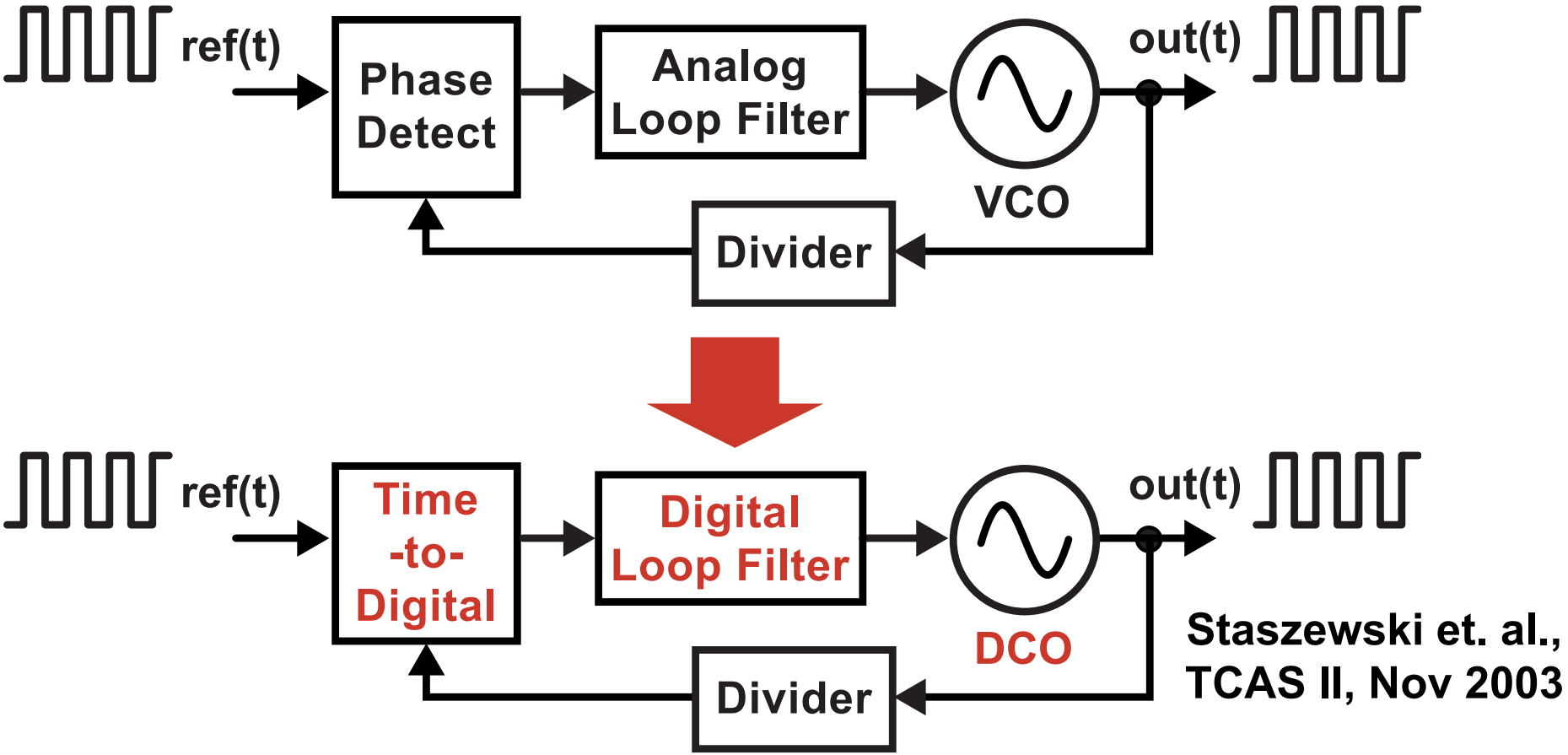
- Benefit: average of pulsed output is a continuous, linear function of phase error
- Issue: analog loop filter implementation is undesirable

Issues with Analog Loop Filter



- Charge pump: output resistance, mismatch
- Filter caps: leakage current, *large area*

Going Digital …

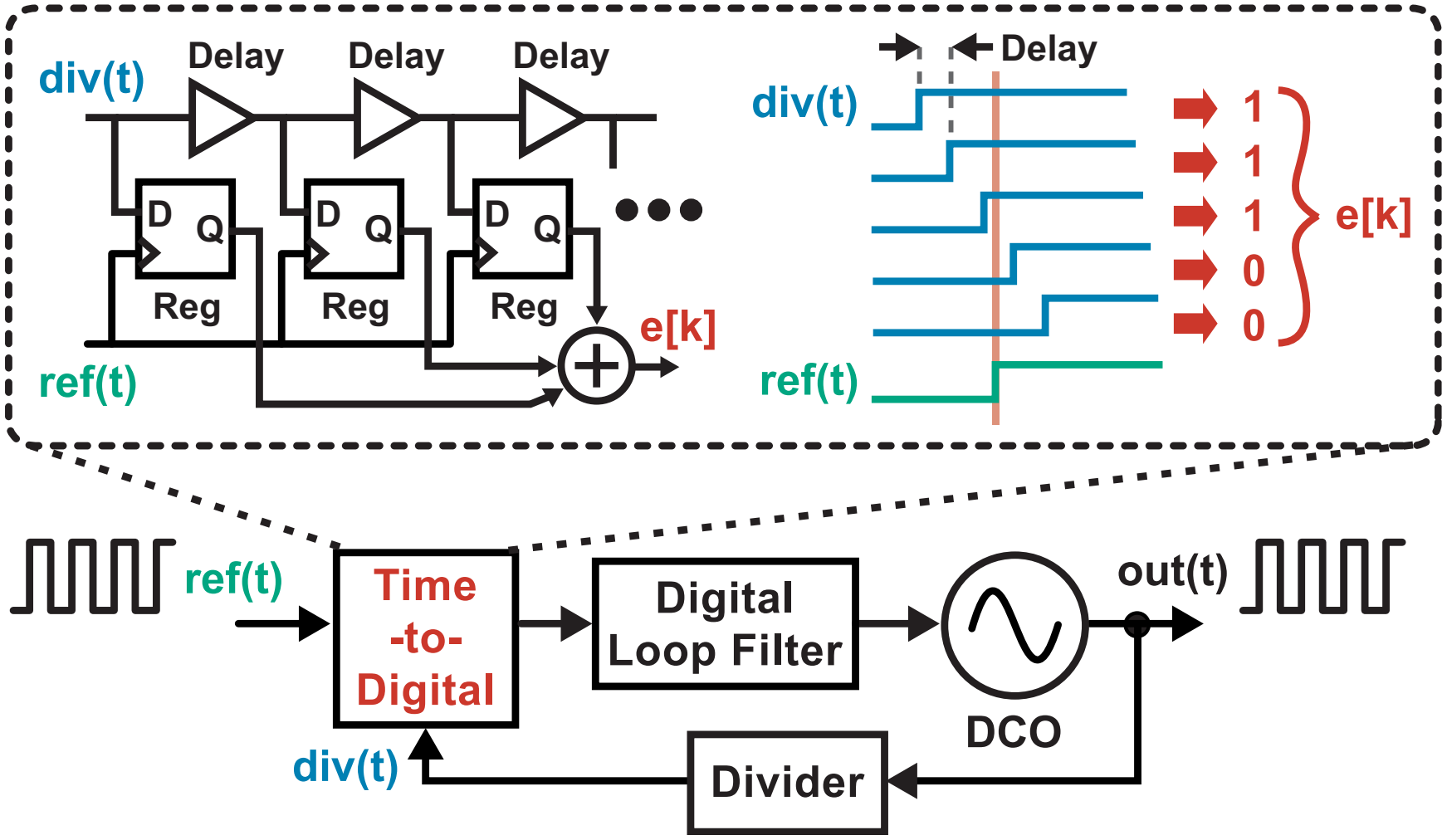


- Digital loop filter: compact area, insensitive to leakage
- Challenges:
  - Time-to-Digital Converter (TDC)
  - Digitally-Controlled Oscillator (DCO)

Outline of Talk

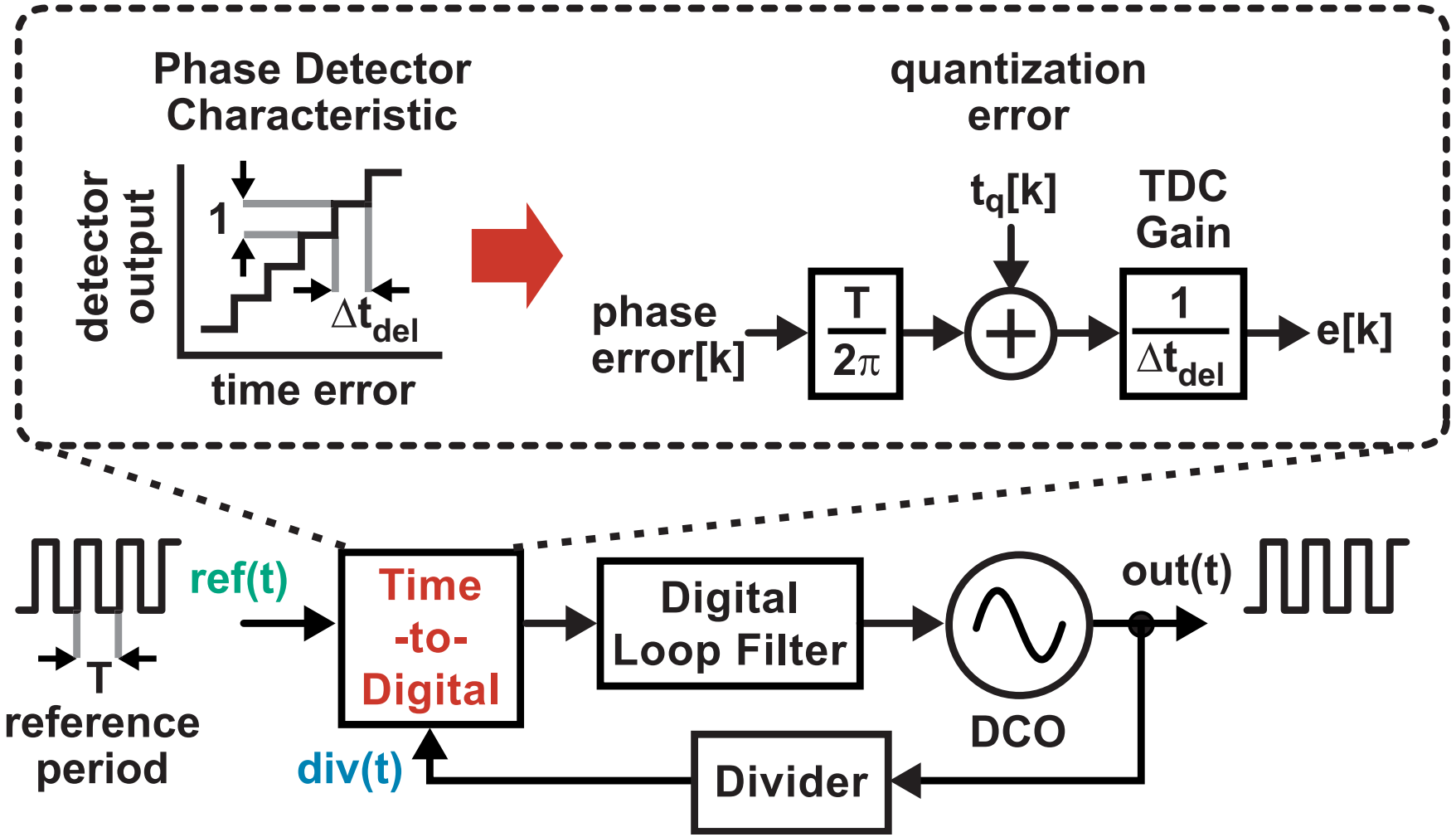
- **Basics**
  - **Time-to-Digital Converters (TDCs)**
  - **Digitally-Controlled Oscillators (DCOs)**
- **Modeling**
  - **Transfer function modeling**
  - **Noise analysis**
- **Improving the TDC**
  - **Background**
  - **Gated-Ring Oscillator (GRO) structure**
- **A high performance digital PLL example**
  - **GRO TDC for low noise**
  - **Quantization noise cancellation**
  - **Low jitter divider design**

Classical Time-to-Digital Converter



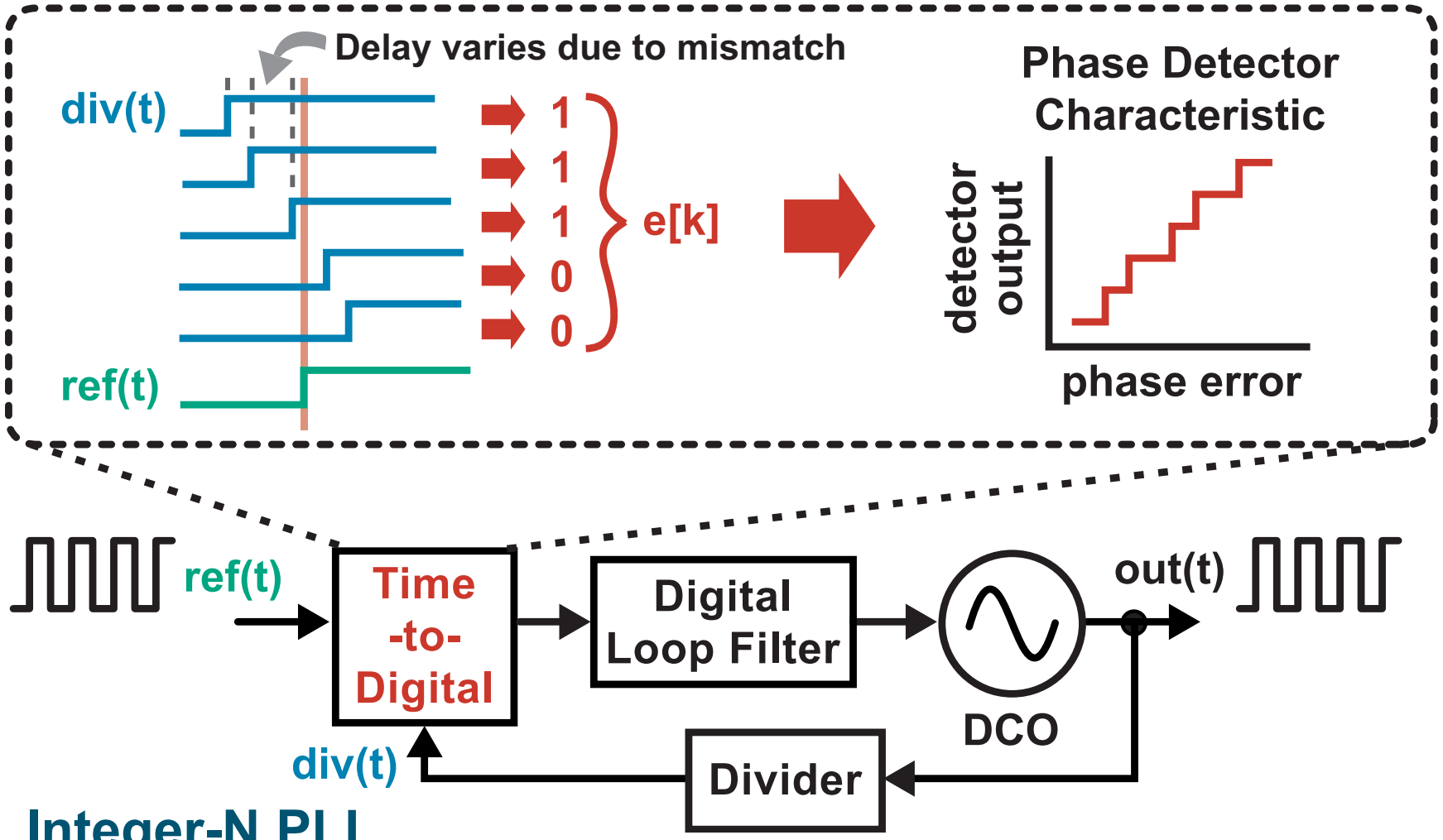
- Resolution set by a “Single Delay Chain” structure
  - Phase error is measured with delays and registers
- Corresponds to a flash architecture

Modeling of TDC



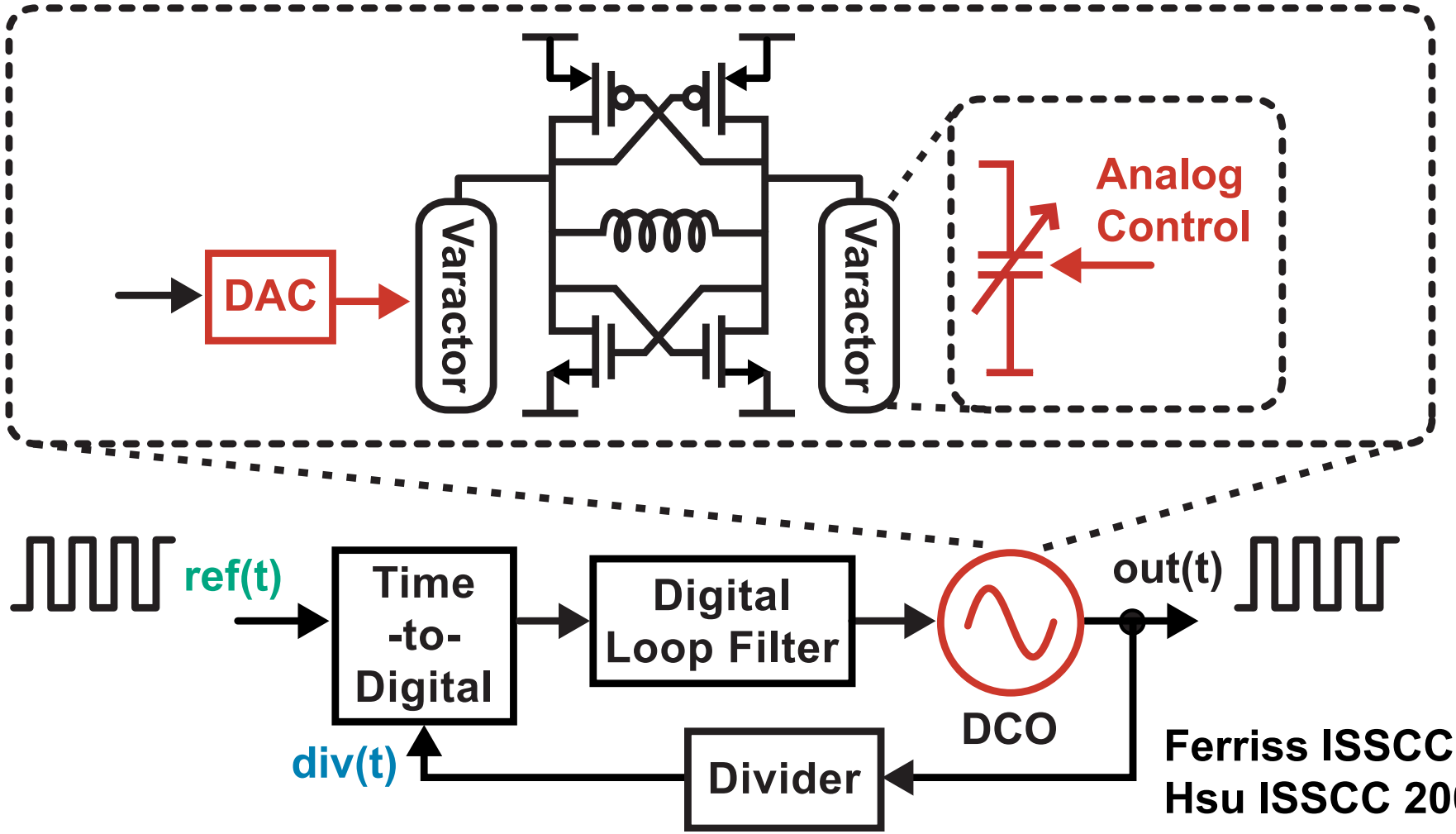
- Phase error converted to time error by scale factor: $T/2\pi$
- TDC introduces quantization error: $t_q[k]$
- TDC gain set by average delay per step: Δt_{del}

Impact of Limited Resolution and Delay Mismatch



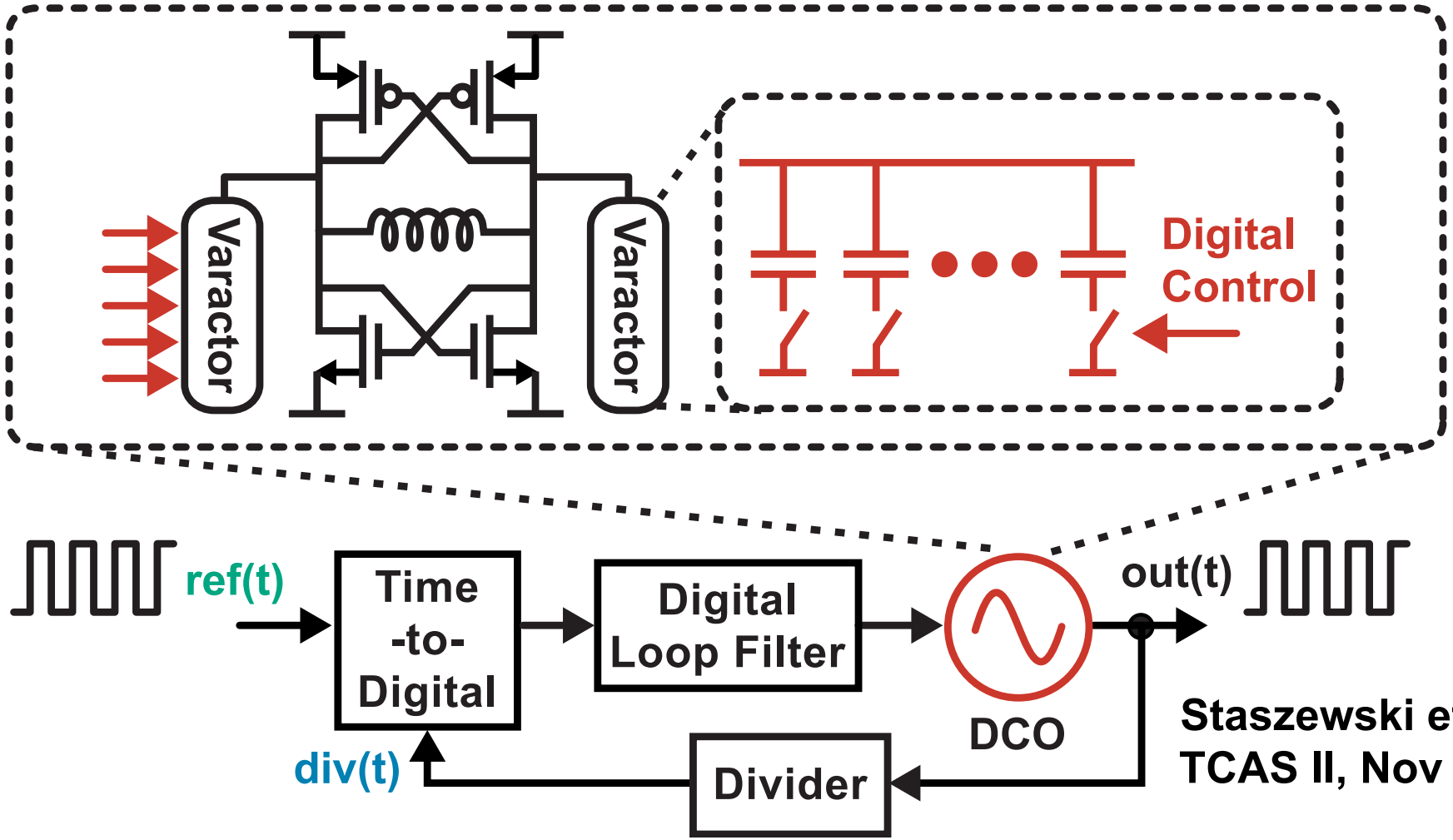
- Integer-N PLL
  - Limit cycles due to limited resolution (unless high ref noise)
- Fractional-N PLL
  - Fractional spurs due to non-linearity from delay mismatch

A Straightforward Approach for Achieving a DCO



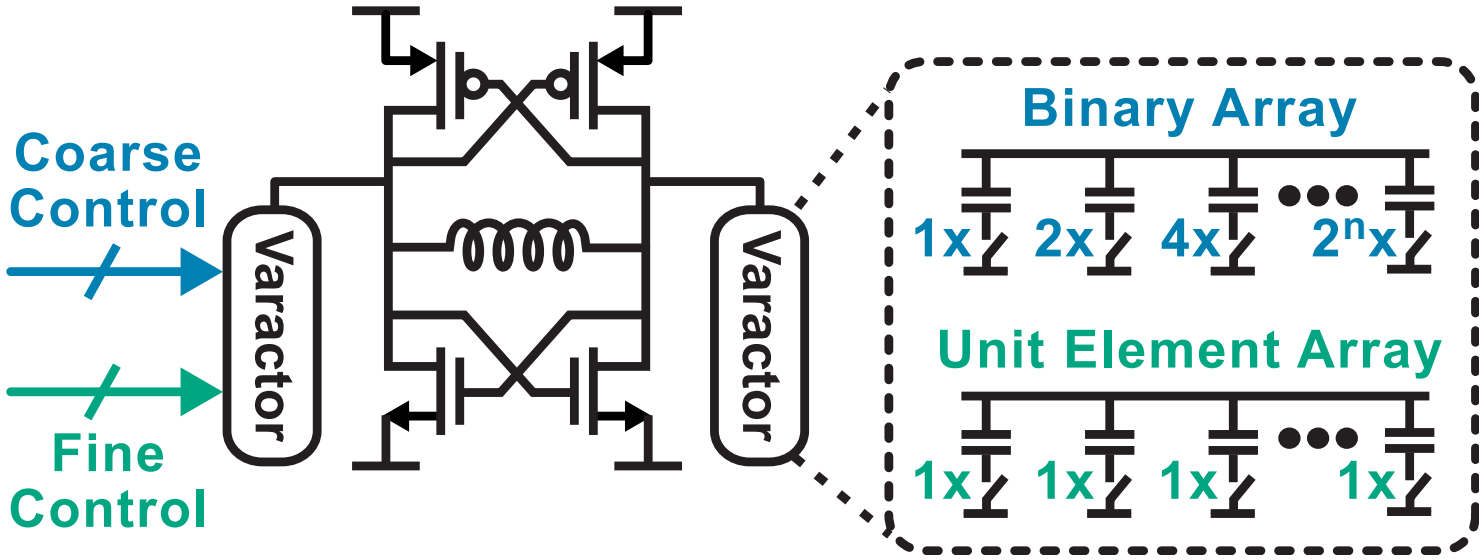
- Use a DAC to control a conventional LC oscillator
  - Allows the use of an existing VCO within a digital PLL
  - Can be applied across a broad range of IC processes

A Much More Digital Implementation



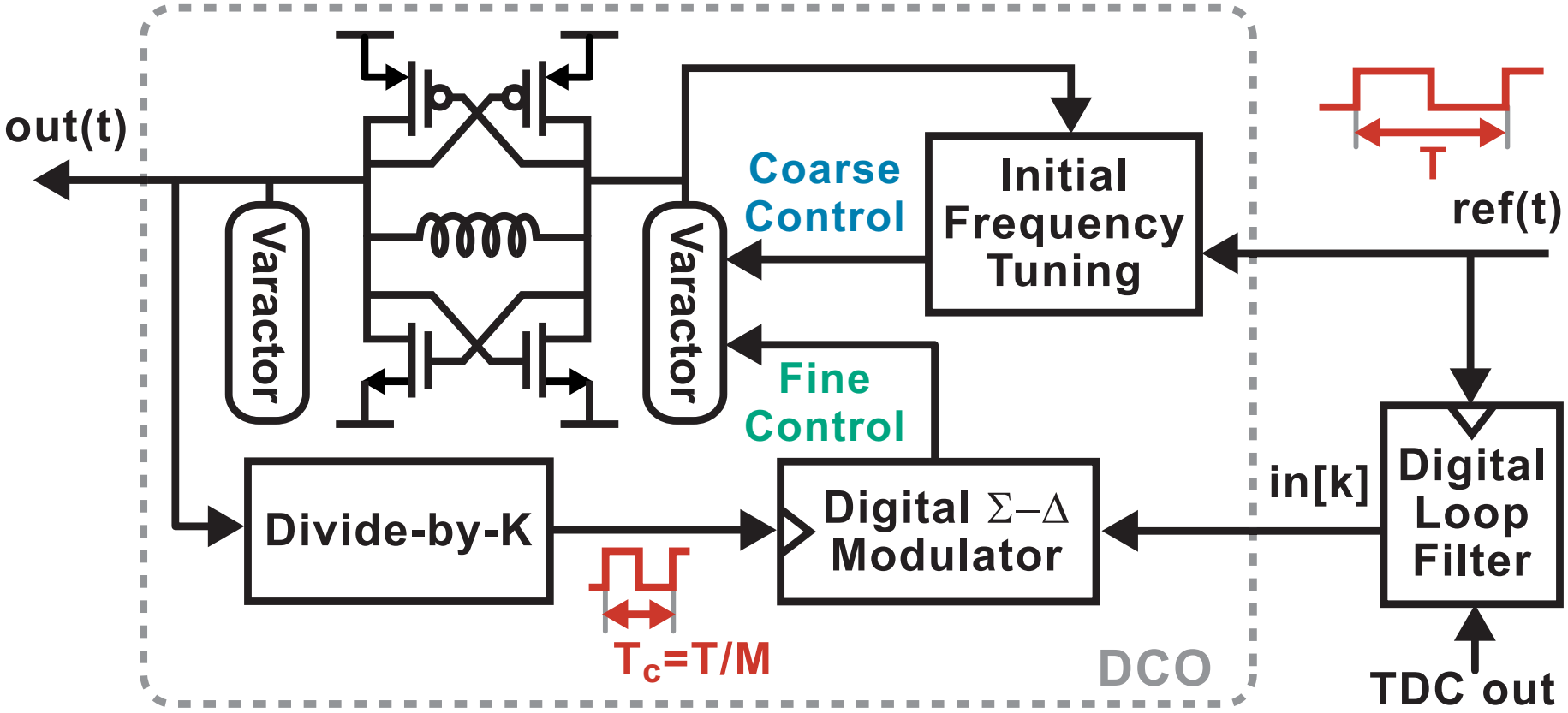
- Adjust frequency in an LC oscillator by switching in a variable number of small capacitors
  - Most effective for CMOS processes of 0.13u and below

Leveraging Segmentation in Switched Capacitor DCO



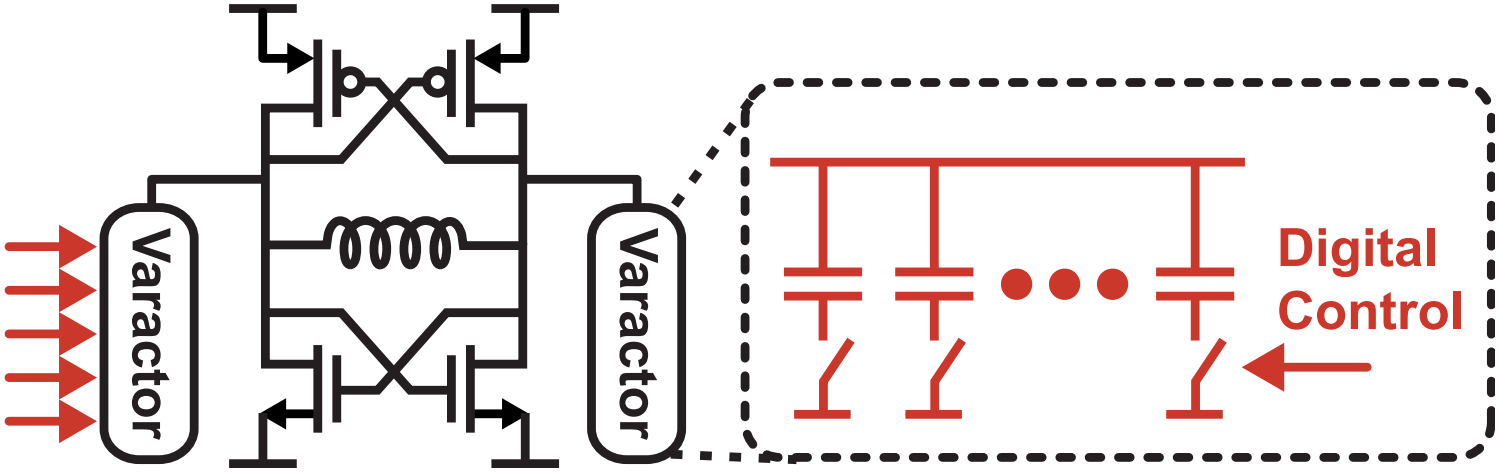
- **Similar tradeoffs as *segmented* capacitor DAC structures**
  - **Binary array: efficient control, but may lack monotonicity**
  - **Unit element array: monotonic, but complex control**
- **Coarse and fine control segmentation of DCO**
  - **Coarse control: active only during initial frequency tuning**
    - Binary array provides efficient control implementation
  - **Fine control: controlled by PLL feedback**
    - Unit element array minimizes dynamic charge transfer

Leveraging Dithering for Fine Control of DCO

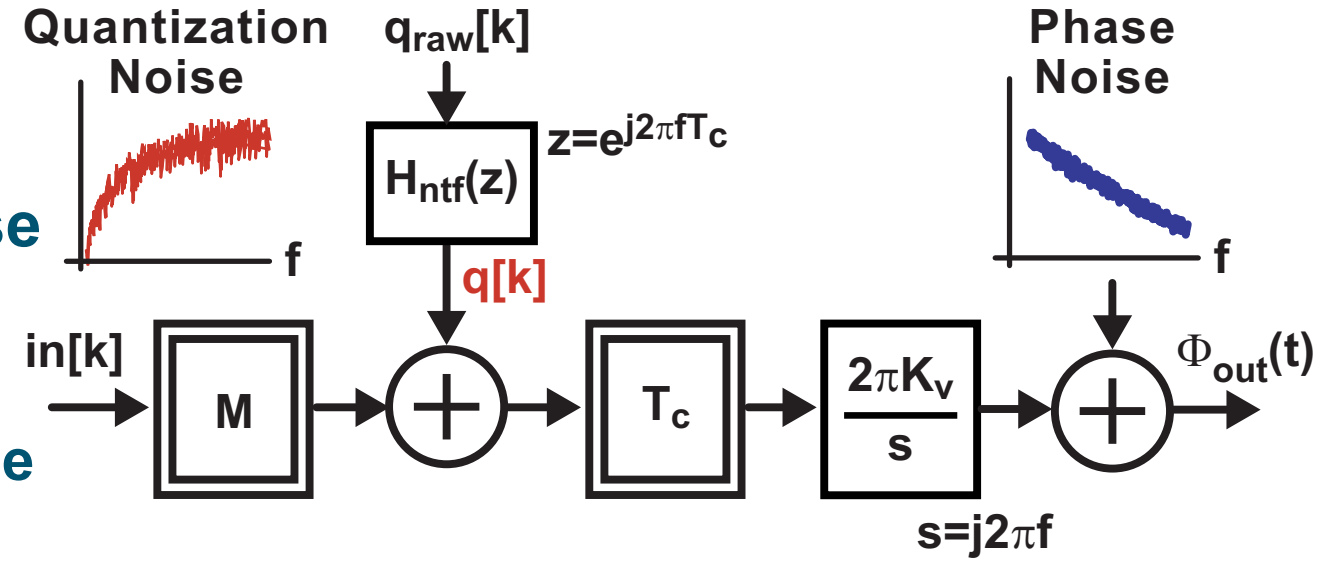


- Increase resolution by Σ–Δ dithering of fine cap array
- Reduce noise from dithering by
  - Using small unit caps in the fine cap array
  - Increasing the dithering frequency (defined as $1/T_c$)
    - Assume $1/T_c = M/T$ (i.e. M times reference frequency)

Noise Spectrum of a Switched Cap DCO

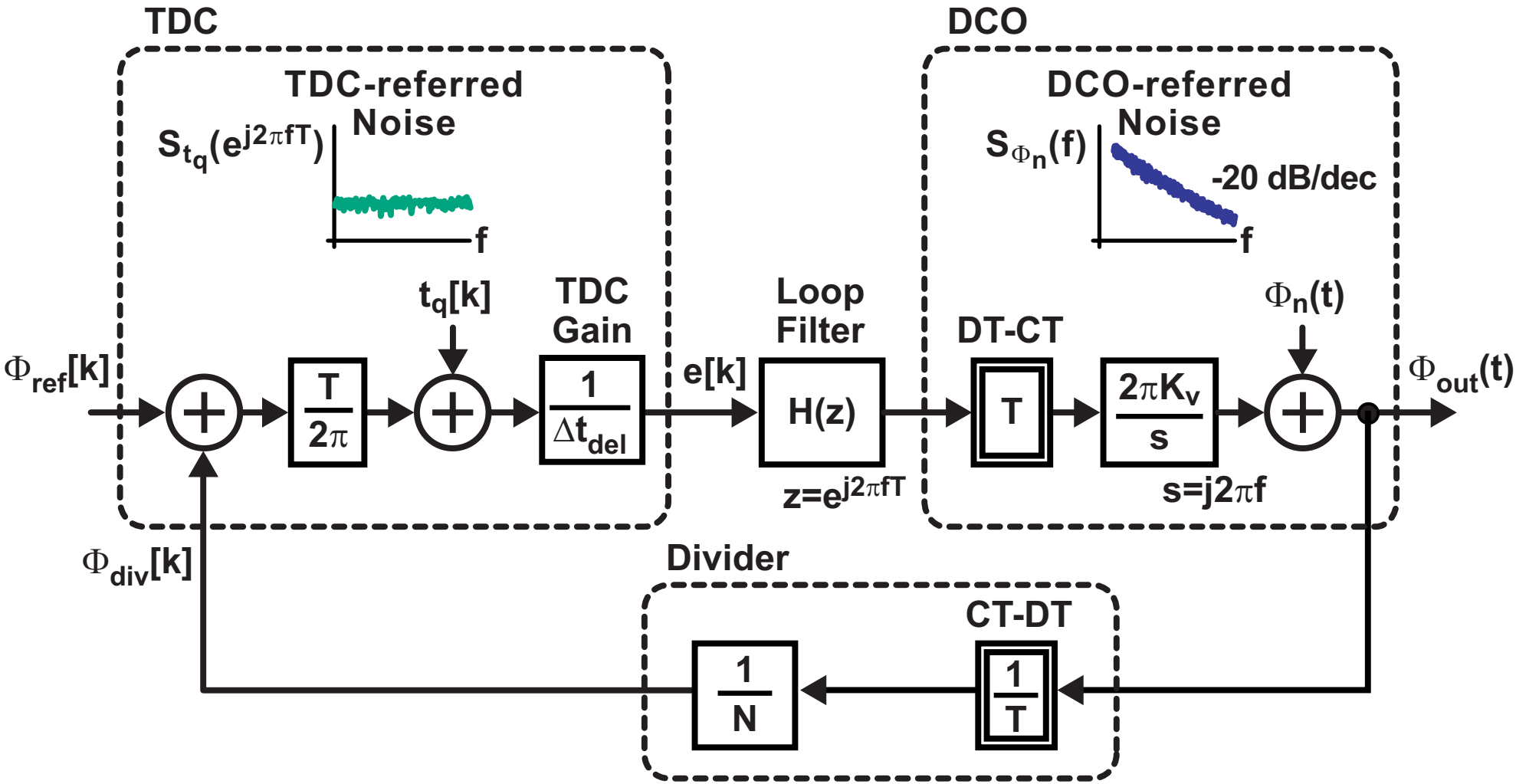


- Phase noise
  - Same as for conventional VCO (tank *Q*, etc.)
- Quantization noise from dithering
  - Designed to be lower than phase noise



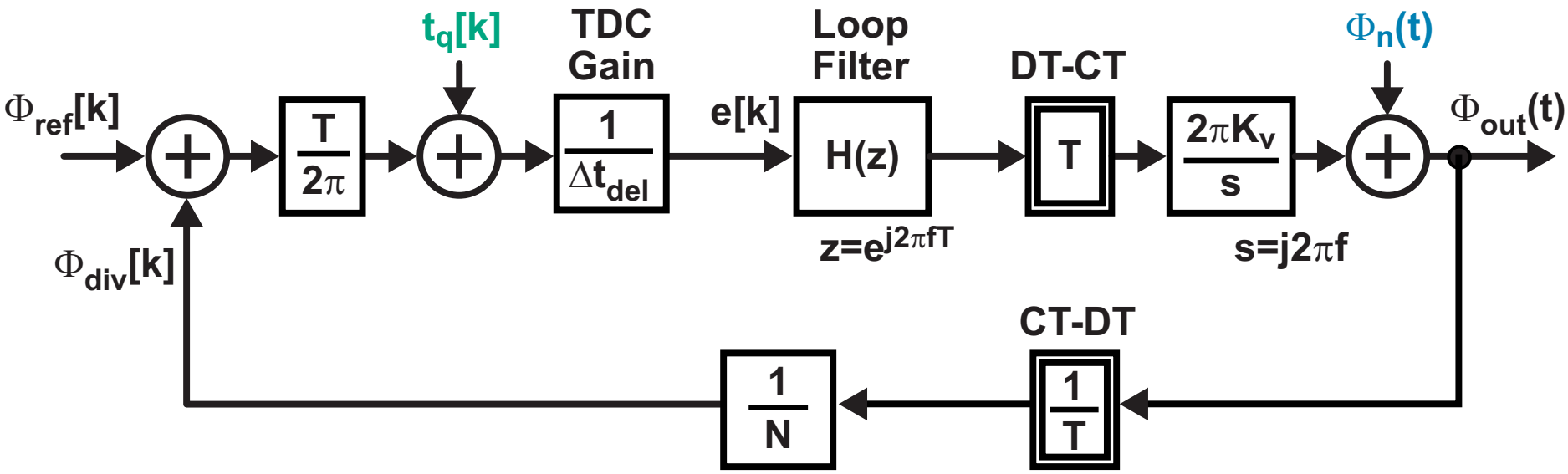
Modeling

Overall Digital PLL Model



- TDC and DCO-referred noise influence overall phase noise according to associated transfer functions to output
- Calculations involve both discrete *and* continuous time

Key Transfer Functions



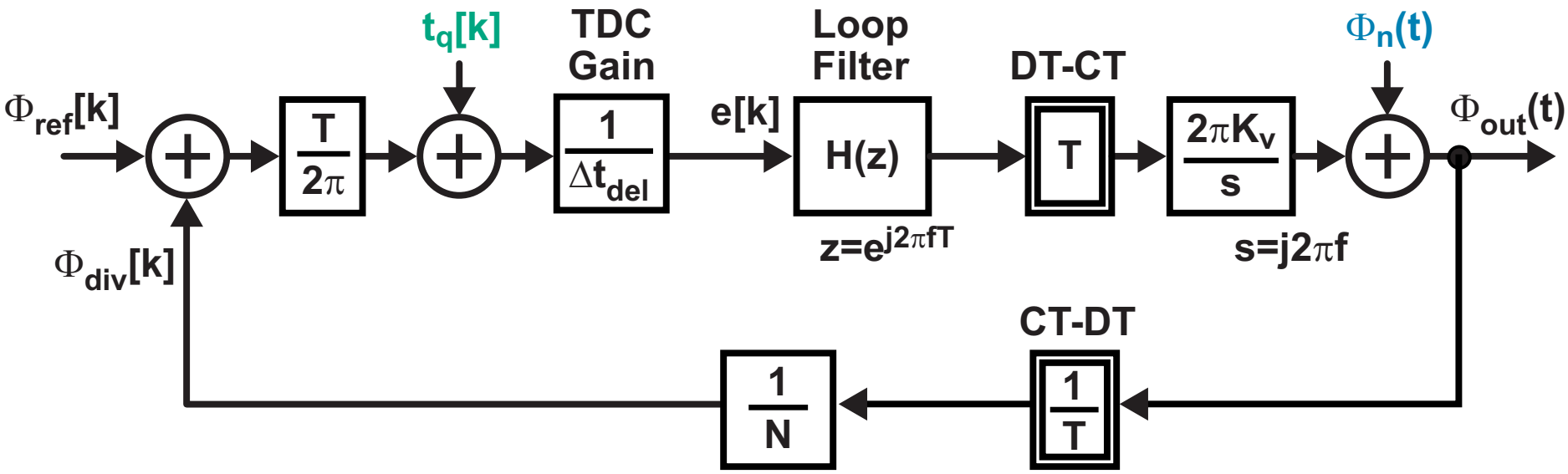
- **TDC-referred noise**

$$\frac{\Phi_{out}}{t_q} = \frac{(1/\Delta t_{del})H(e^{j2\pi fT})T2\pi K_v/(2\pi jf)}{1+(1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

- **DCO-referred noise**

$$\frac{\Phi_{out}}{\Phi_n} = \frac{1}{1+(1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

Utilize G(f) as a Parameterizing Function



- **Define open loop transfer function *A(f)* as:**

$$A(f) = (1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)$$

- **Define closed loop parameterizing function *G(f)* as:**

$$G(f) = \frac{A(f)}{1 + A(f)}$$

  - **Note: *G(f)* is a lowpass filter with DC gain = 1**

Transfer Function Parameterization Calculations

- **TDC-referred noise**

$$\frac{\Phi_{out}}{t_q} = \frac{(1/\Delta t_{del})H(e^{j2\pi fT})T2\pi K_v/(2\pi jf)}{1+(1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

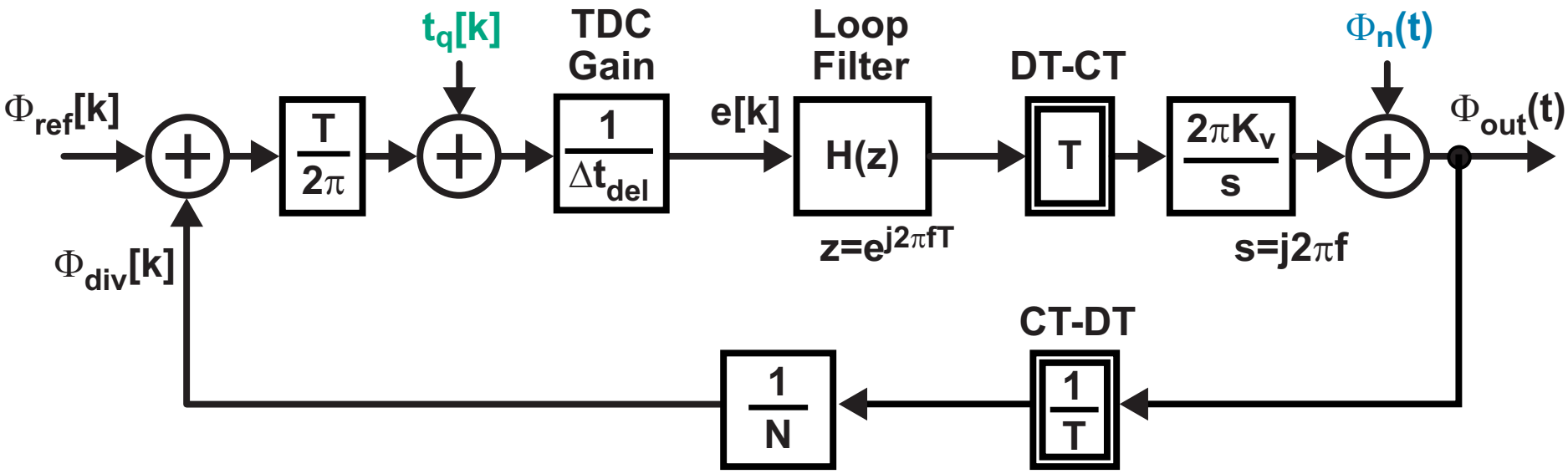
$$= \frac{2\pi NA(f)}{1+A(f)} = \boxed{2\pi NG(f)}$$

- **DCO-referred noise**

$$\frac{\Phi_{out}}{\Phi_n} = \frac{1}{1+(1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

$$= \frac{1}{1+A(f)} = \frac{1+A(f)-A(f)}{1+A(f)} = \boxed{1-G(f)}$$

Key Observations



- **TDC-referred noise**

$$\frac{\Phi_{out}}{t_q} = 2\pi N G(f)$$

Lowpass with a DC gain of 2πN

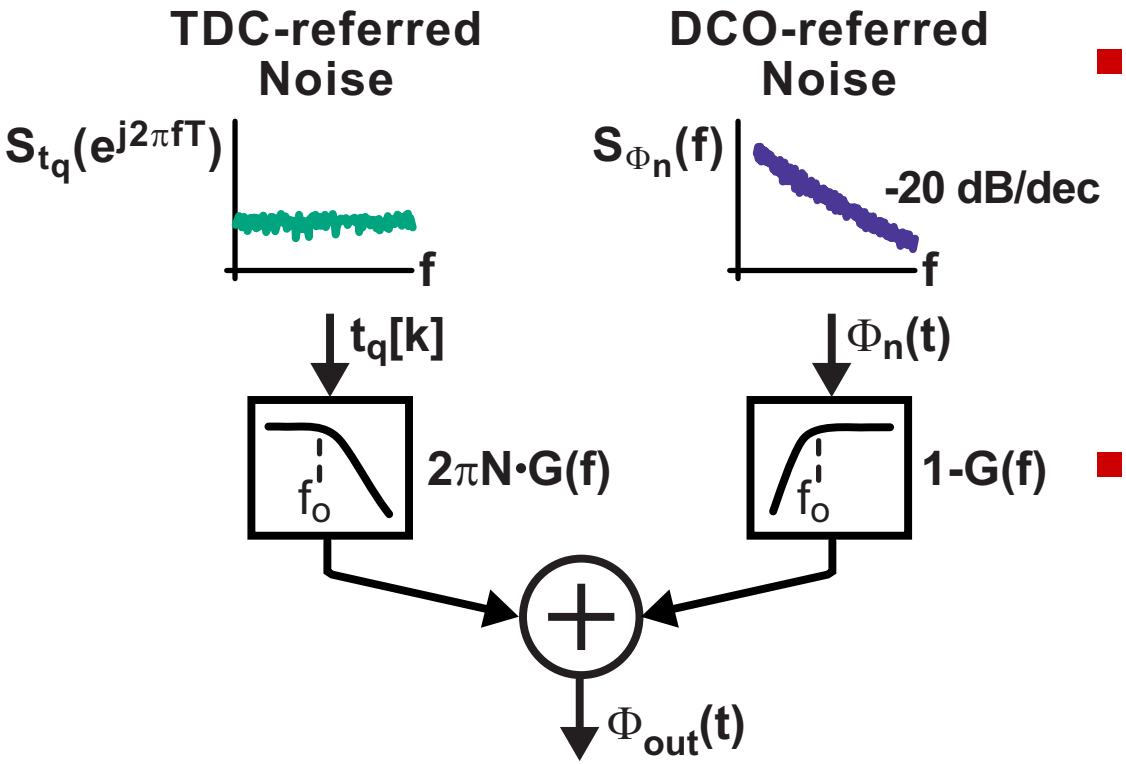
- **DCO-referred noise**

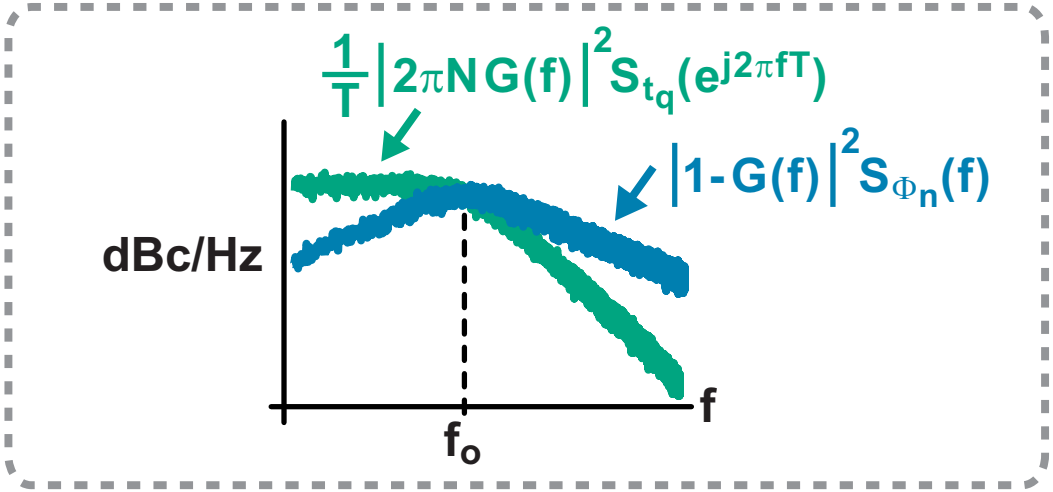
$$\frac{\Phi_{out}}{\Phi_n} = 1 - G(f)$$

Highpass with a high frequency gain of 1

How do we calculate the output phase noise?

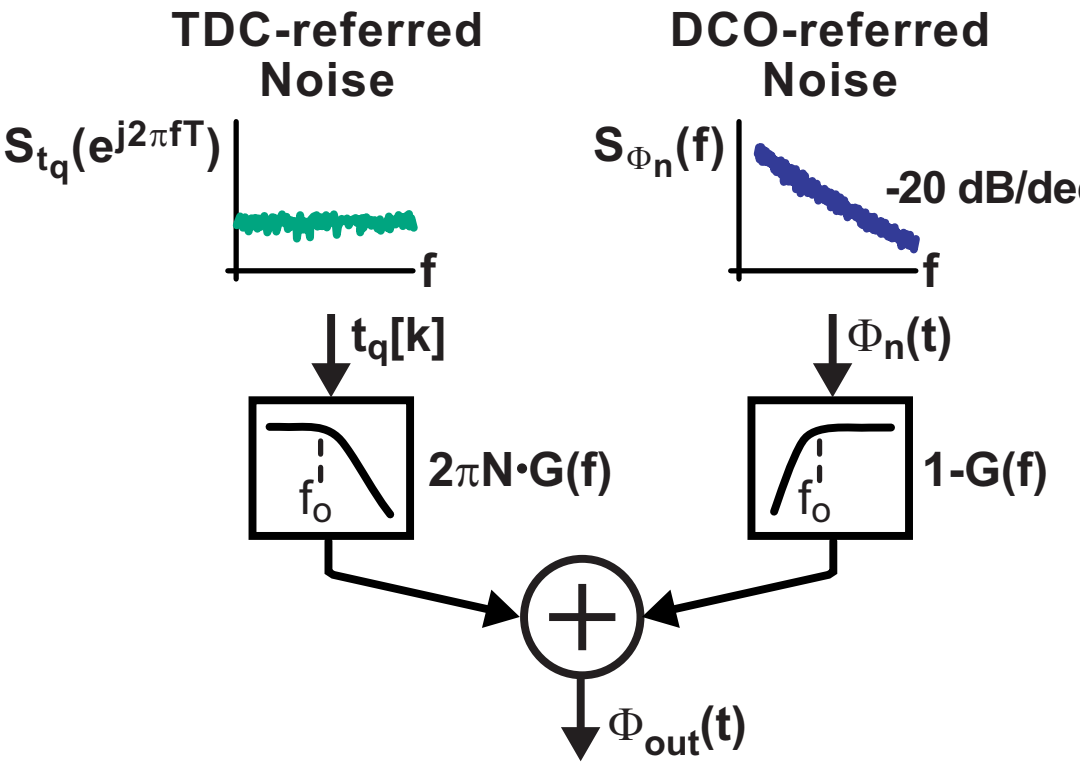
Phase Noise Calculation





- **TDC noise**
  - Dominates PLL phase noise at low frequency offsets
- **DCO noise**
  - Dominates PLL phase noise at high frequency offsets

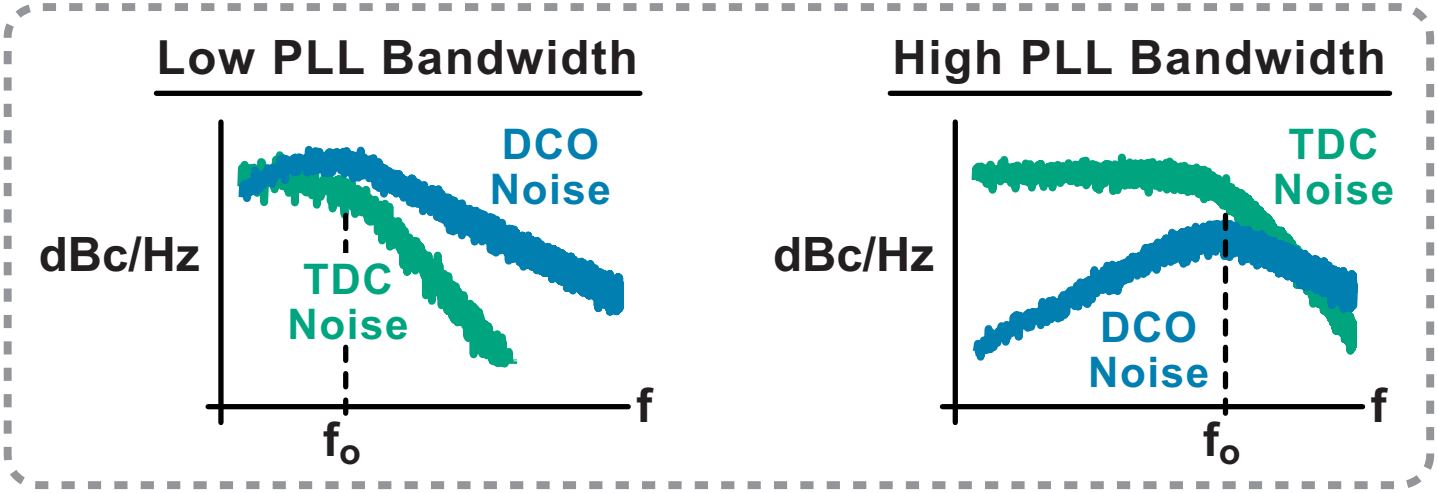
A Closer Look at the Influence of TDC Noise



- **PLL bandwidth dramatically influences relative impact of TDC and VCO noise**

Want high PLL bandwidth?

➡ **Need low TDC Noise**

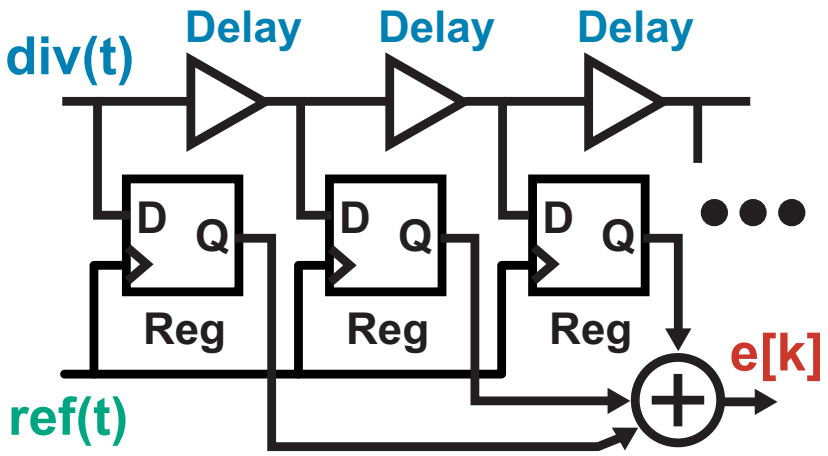


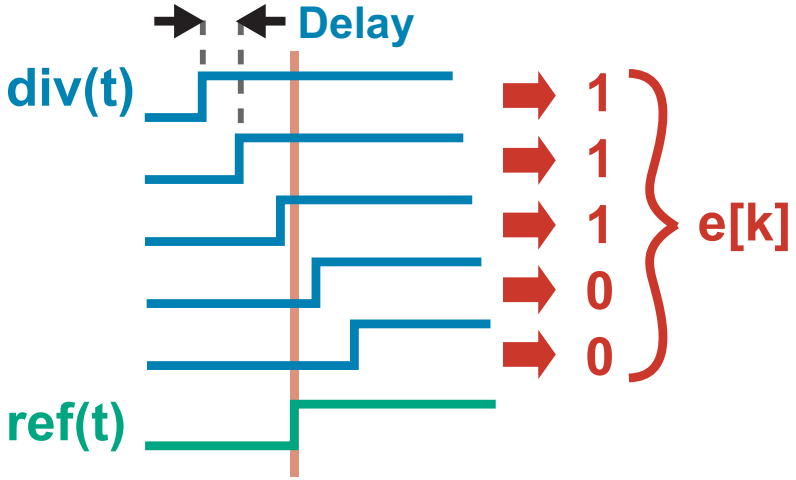
How Do We Improve TDC Performance?

Two Key Issues:

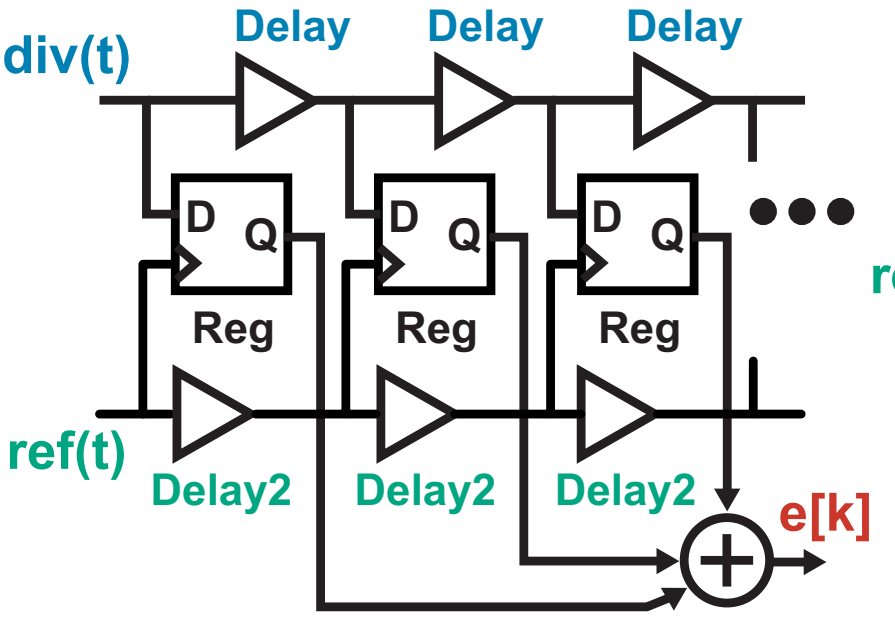
- **TDC resolution**
- **Mismatch**

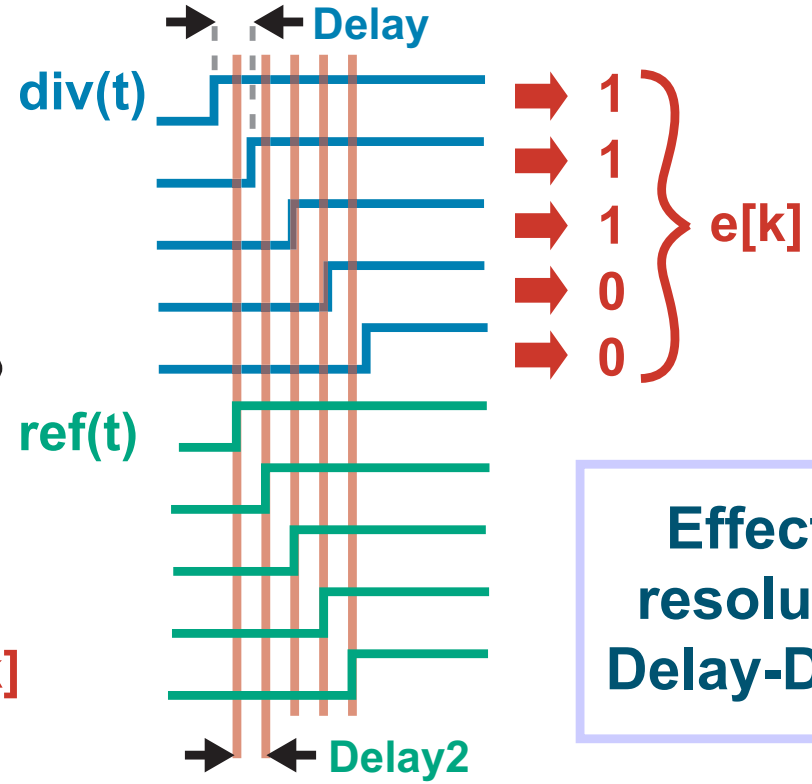
Improve Resolution with Vernier Delay Technique





Vernier

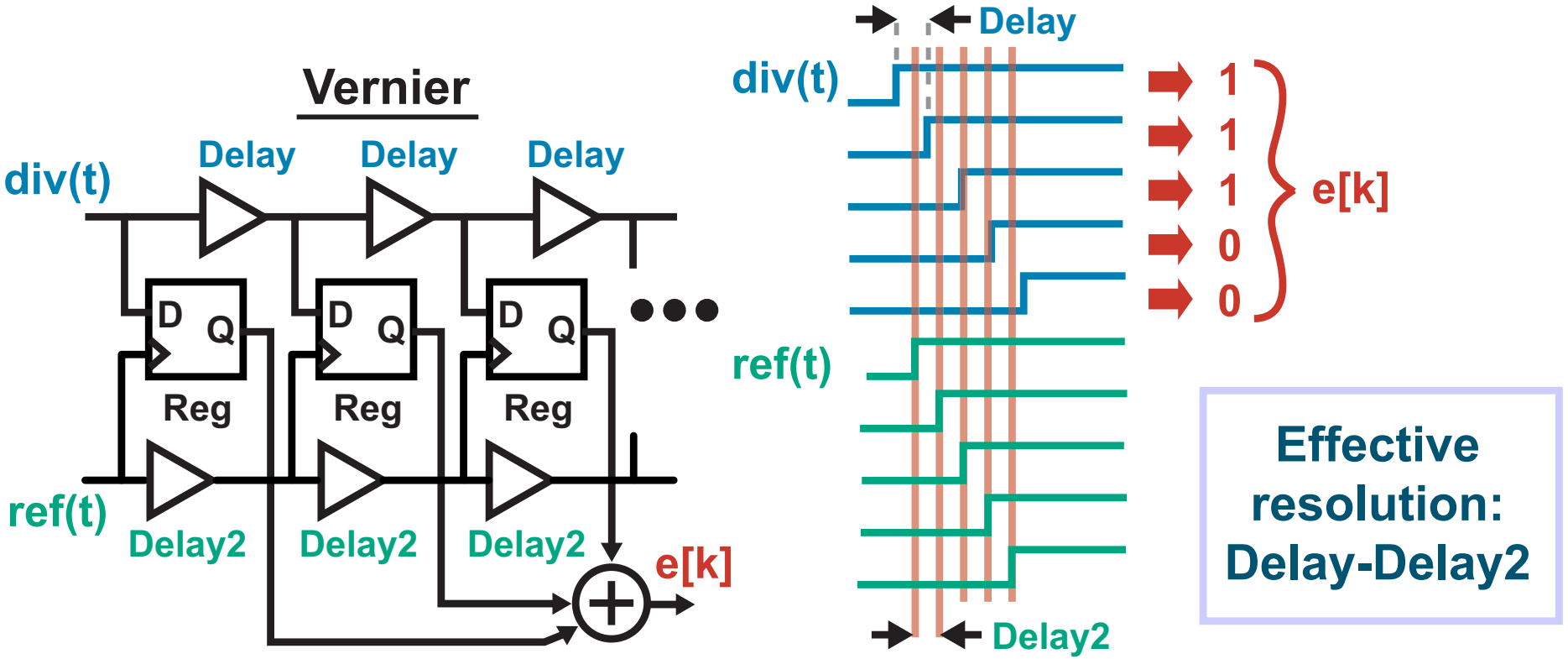




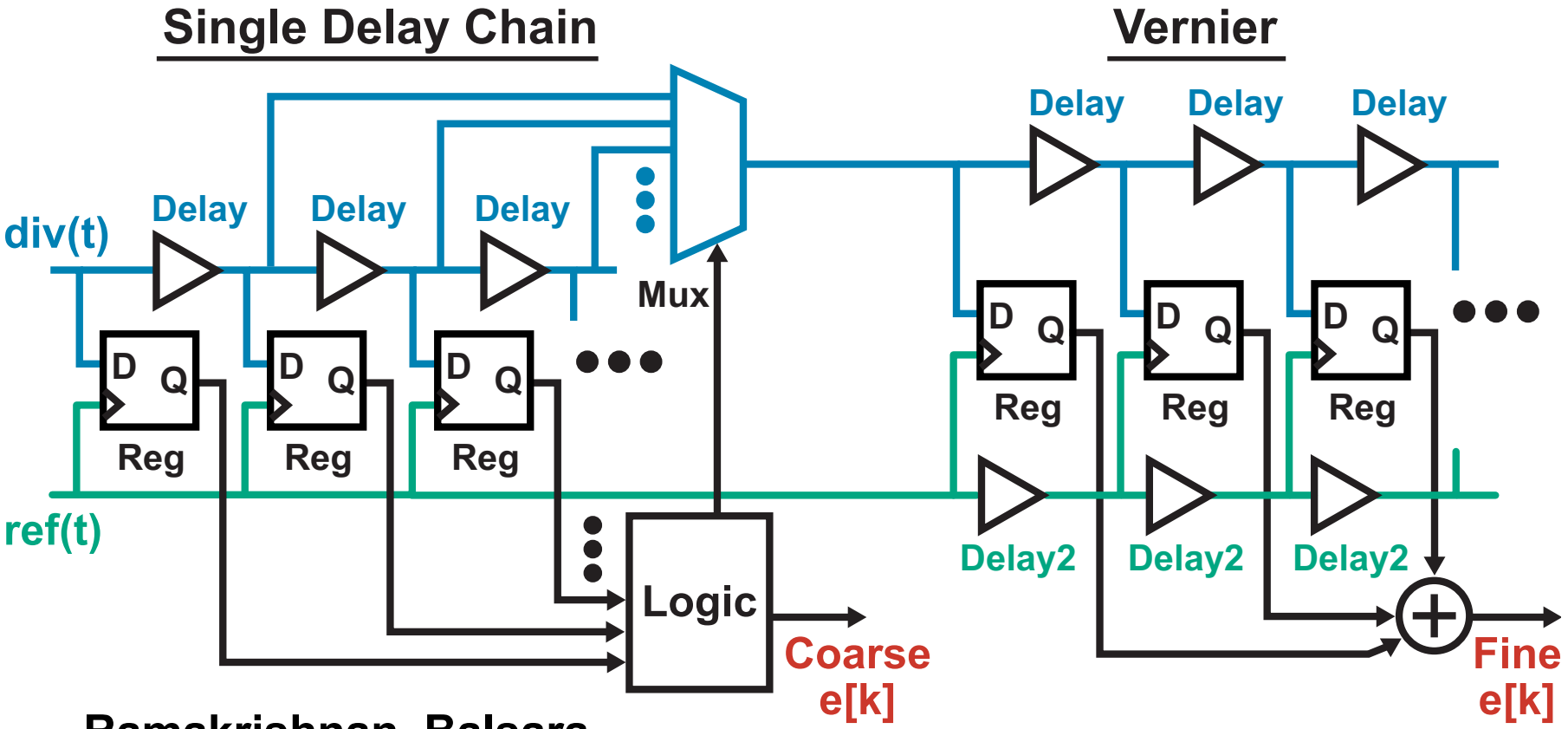
Effective resolution: Delay-Delay2

Issues with Vernier Approach

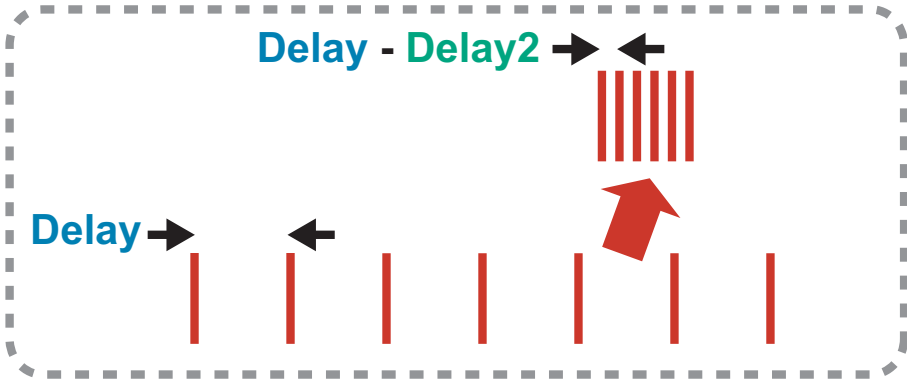
- **Mismatch issues are more severe than the single delay chain TDC**
  - **Reduced delay is formed as *difference* of two delays**
- **Large measurement range requires large area**
  - **Initial PLL frequency acquisition may require a large range**



Two-Step TDC Architecture Allows Area Reduction

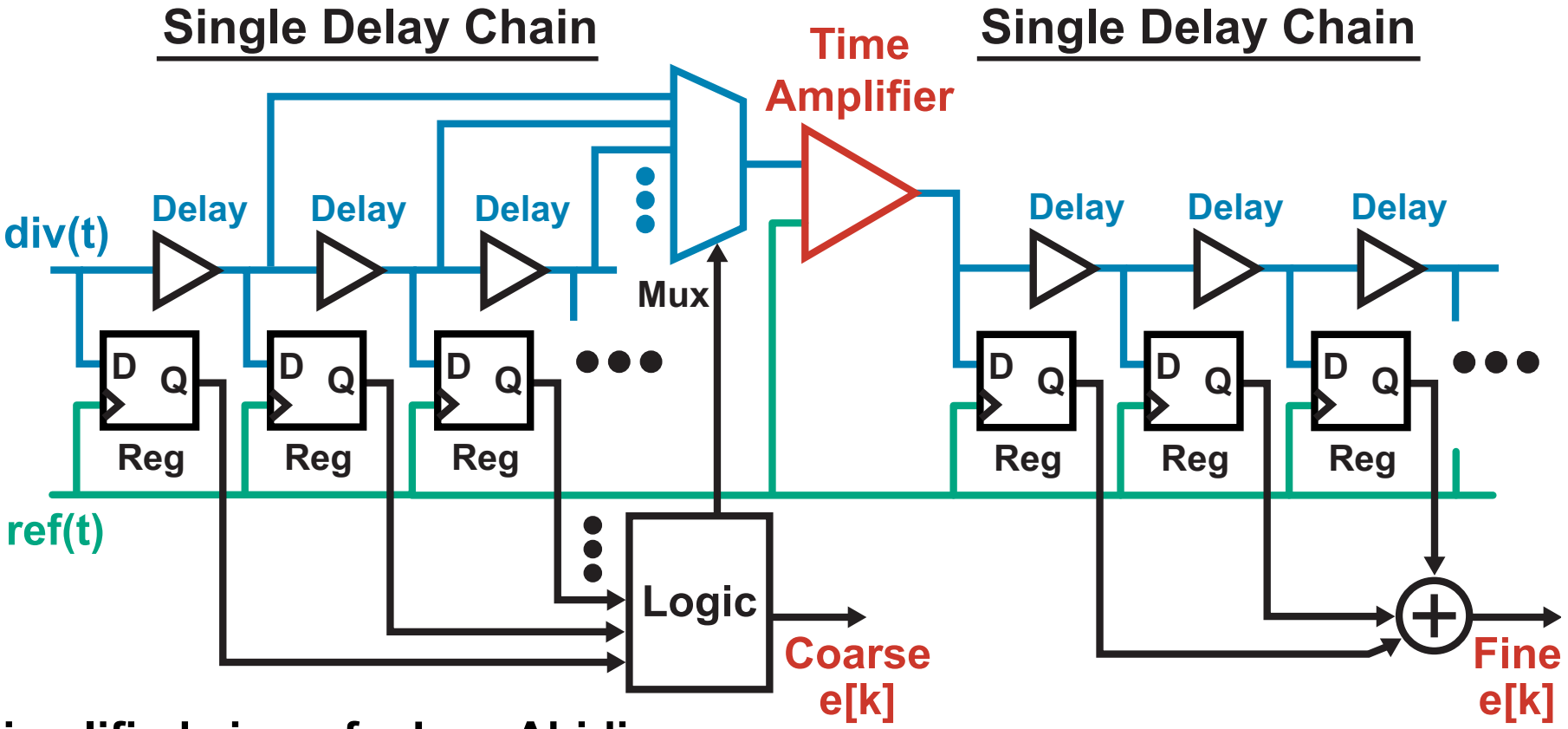


Ramakrishnan, Balsara
VLSID '06

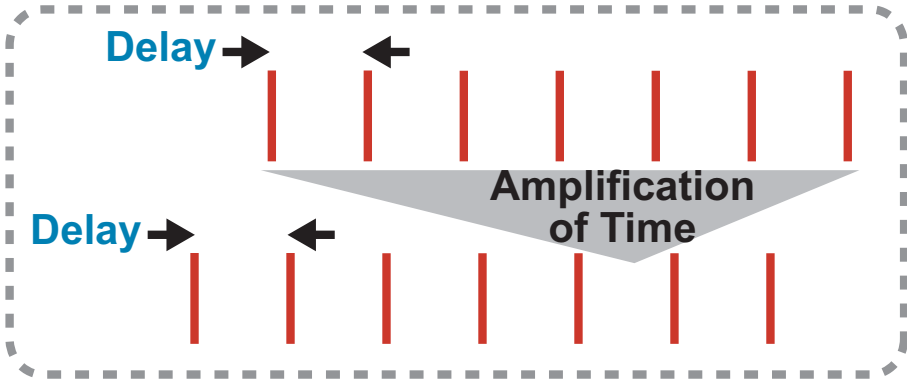


- Single delay chain provides coarse resolution
- (Folded) Vernier provides fine resolution

Two-Step TDC Using Time Amplification

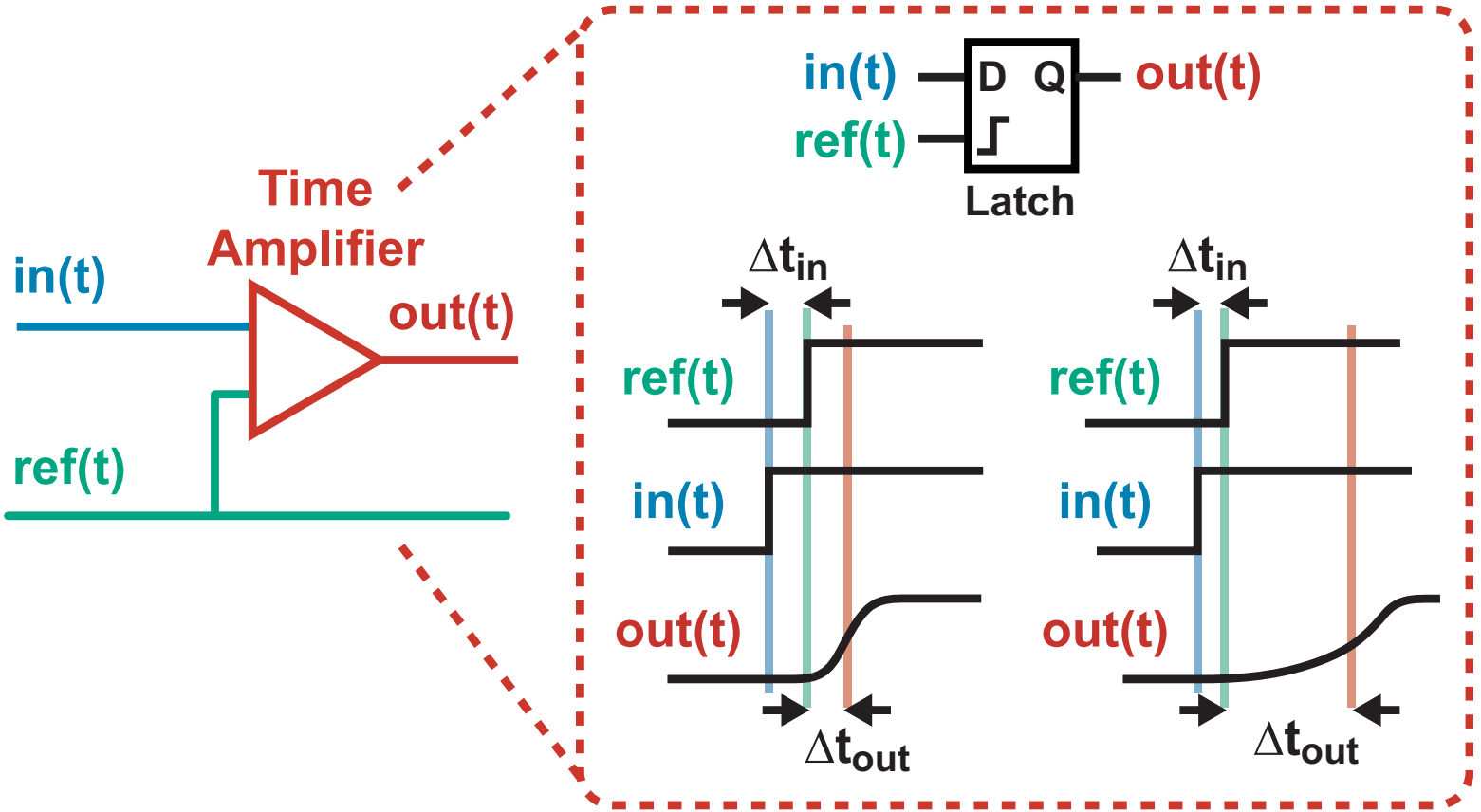


Simplified view of: Lee, Abidi VLSI 2007



- Single delay chain provides coarse and fine resolution
- Time amplification is used to improve resolution

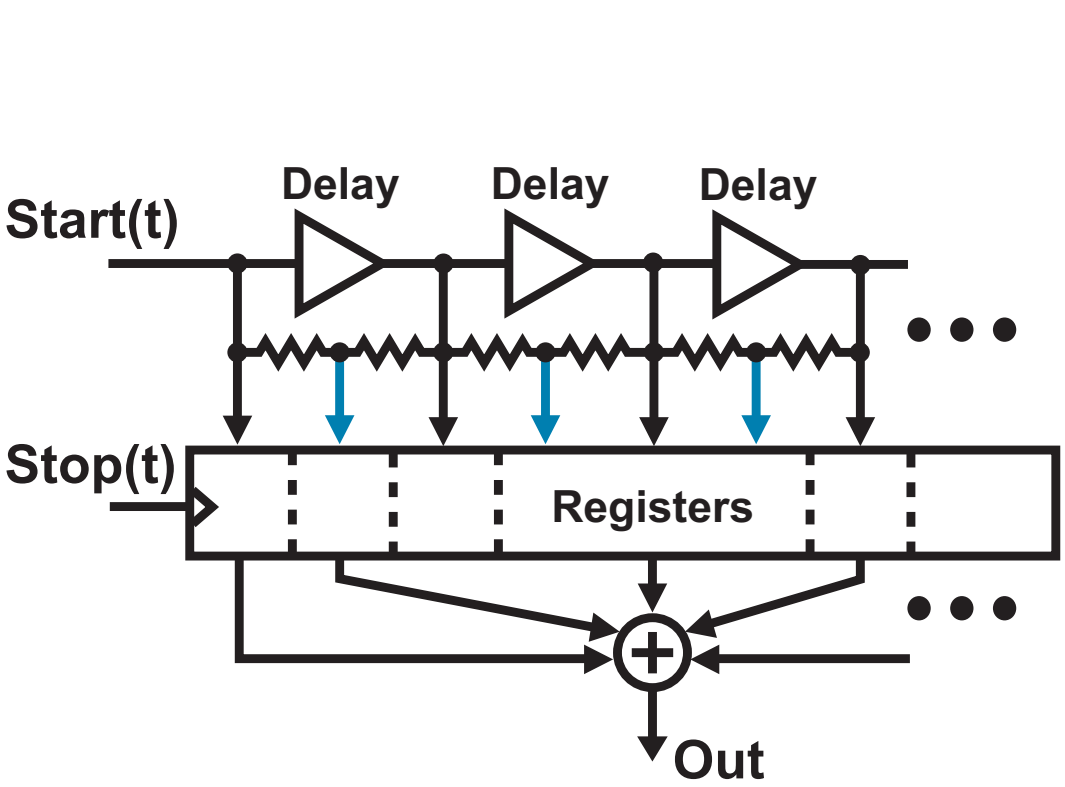
Leveraging Metastability to Create a Time Amplifier



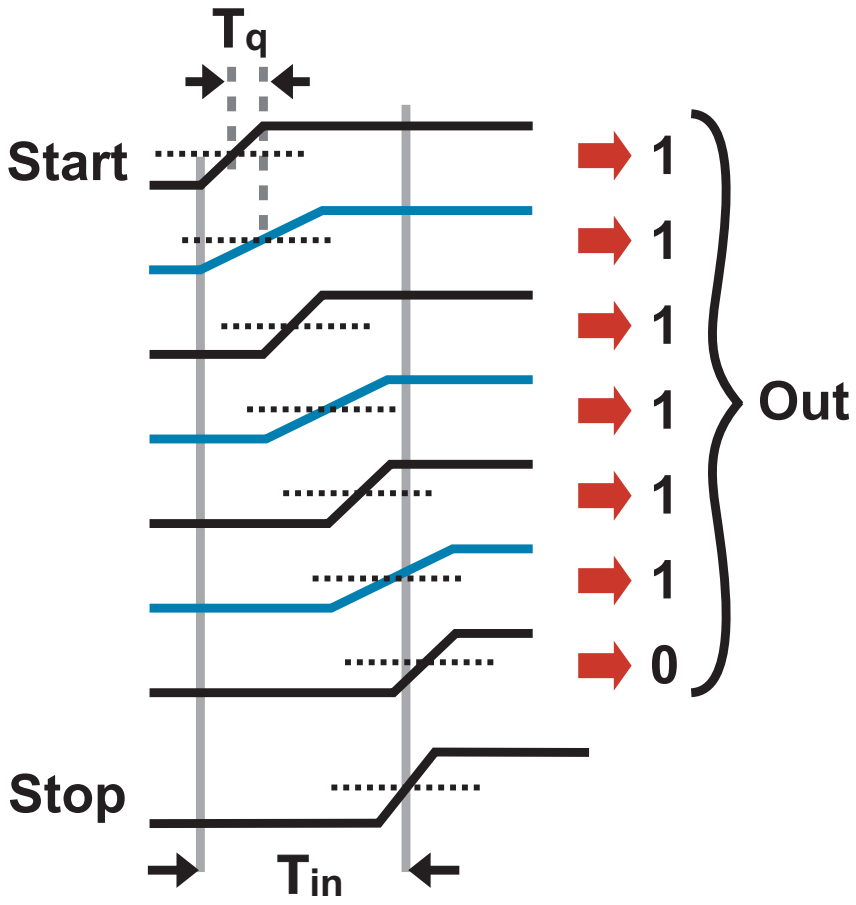
Simplified view of: Abas, et al., Electronic Letters, Nov 2002
(note that actual implementation uses SR latch)

- **Metastability leads to progressively slower output transitions as setup time on latch is encroached upon**
  - **Time difference at input is amplified at output**

Interpolating time-to-digital converter

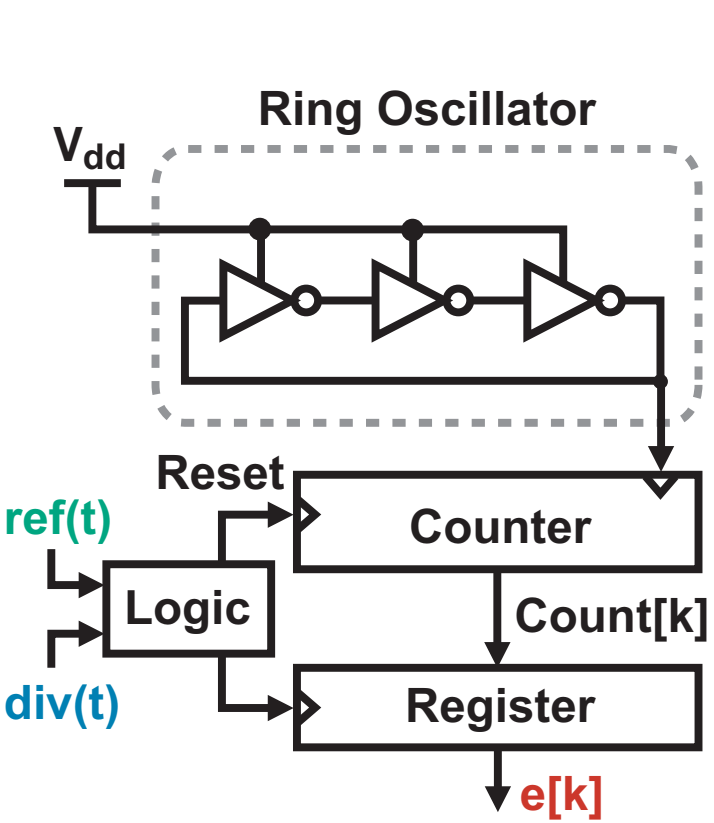


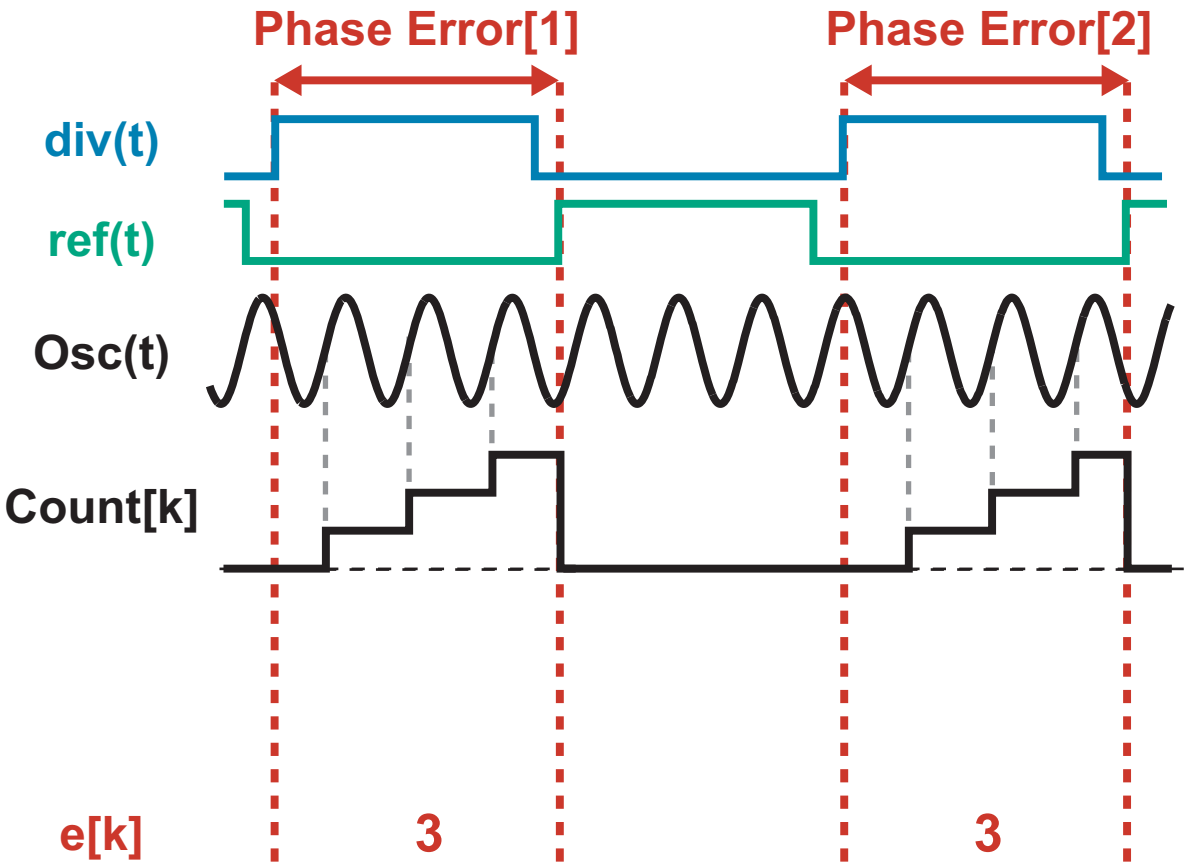
Henzler et al., ISSCC 2008



- Interpolate between edges to achieve fine resolution
- Cyclic approach can also be used for large range

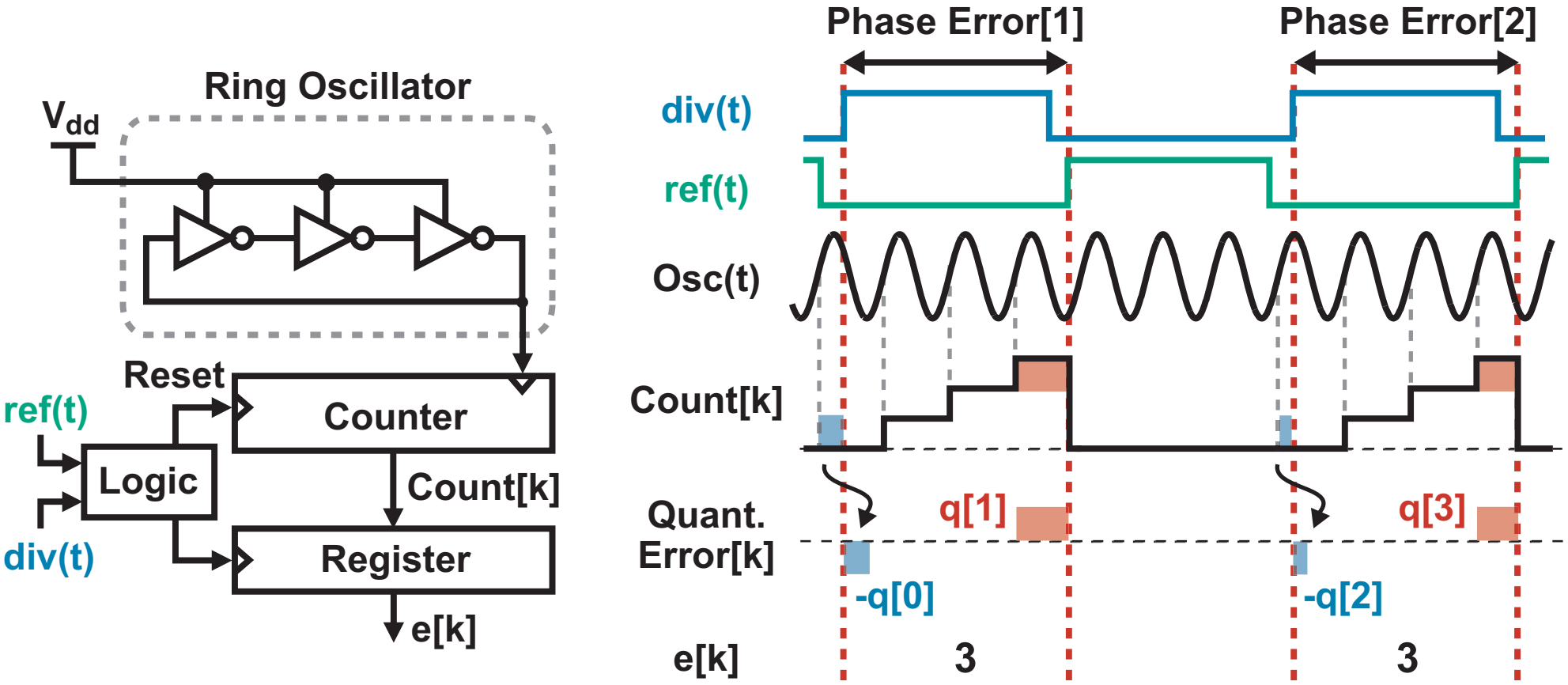
An Oscillator-Based TDC





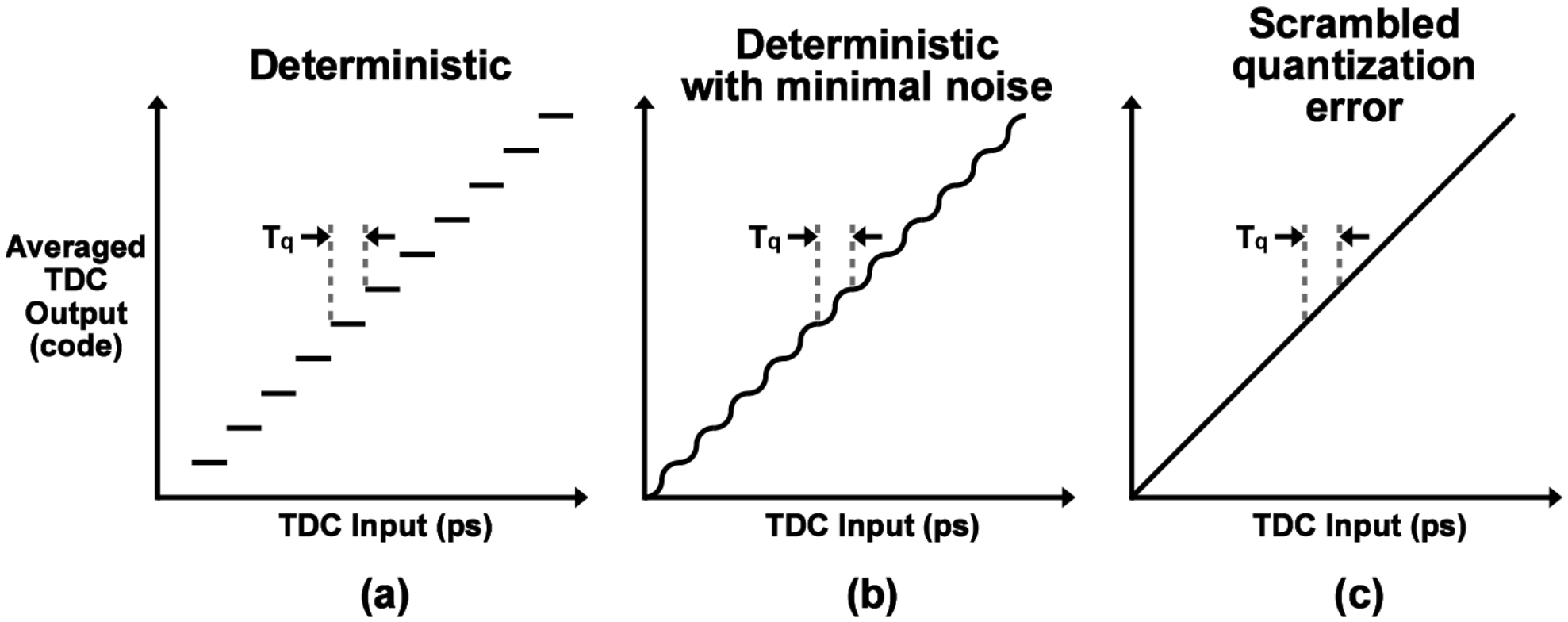
- Output *e[k]* corresponds to the number of oscillator edges that occur during the measurement time window
- Advantages
  - Extremely large range can be achieved with compact area
  - Quantization noise is scrambled across measurements

A Closer Look at Quantization Noise Scrambling



- Quantization error occurs at beginning and end of each measurement interval
- As a rough approximation, assume error is uncorrelated between measurements
  - Averaging of measurements improves effective resolution

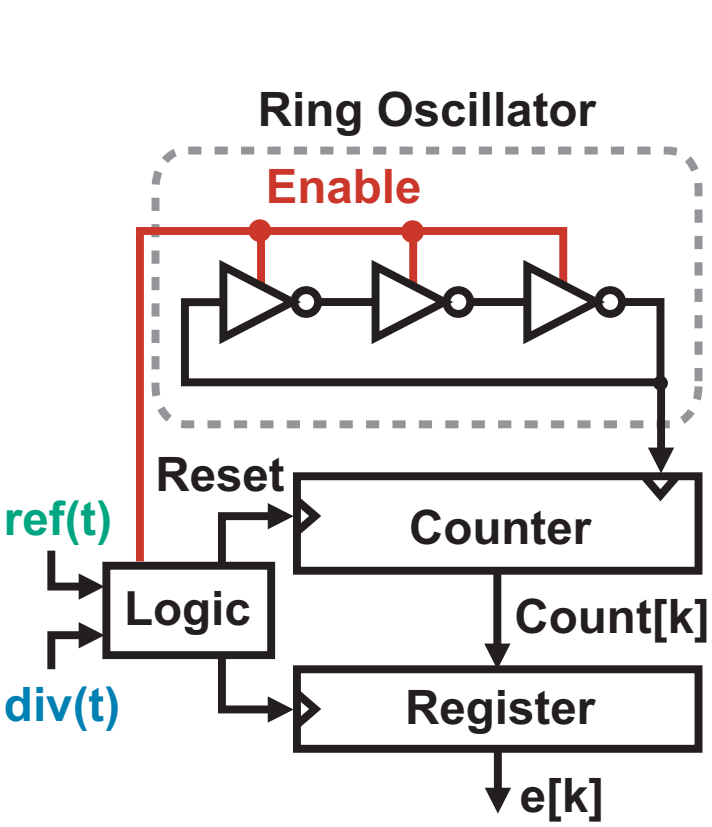
Deterministic quantizer error vs. scrambled error

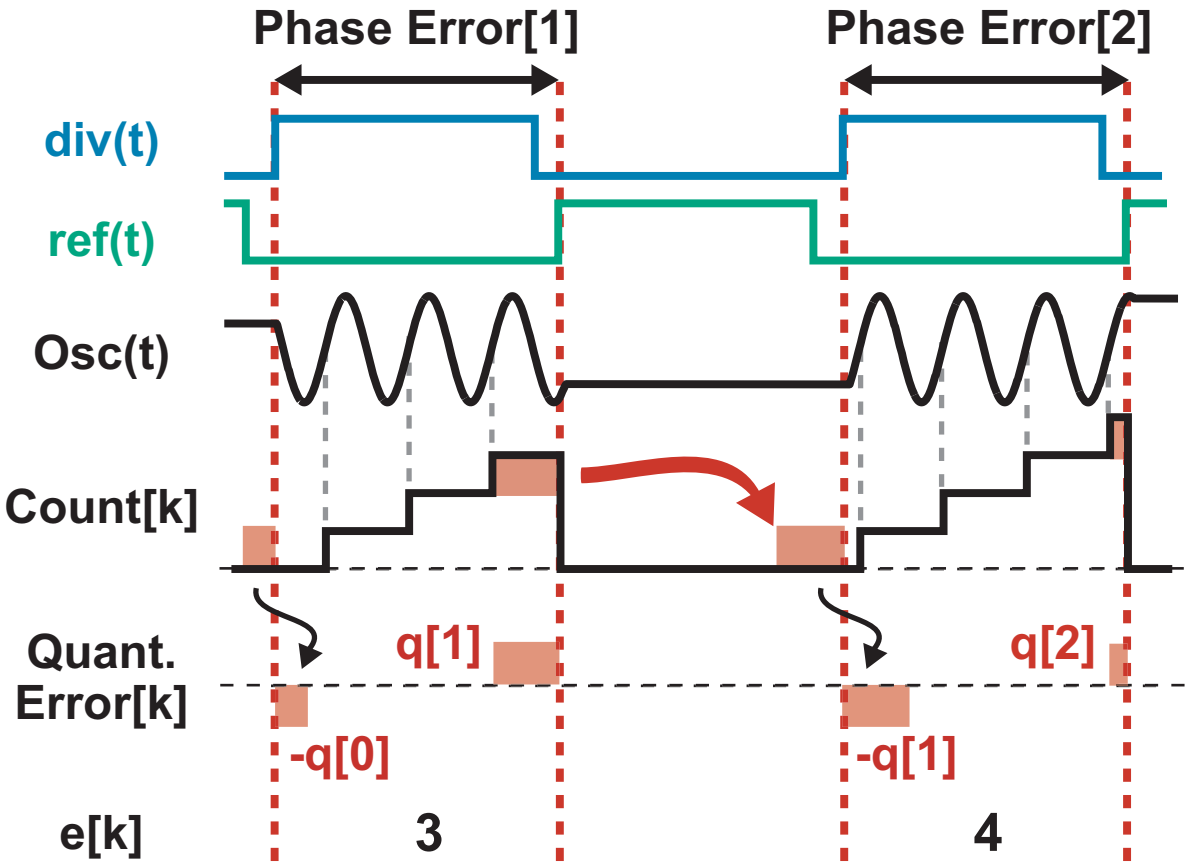


- Deterministic TDC do not provide inherent scrambling
- For oversampling benefit, TDC error must be scrambled!
- Some systems provide input scrambling ($\Delta\Sigma$ fractional-N PLL), while some others do not (integer-N PLL)

Proposed GRO TDC Structure

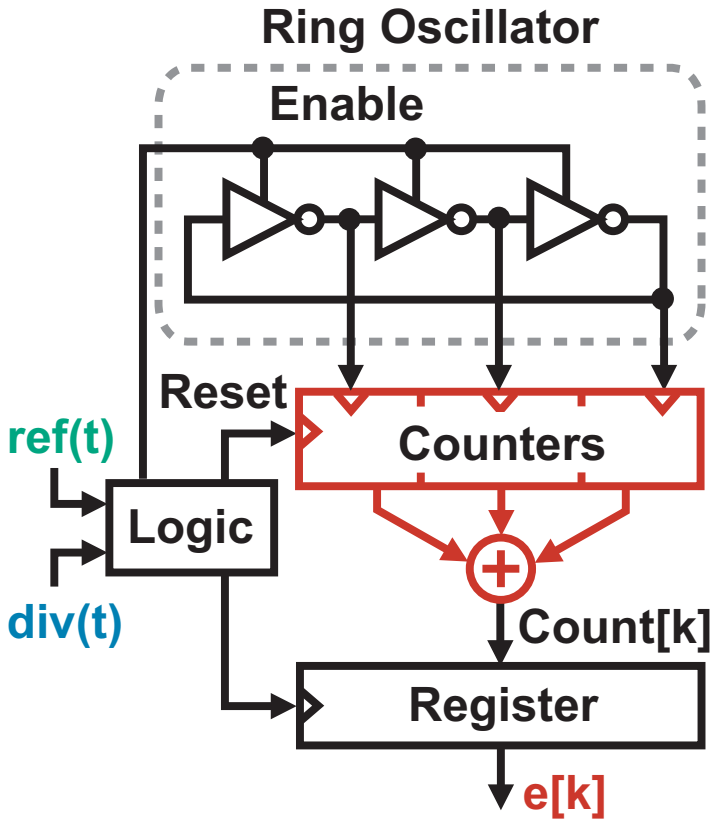
A Gated Ring Oscillator (GRO) TDC



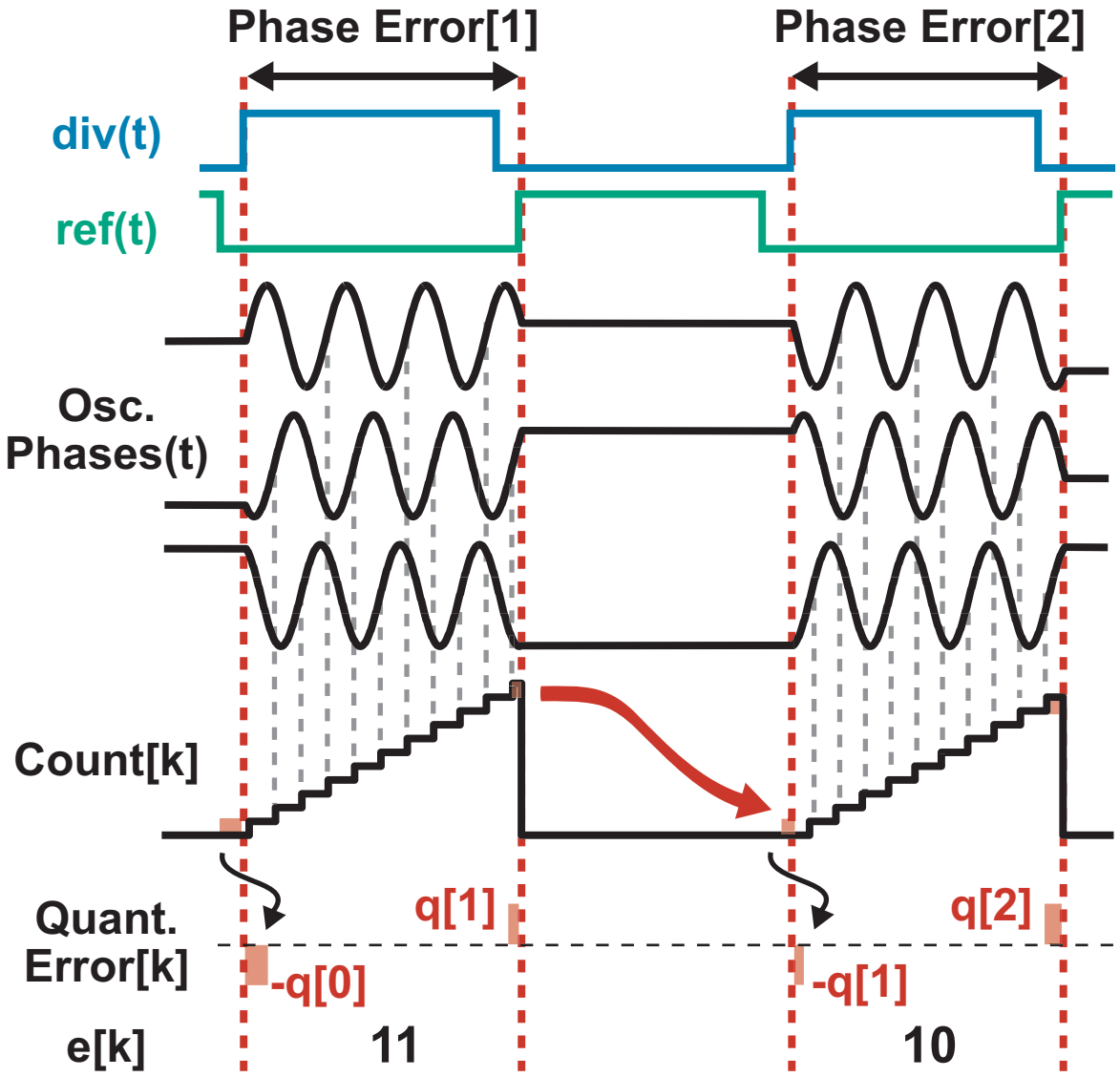


- Enable ring oscillator only during measurement intervals
  - Hold the state of the oscillator between measurements
- Quantization error becomes first order noise shaped!
  - *e[k] = Phase Error[k] + q[k] – q[k-1]*
  - Averaging dramatically improves resolution!

Improve Resolution By Using All Oscillator Phases

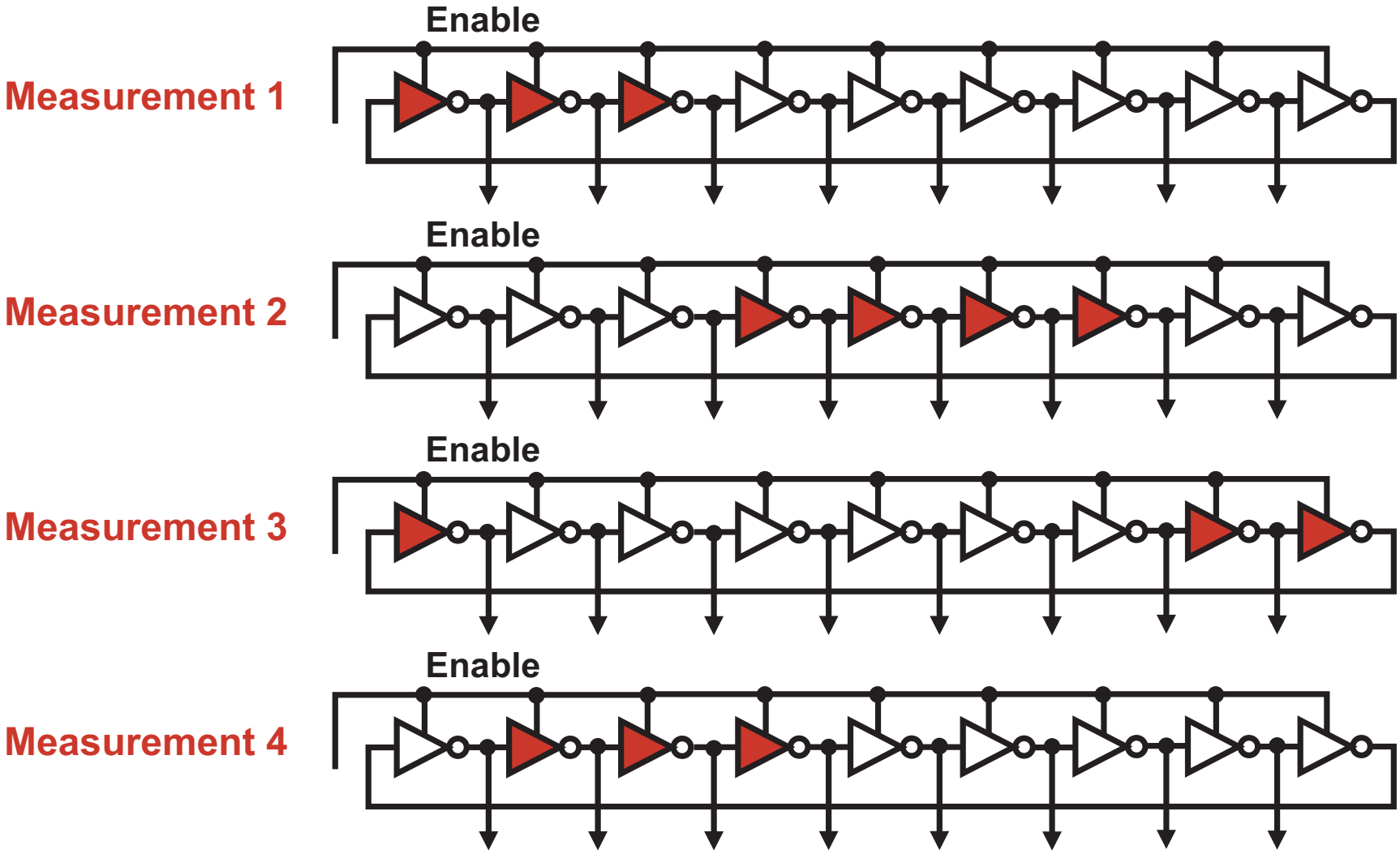


Helal, Straayer, Wei,
Perrott VLSI 2007



- Raw resolution is set by inverter delay
- Effective resolution is dramatically improved by averaging

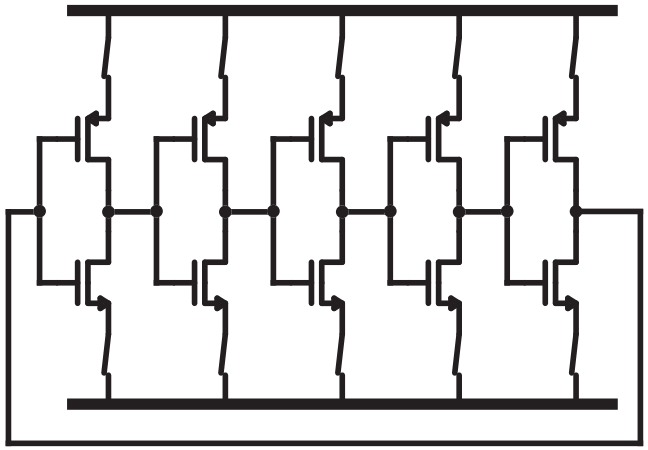
GRO TDC Also Shapes Delay Mismatch



- Barrel shifting occurs through delay elements across different measurements
  - Mismatch between delay elements is first order shaped!

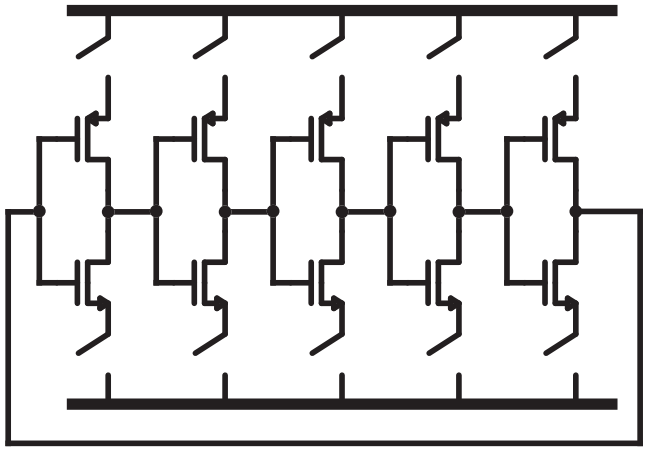
Simple gated ring oscillator inverter-based core

Enabled Ring Oscillator



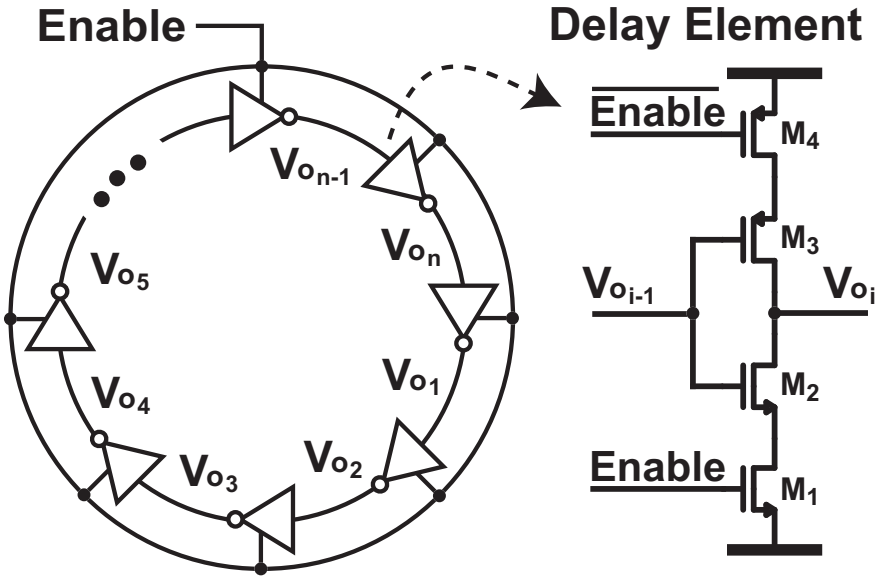
(a)

Disabled Ring Oscillator

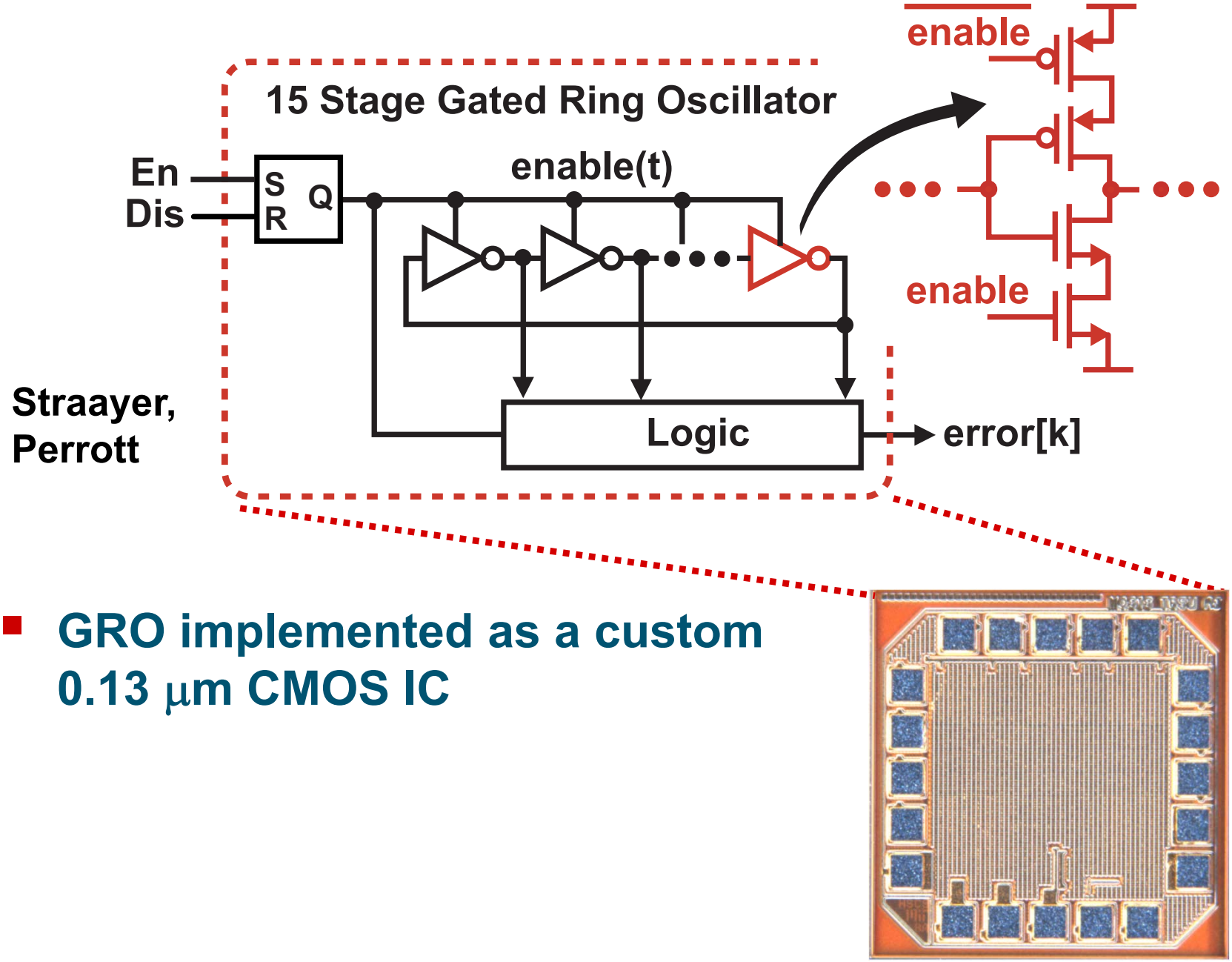


(b)

Gate the oscillator by switching the inverter cores to the power supply

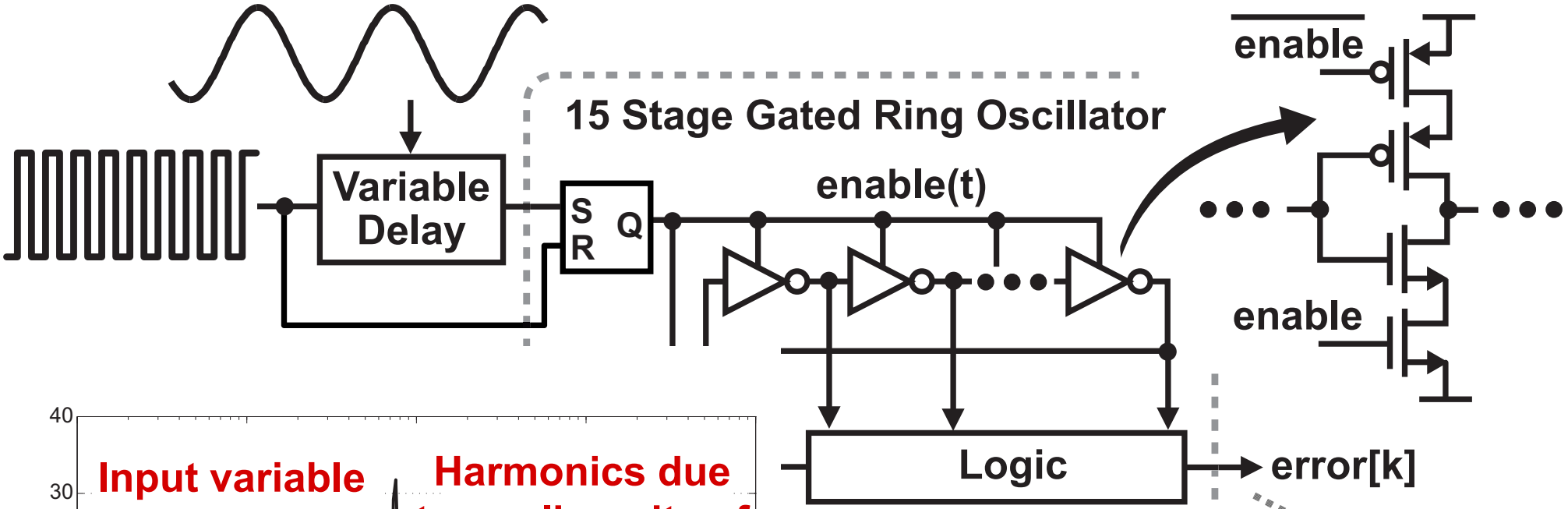


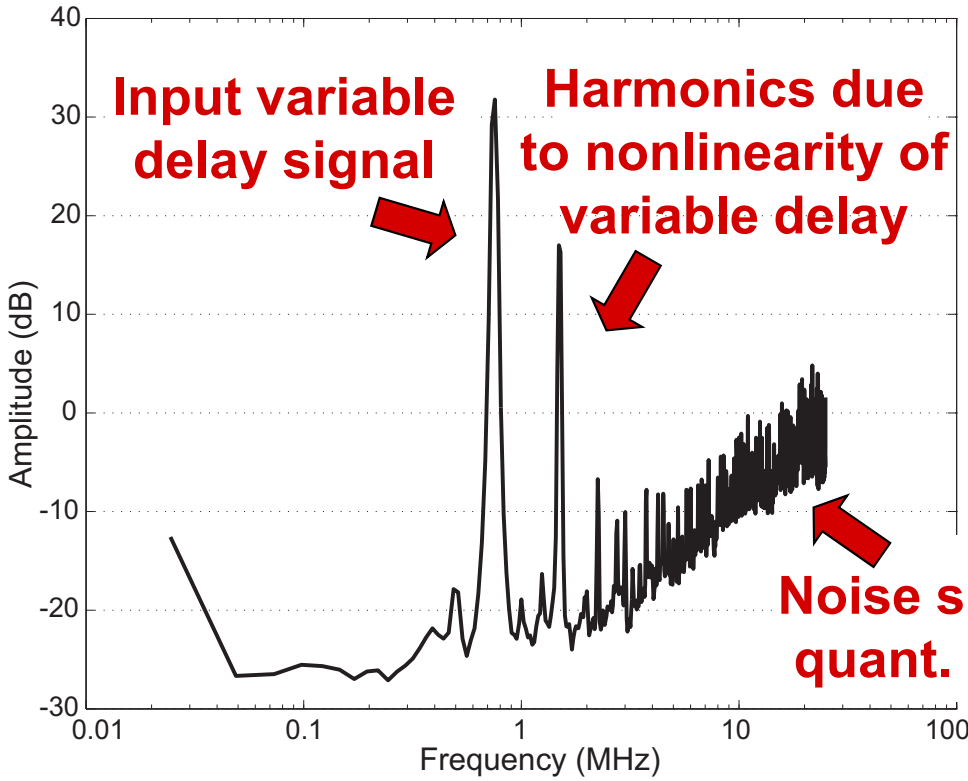
GRO Prototype

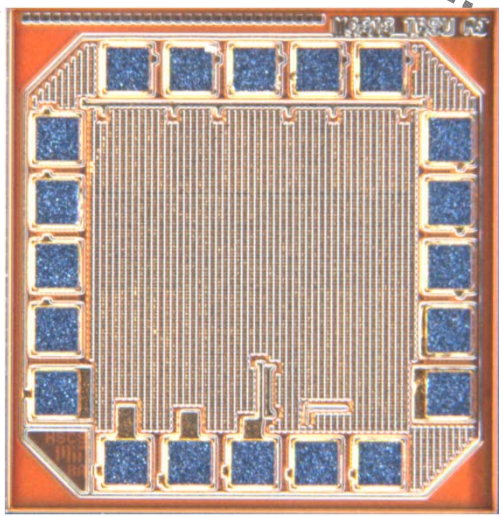


- GRO implemented as a custom 0.13 μm CMOS IC

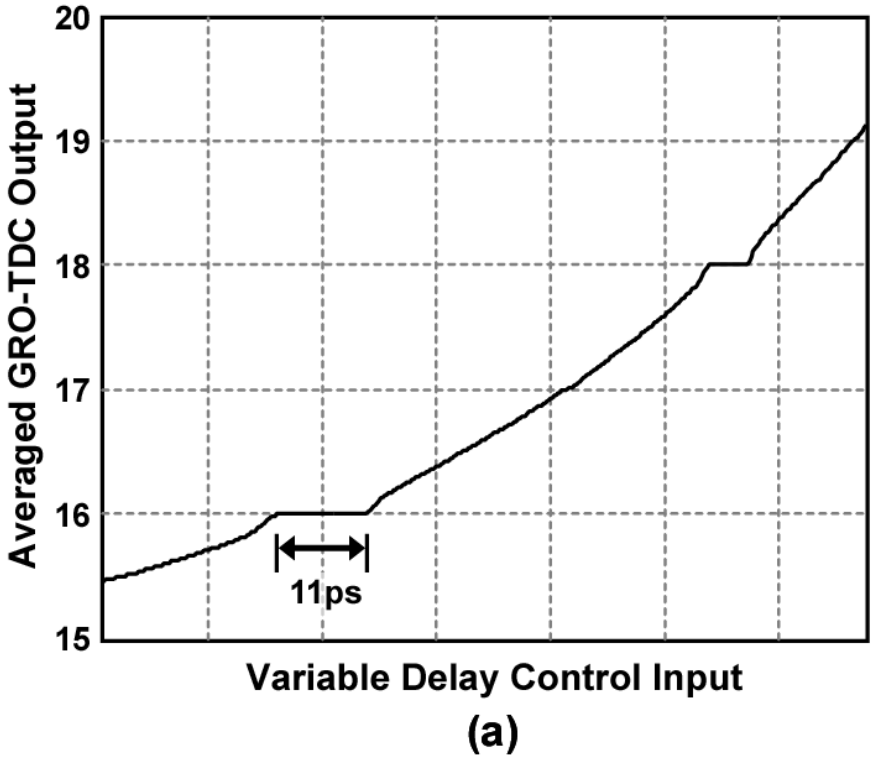
Measured GRO Results Confirm Noise Shaping

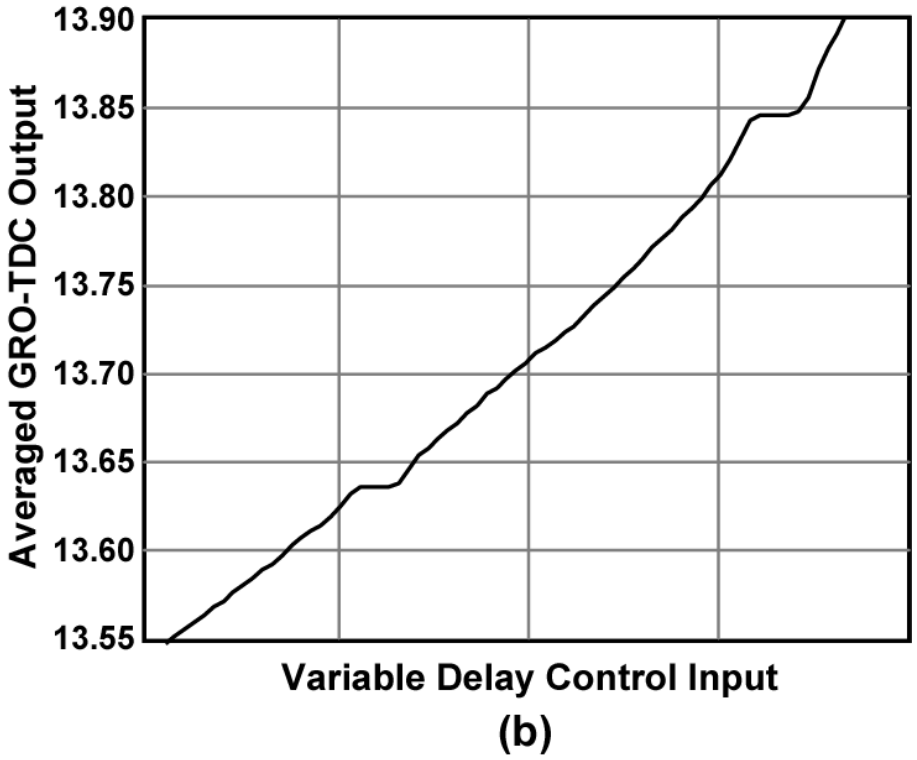






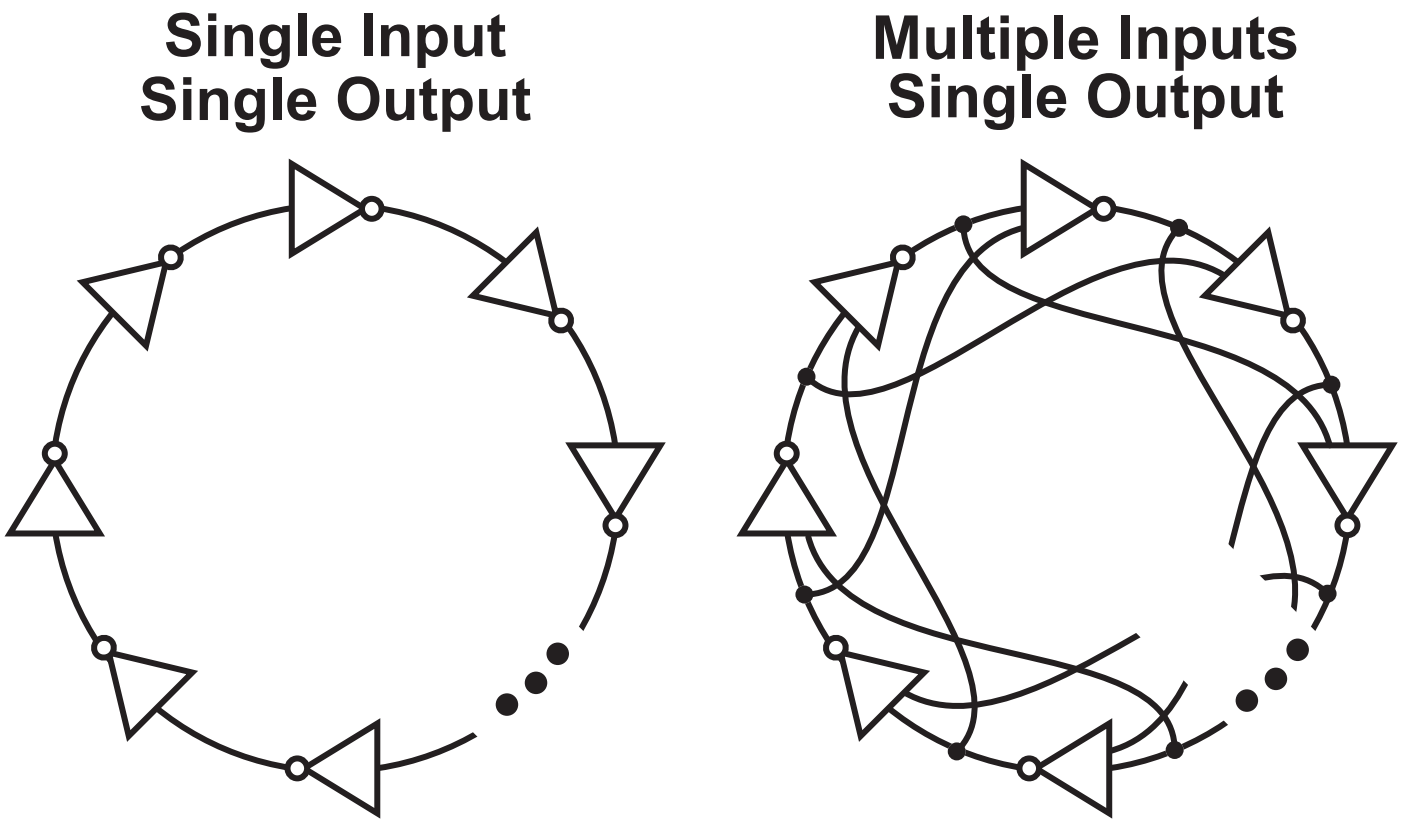
Measured deadzone behavior of inverter-based GRO





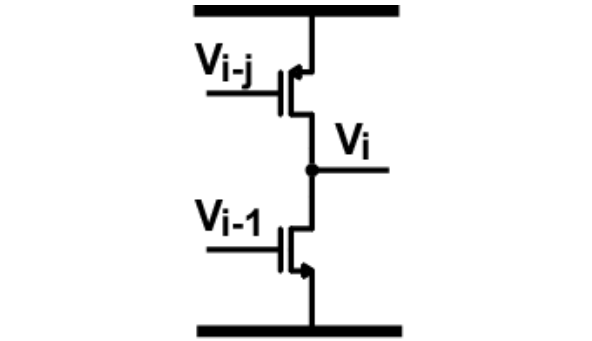
- Deadzones were caused by errors in gating the oscillator
- GRO "injection locked" to an integer ratio of F_S
- Behavior occurred for almost all integer boundaries, and some fractional values as well
- Noise shaping benefit was limited by this gating error

Next Generation GRO: Multi-path oscillator concept



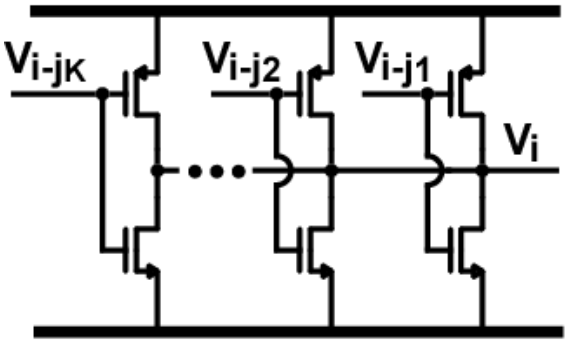
- Use multiple inputs for each delay element instead of one
- Allow each stage to optimally begin its transition based on information from the entire GRO phase state
- Key design issue is to ensure primary mode of oscillation

Multi-path inverter core



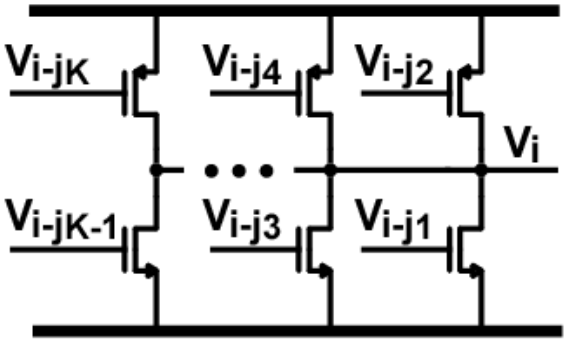
(a) Asymmetrically skewed inverter

Lee, Kim, Lee
JSSC 1997

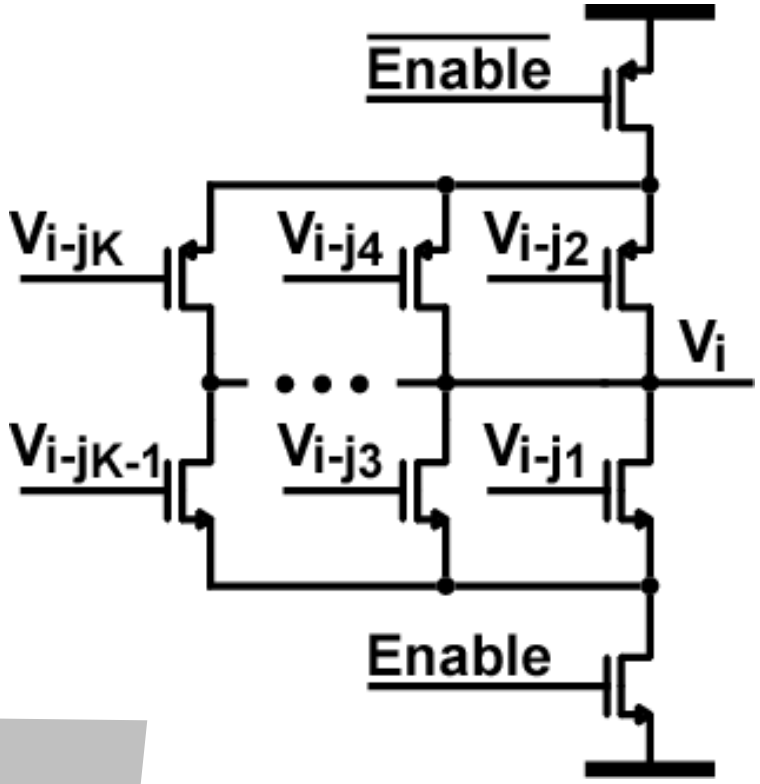


(b) Multiple skewed inverters

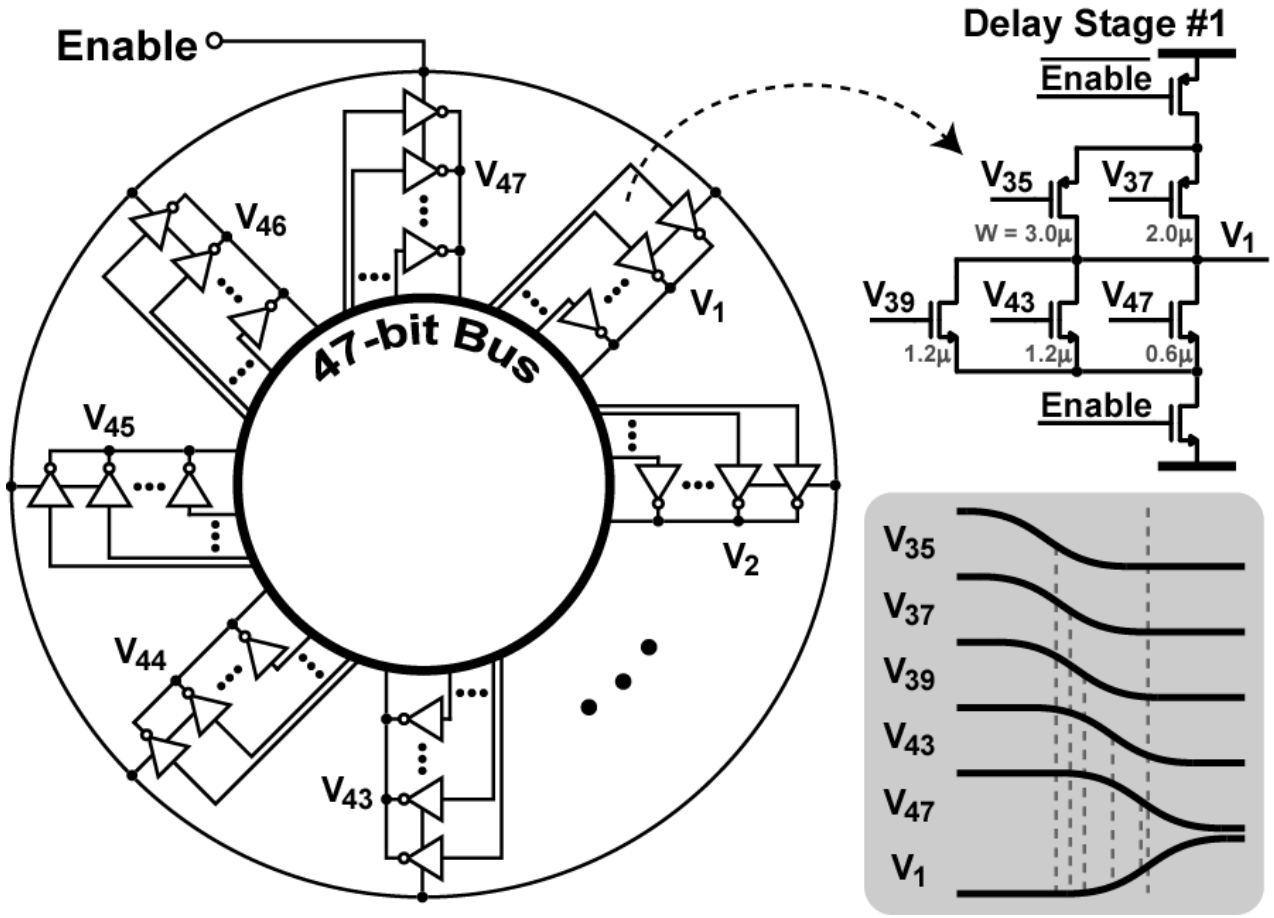
Mohan, et. al.,
CICC 2005



(c) Unrestricted connections



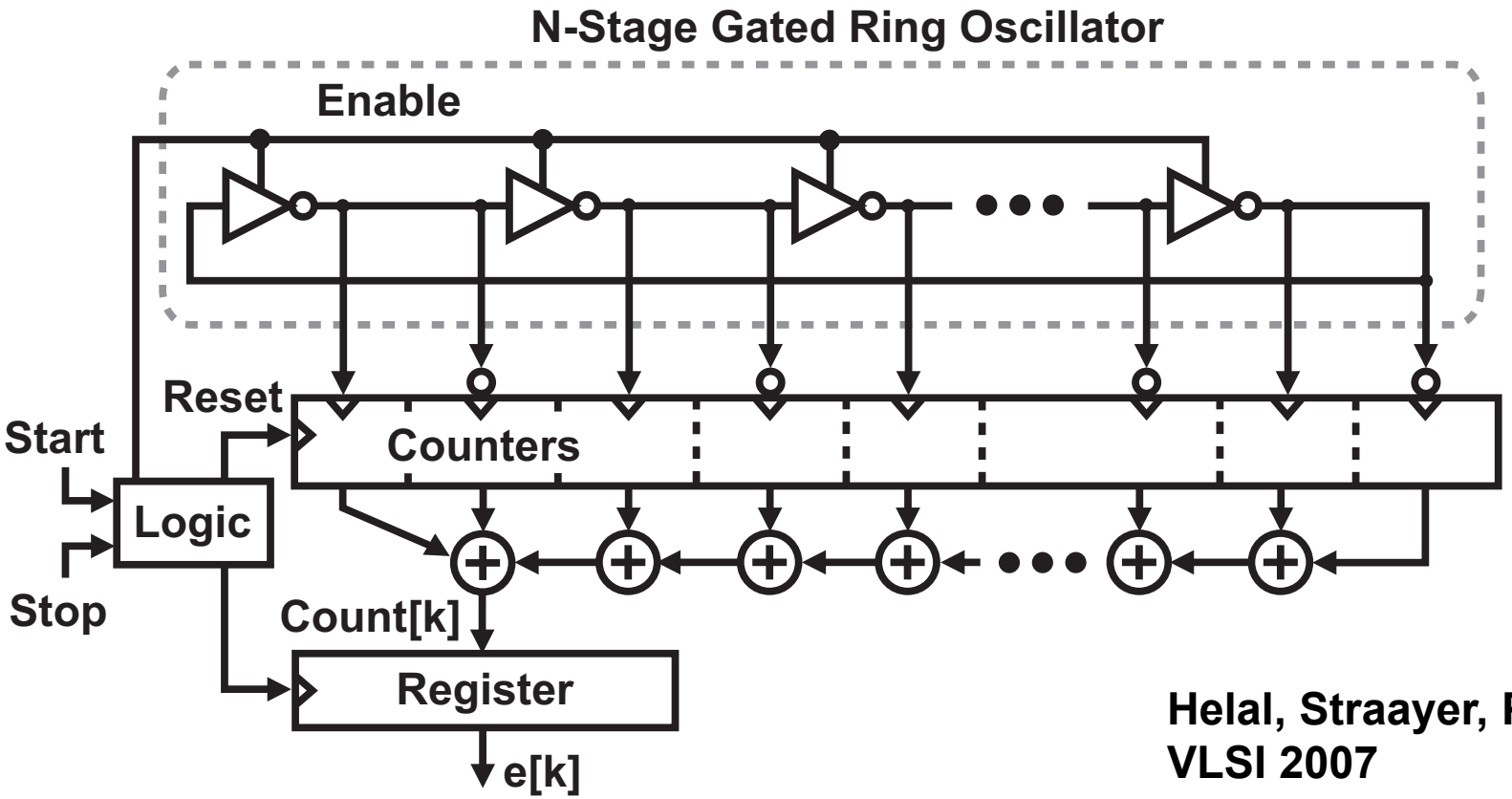
Proposed multi-path gated ring oscillator



Hsu, Straayer, Perrott
ISSCC 2008

- Oscillation frequency near 2GHz with 47 stages…
- Reduces effective delay per stage by a factor of 5-6!
- Represents a factor of 2-3 improvement compared to previous multi-path oscillators

A simple measurement approach…

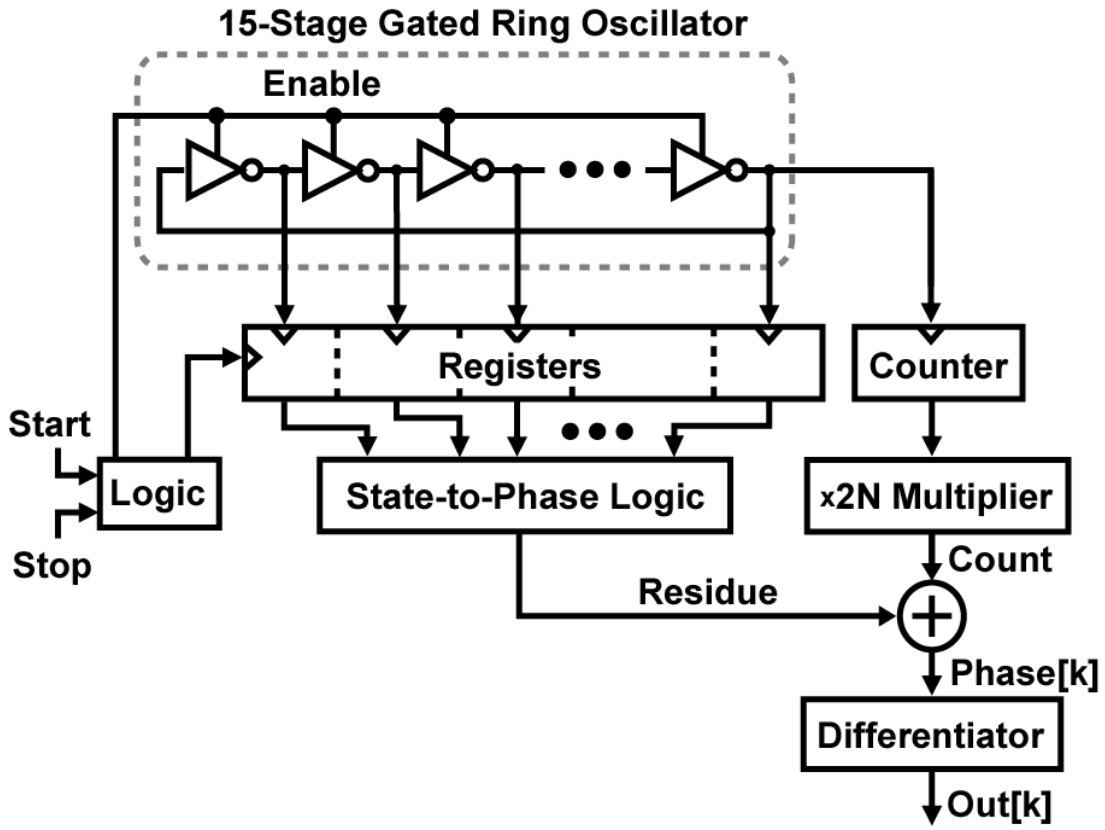


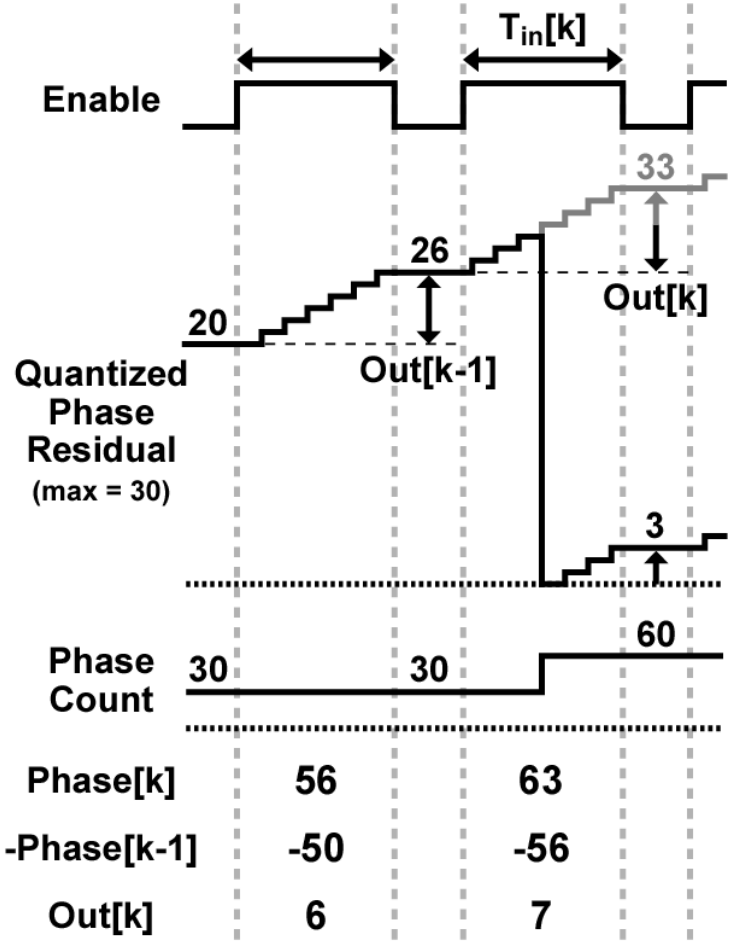
Helal, Straayer, Perrott
VLSI 2007

- 2 counters per stage * 47 stages = 94 counters each at 2GHz
- Power consumption for these counters is unreasonable

Need a more efficient way to measure the multi-path GRO

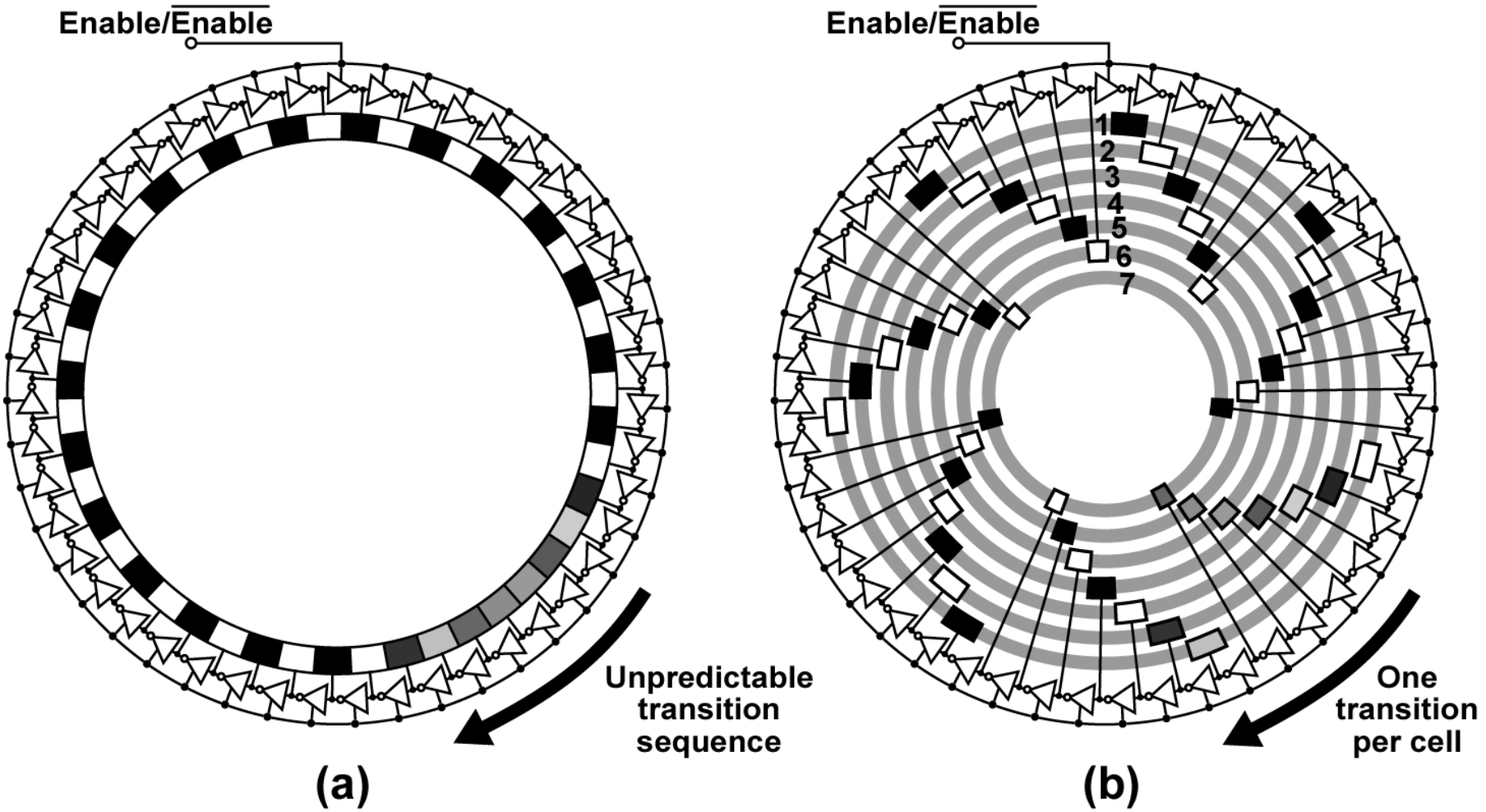
Count Edges by Sampling Phase





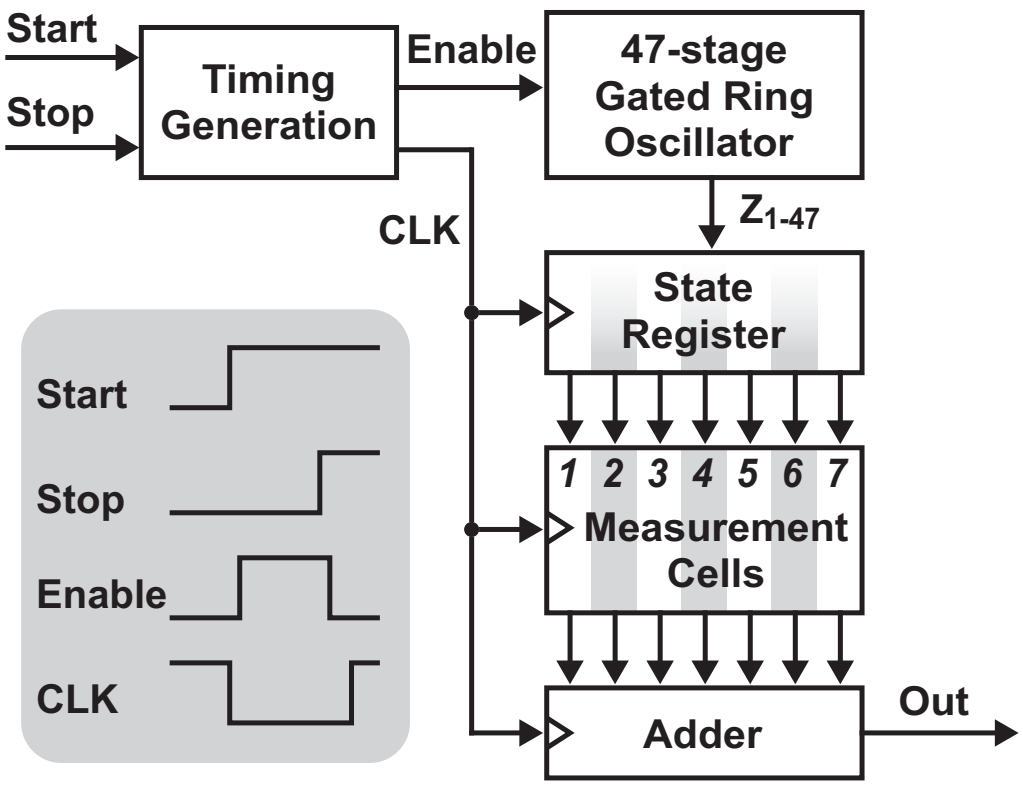
- Calculate phase from:
  - A single counter for coarse phase information (keeps track of phase wrapping)
  - GRO phase state for fine count information
- 1 counter and N registers → much more efficient

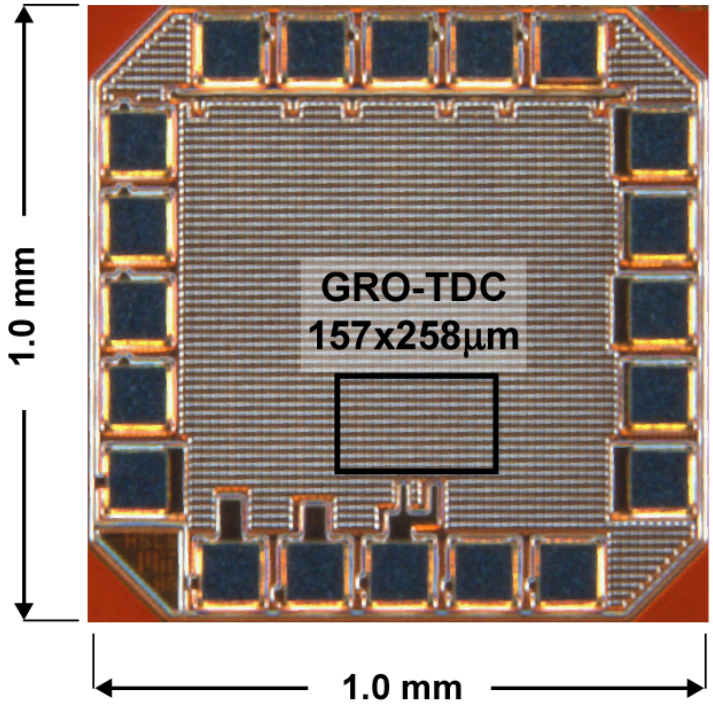
Proposed Multi-Path Measurement Structure



- Multi-path structure leads to ambiguity in edge position
- Partition into 7 cells to avoid such ambiguity
  - Requires 7 counters rather than 1, but power still OK

Prototype 0.13μm CMOS multi-path GRO-TDC

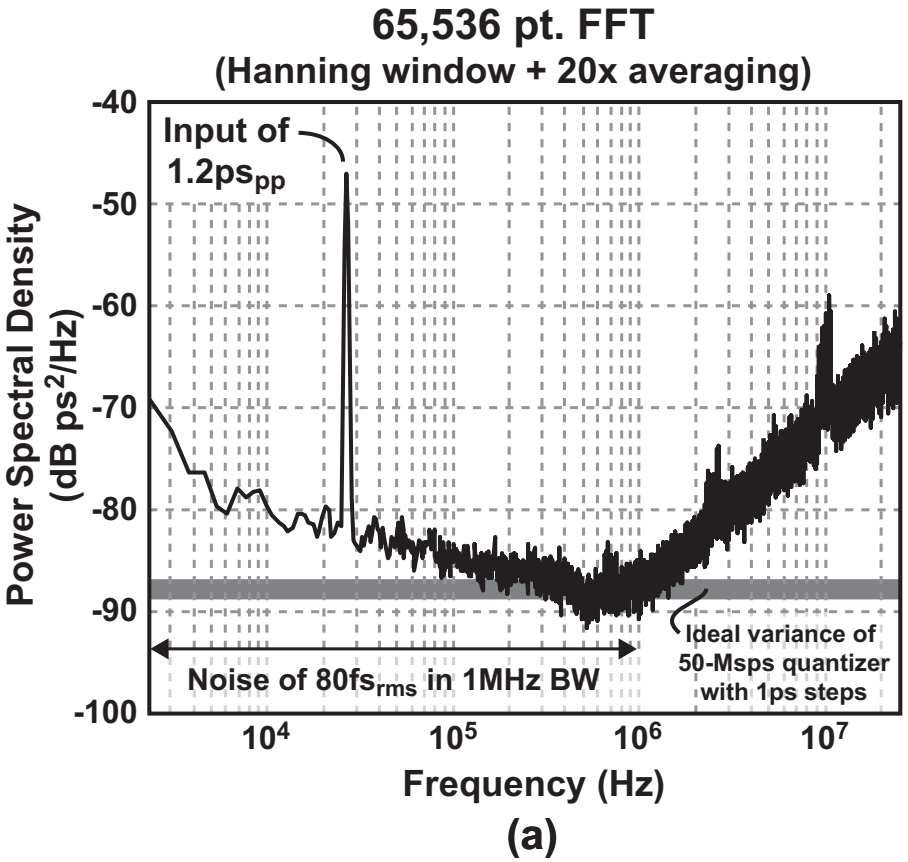


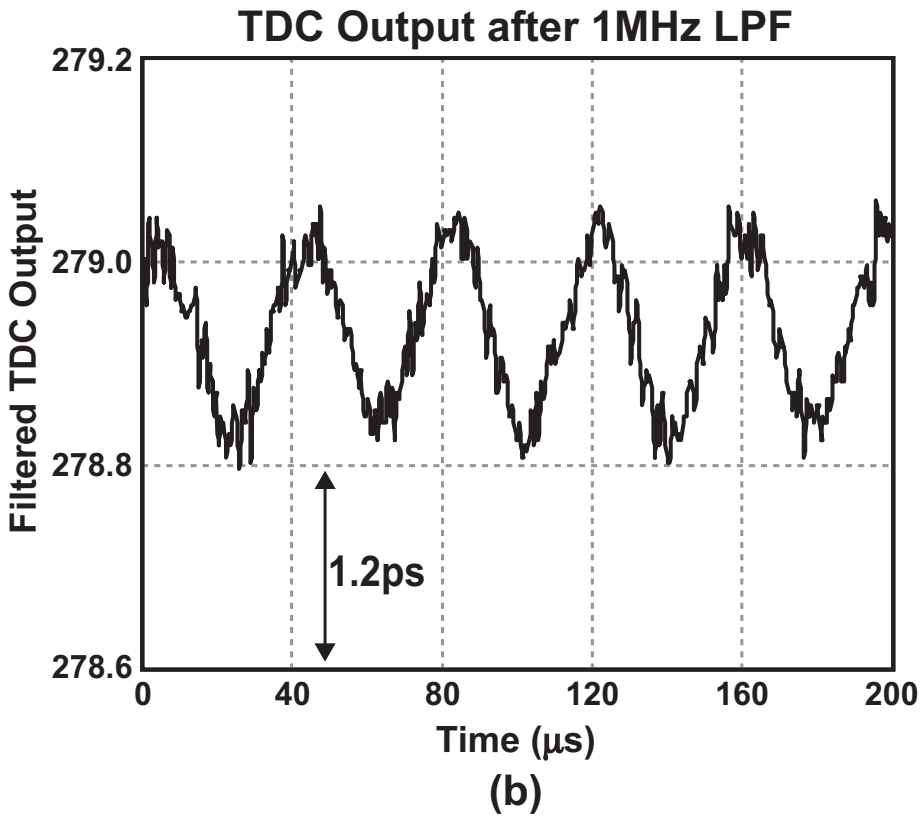


Straayer et al., VLSI 2008

- **Two implemented versions:**
  - **8-bit, 500Msps**
  - **11-bit, 100Msps version**
- **2-21mW power consumption depending on input duty cycle**

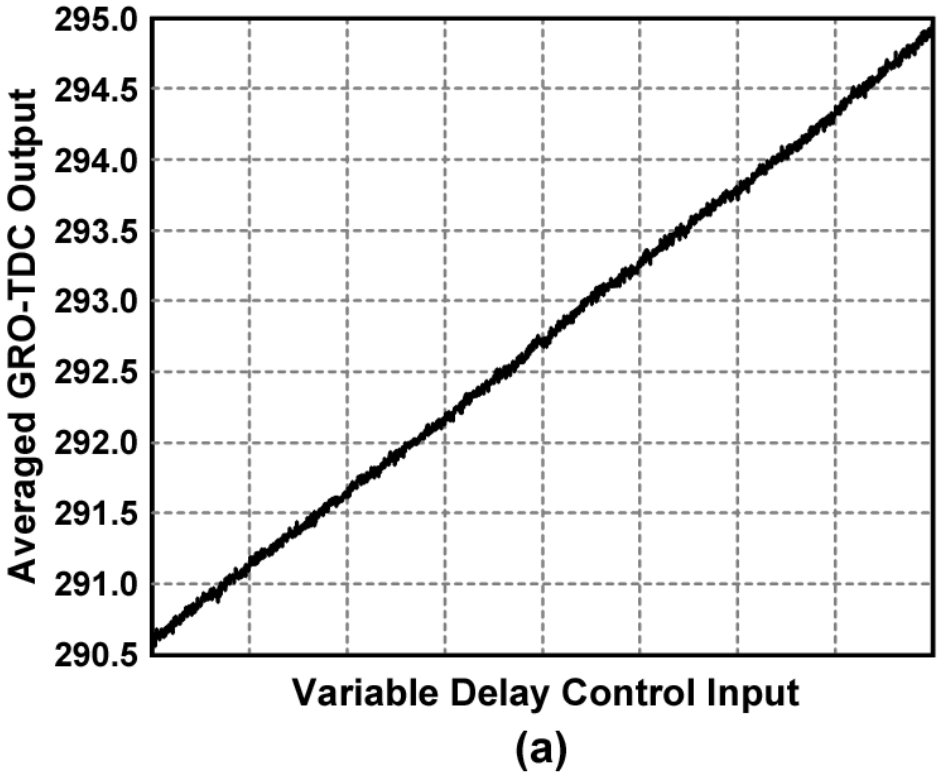
Measured noise-shaping of multi-path GRO

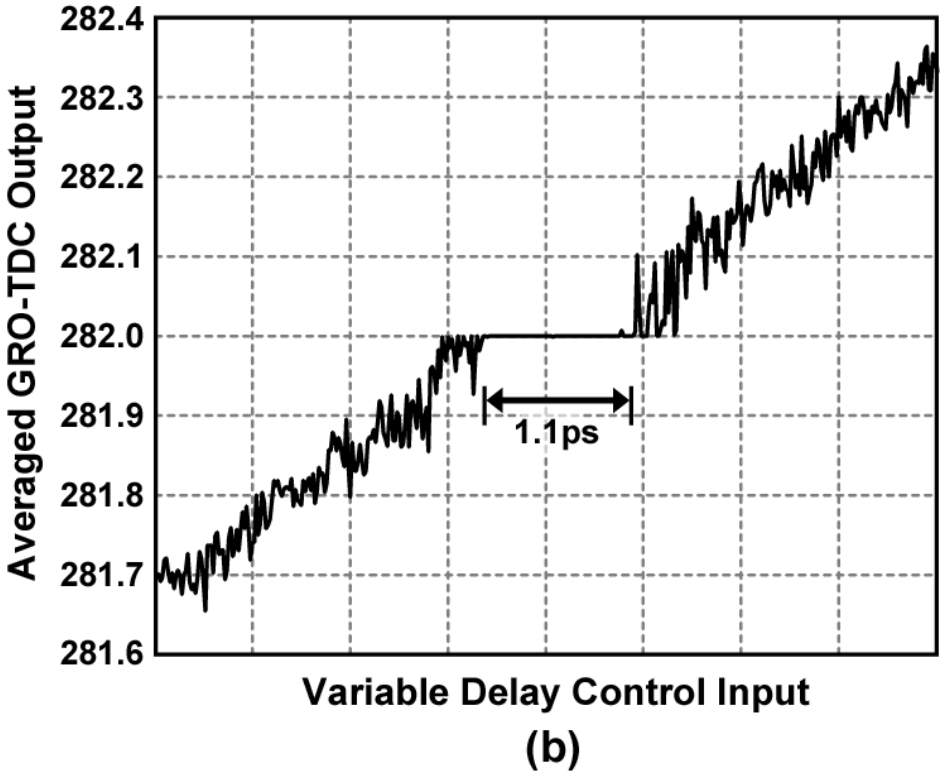




- Data collected at 50Msps
- More than 20dB of noise-shaping benefit
- 80fs$_{rms}$ integrated error from 2kHz-1MHz
- Floor primarily limited by 1/f noise (up to 0.5-1MHz)

Measured deadzone behavior for multi-path GRO

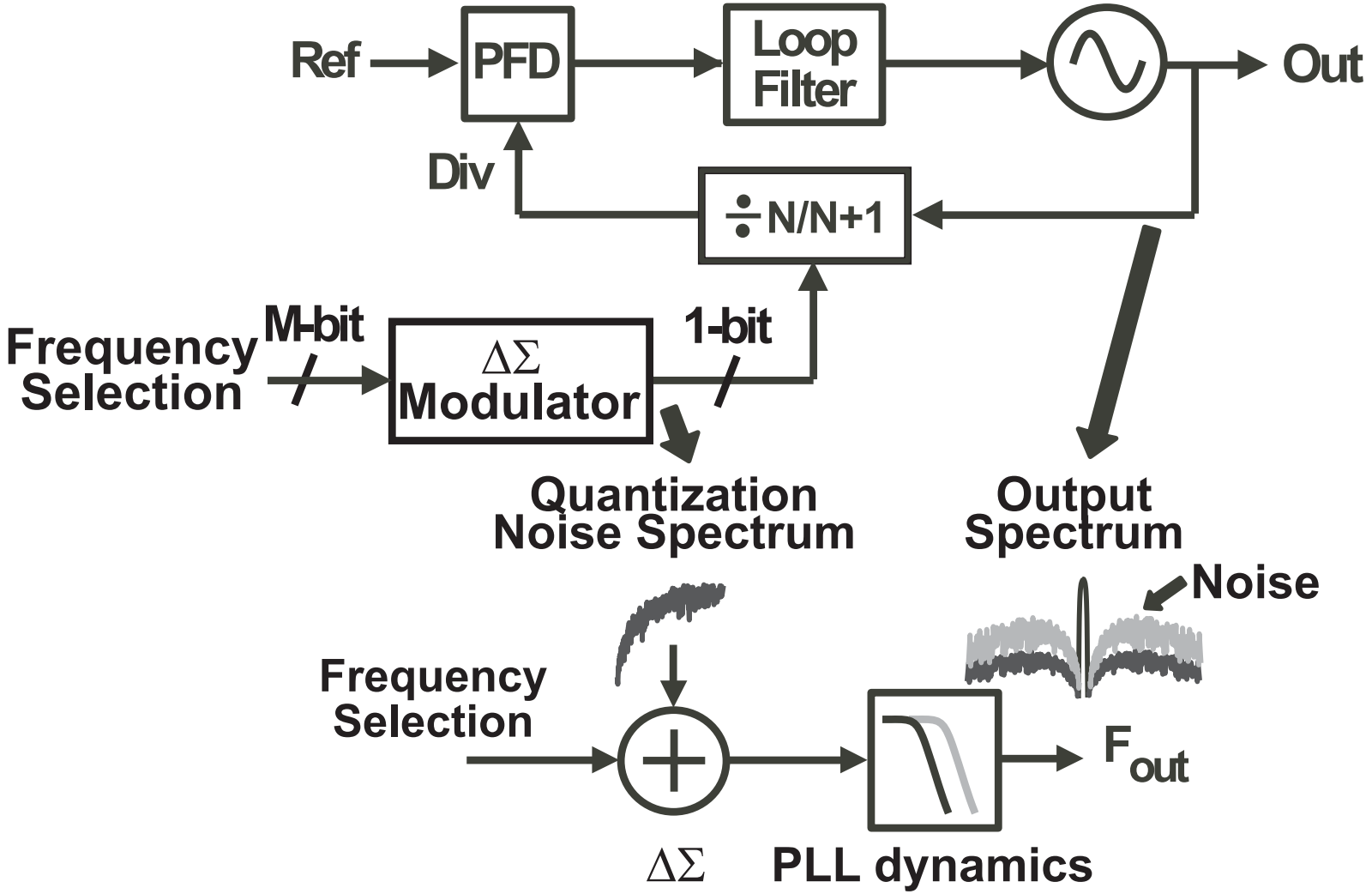




- Only deadzones for outputs that are multiples of 2N
  - 94, 188, 282, etc.
  - No deadzones for other even or odd integers, fractional output
- Size of deadzone is reduced by 10x

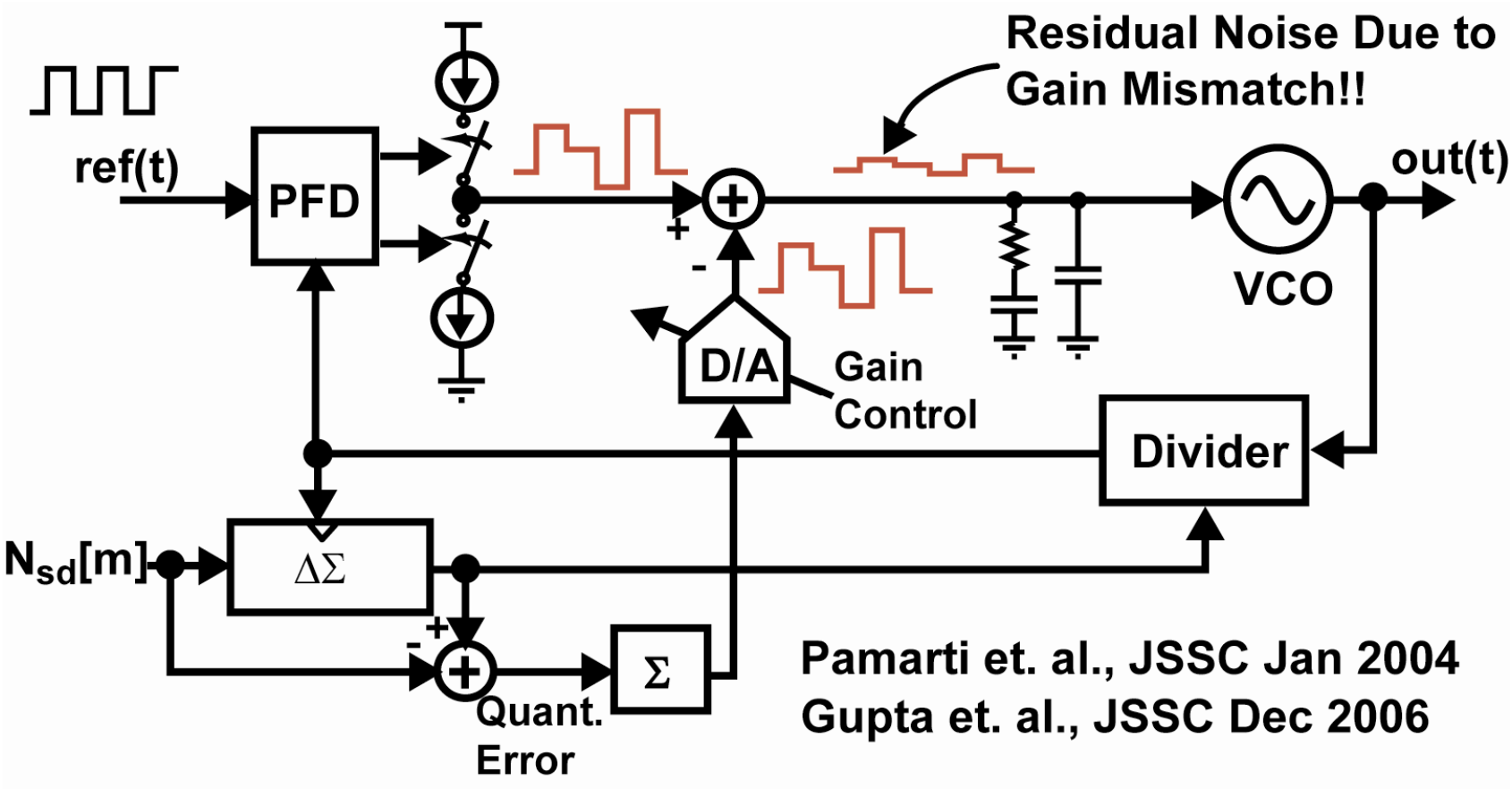
The Issue of Quantization Noise Due to Divider Dithering

The Nature of the Quantization Noise Problem



- Increasing PLL bandwidth increases impact of ΔΣ fractional-N noise
  - Cancellation offers a way out!

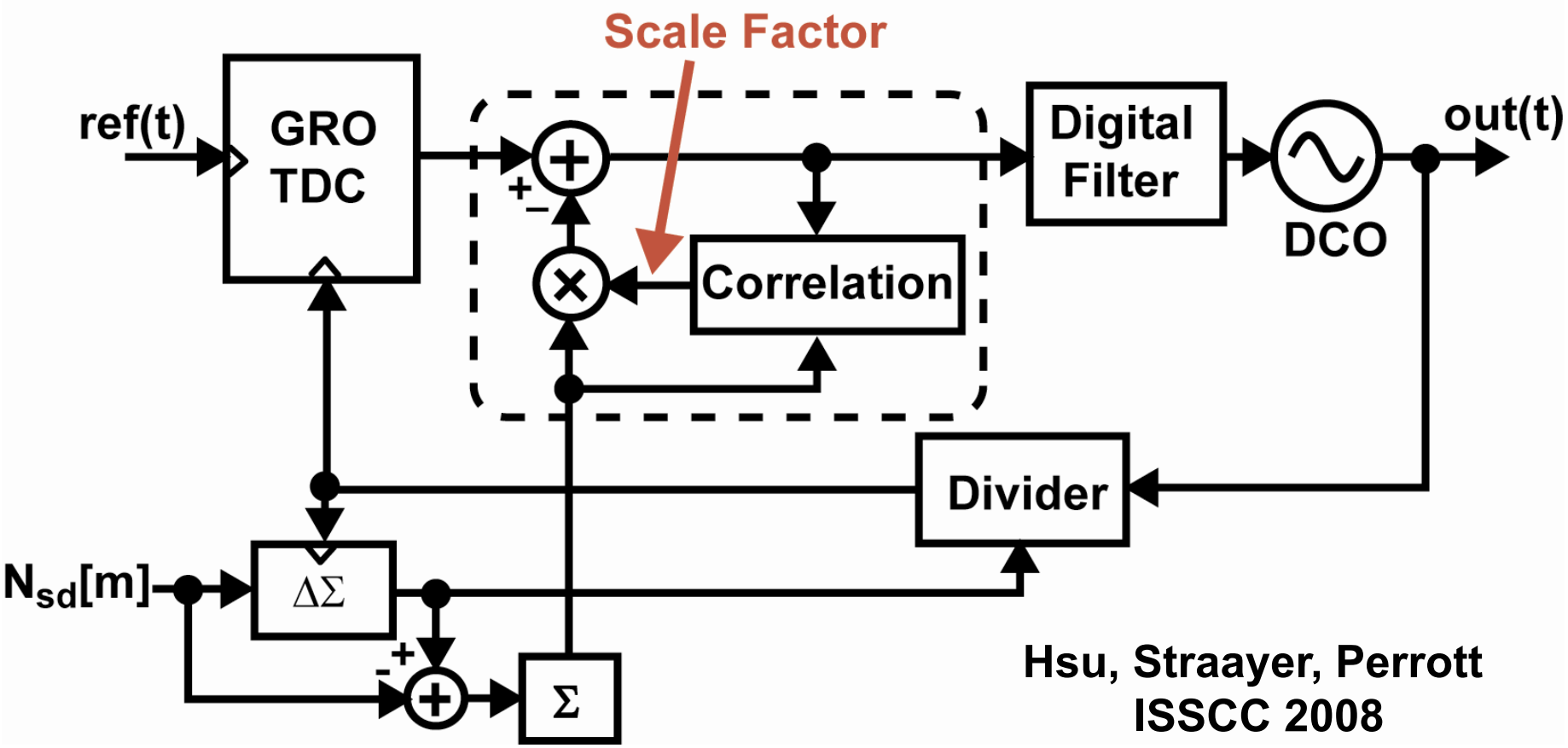
Previous Analog Quantization Noise Cancellation



- Phase error due to ΔΣ is predicted by accumulating ΔΣ quantization error
- Gain matching between PFD and D/A must be precise

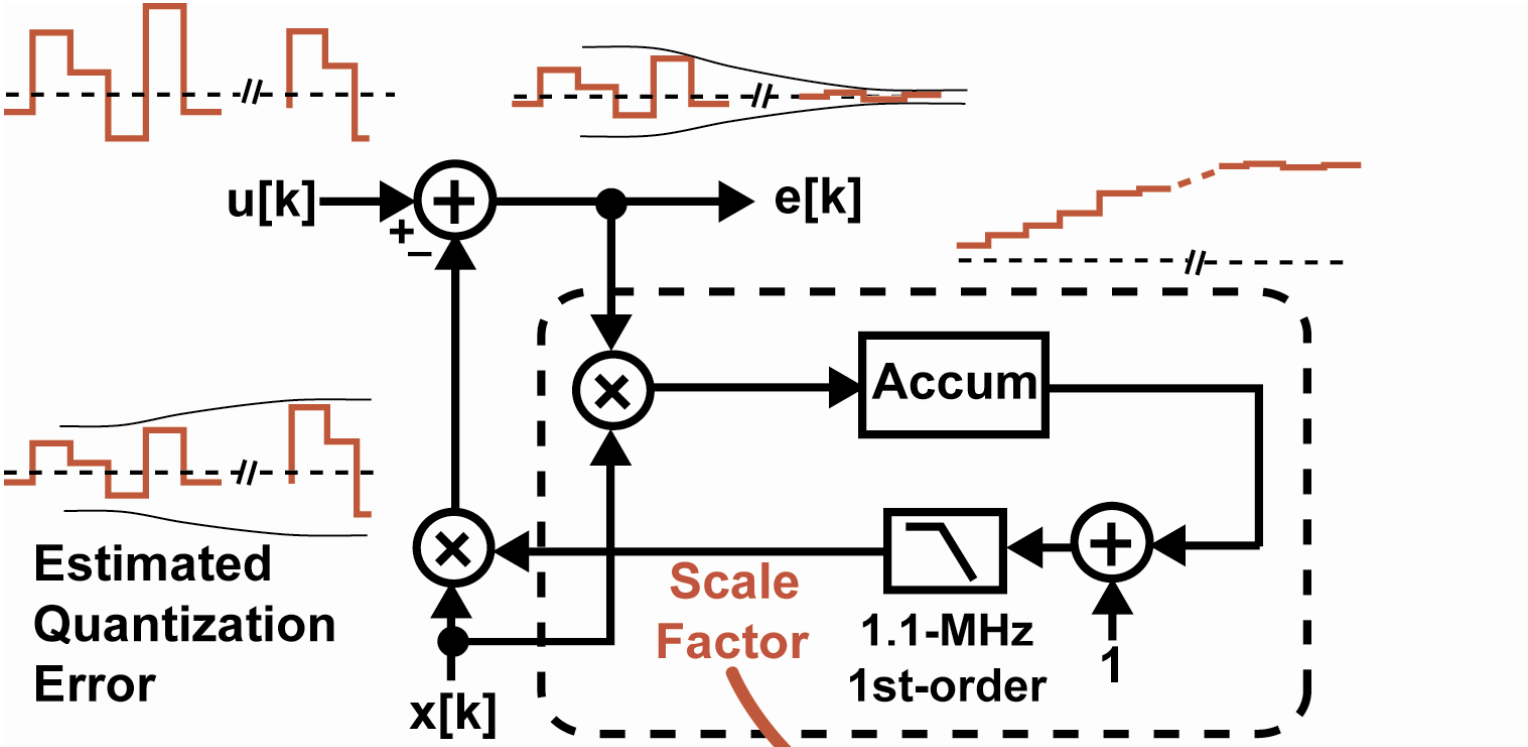
Matching in analog domain limits performance

Proposed All-digital Quantization Noise Cancellation

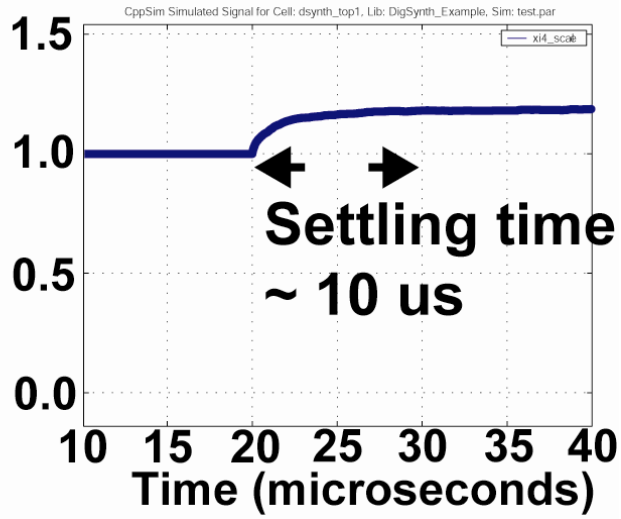


- Scale factor determined by simple digital correlation
- Analog non-idealities such as DC offset are completely eliminated

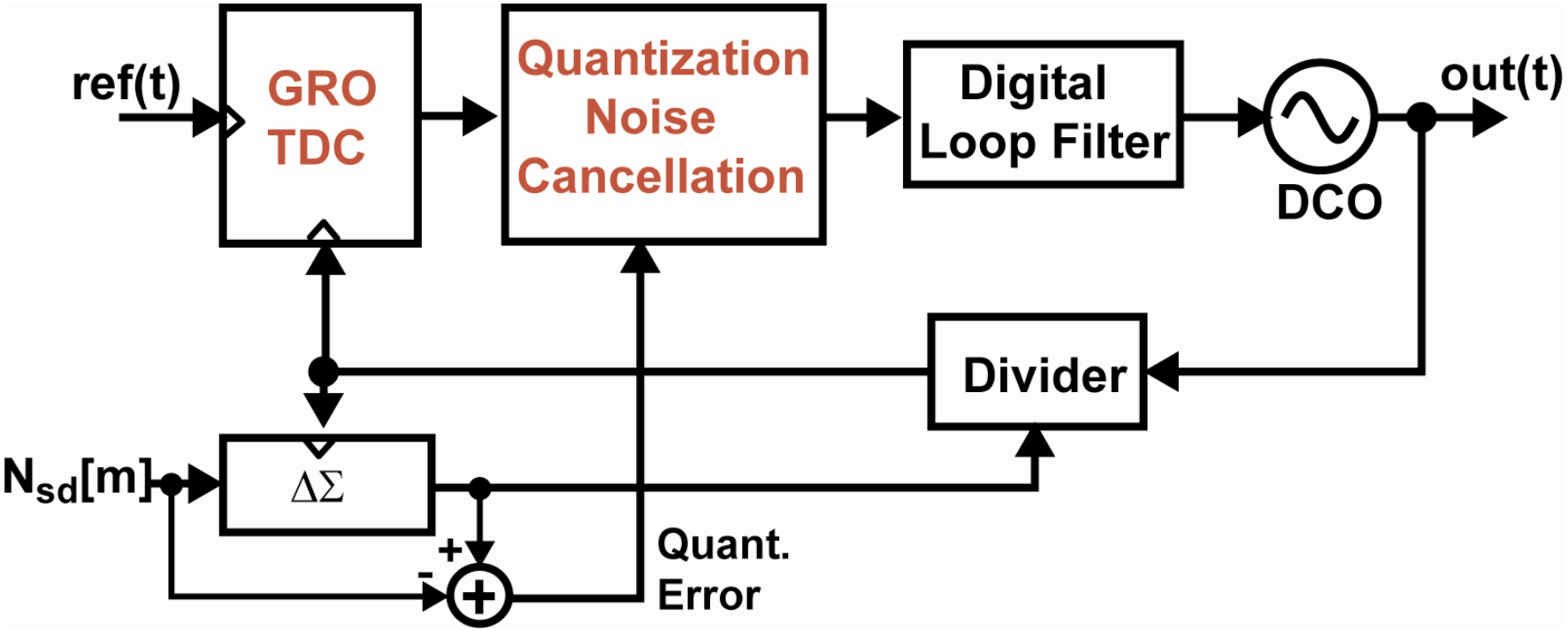
Details of Proposed Quantization Noise Cancellation



- Correlator out is accumulated and filtered to achieve scale factor
  - Settling time chosen to be around 10 us
- See *analog* version of this technique in *Swaminathan et.al., ISSCC 2007*

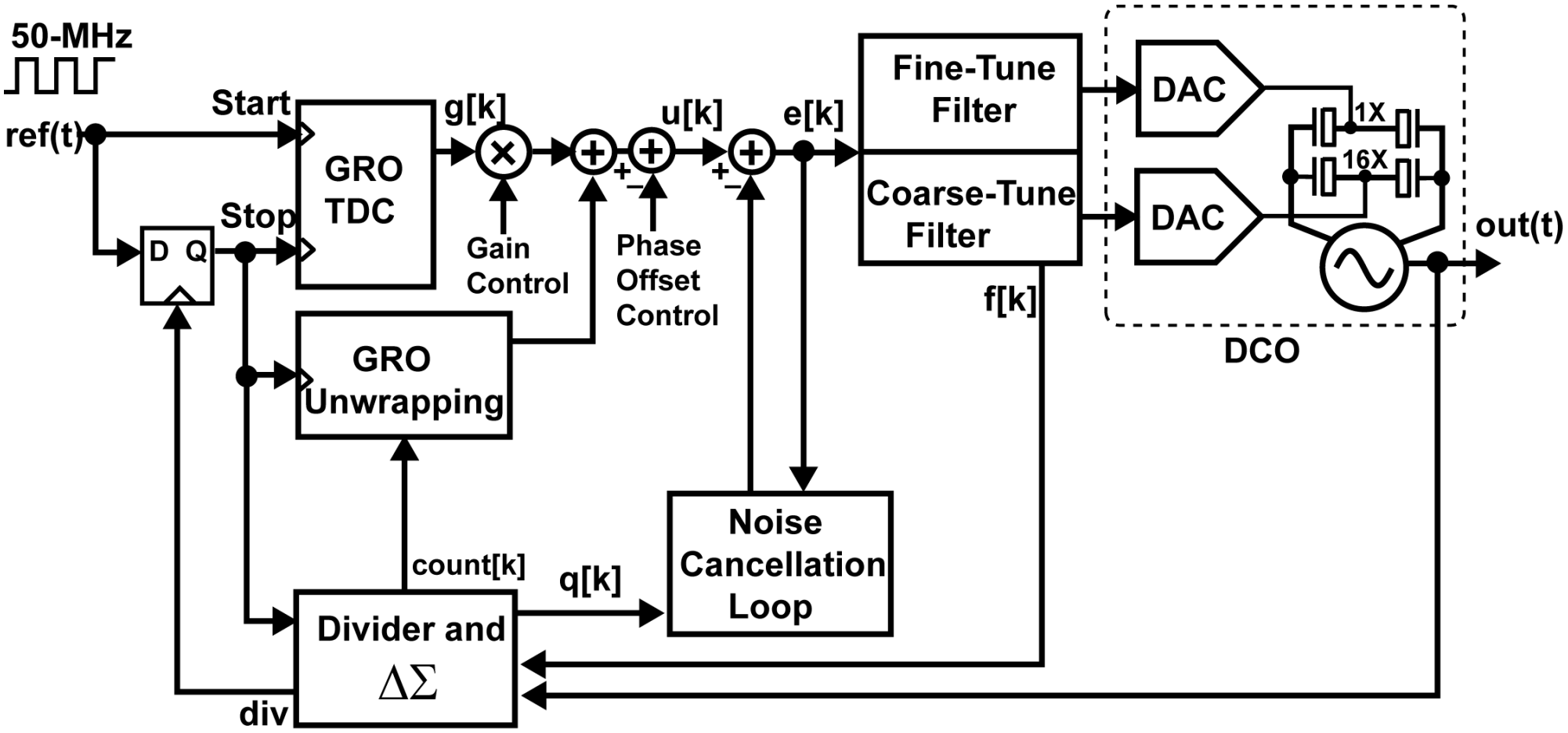


Proposed Digital Wide BW Synthesizer



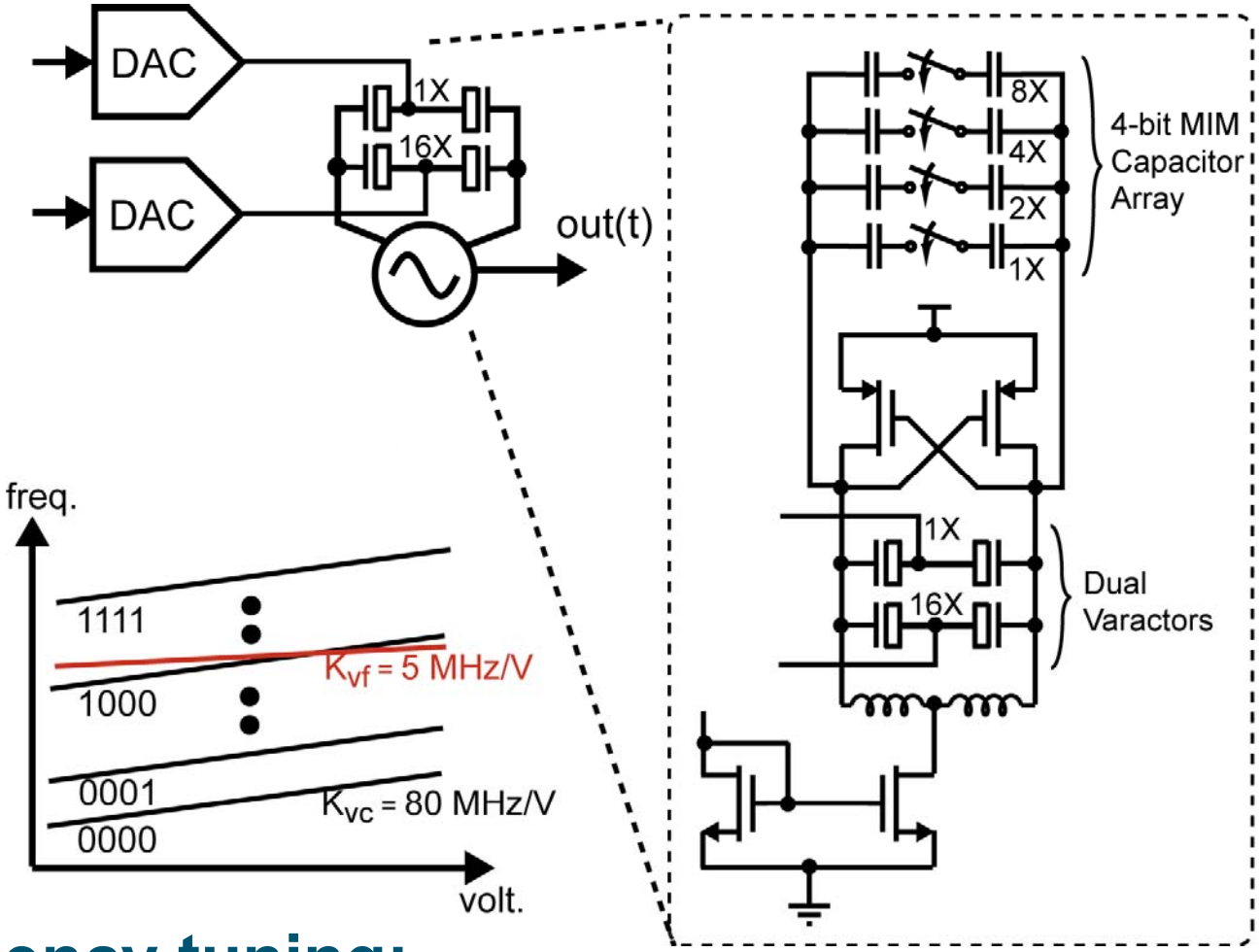
- *Gated-ring-oscillator (GRO) TDC* achieves low in-band noise
- *All-digital quantization noise cancellation* achieves low out-of-band noise
- Design goals:
  - 3.6-GHz carrier, 500-kHz bandwidth
  - <-100dBc/Hz in-band, <-150 dBc/Hz at 20 MHz offset

Overall Synthesizer Architecture



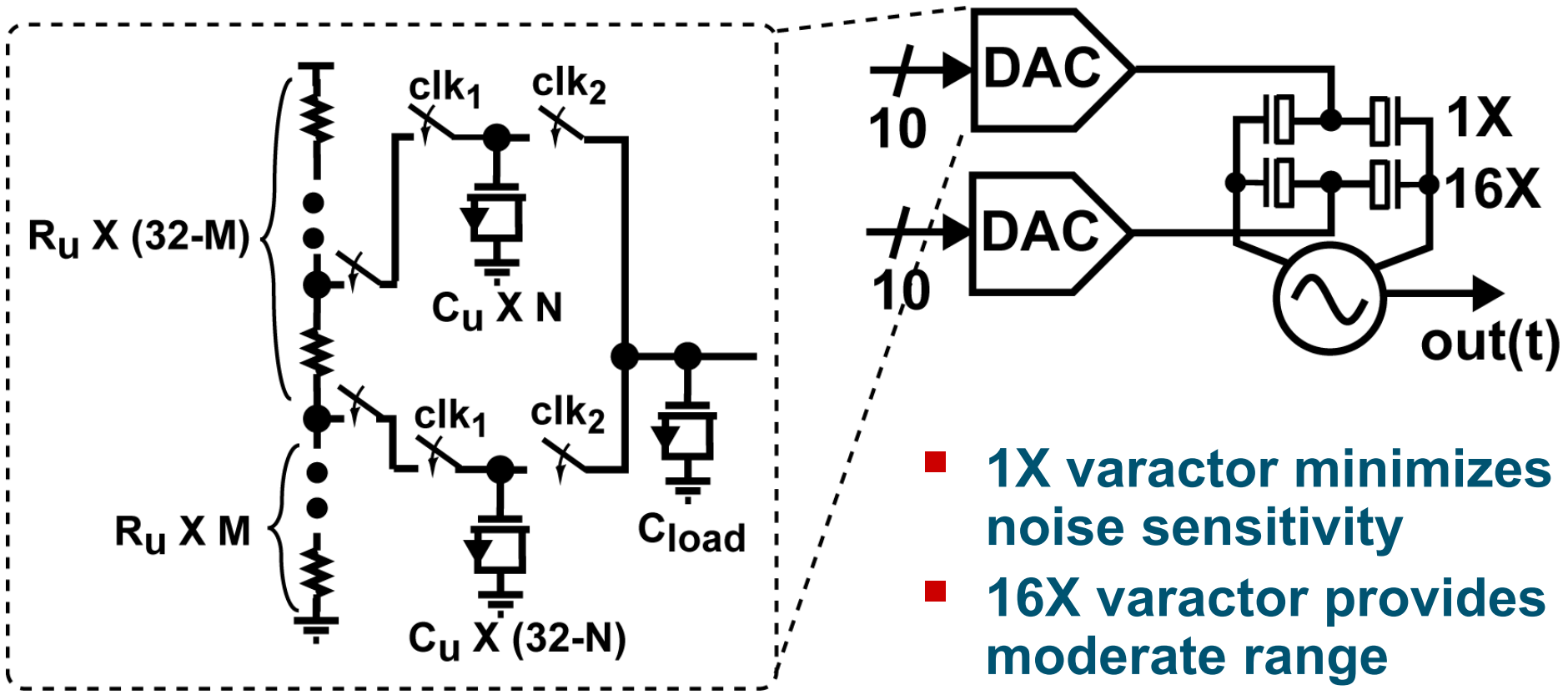
Note: Detailed behavioral simulation model available at http://www.cppsim.com

Dual-Port LC VCO



- **Frequency tuning:**
  - **Use a small 1X varactor to minimize noise sensitivity**
  - **Use another 16X varactor to provide moderate range**
  - **Use a four-bit capacitor array to achieve 3.3-4.1 GHz range**

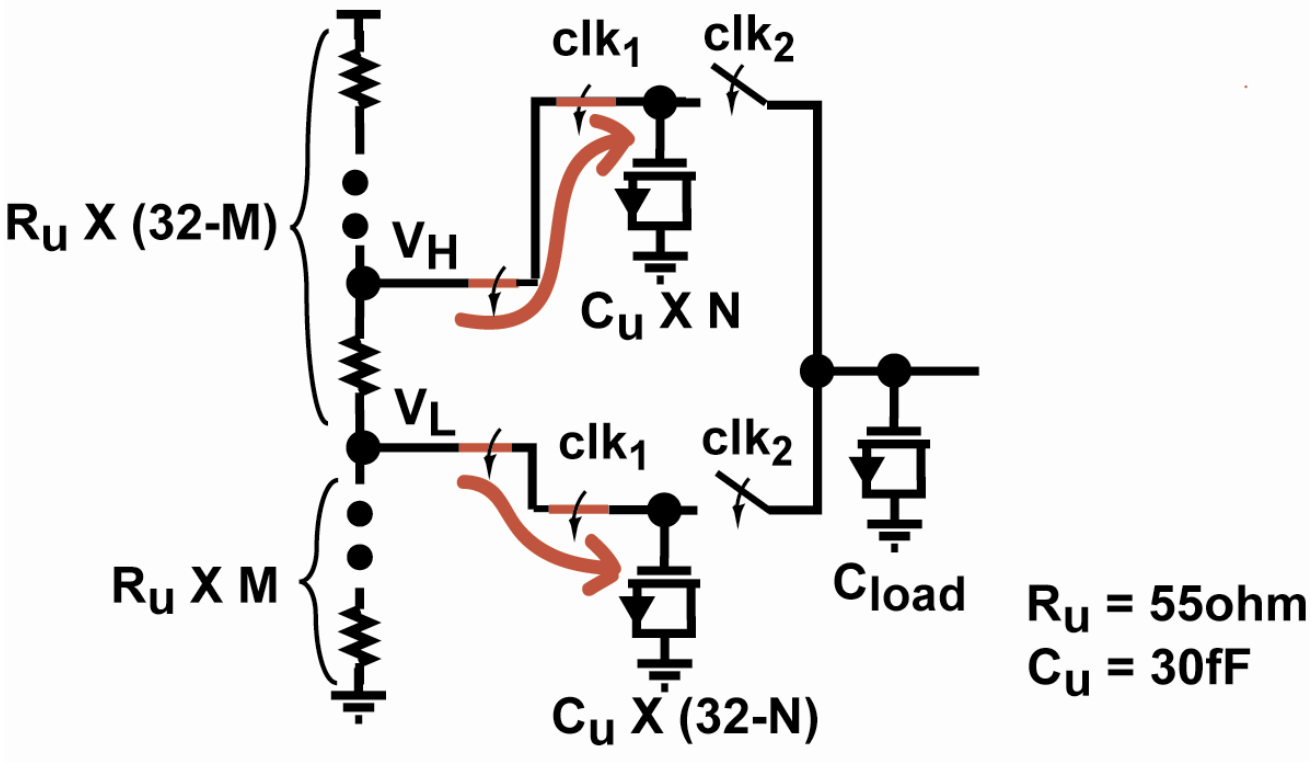
Digitally-Controlled Oscillator with Passive DAC



- 1X varactor minimizes noise sensitivity
- 16X varactor provides moderate range
- A four-bit capacitor array covers 3.3-4.1GHz

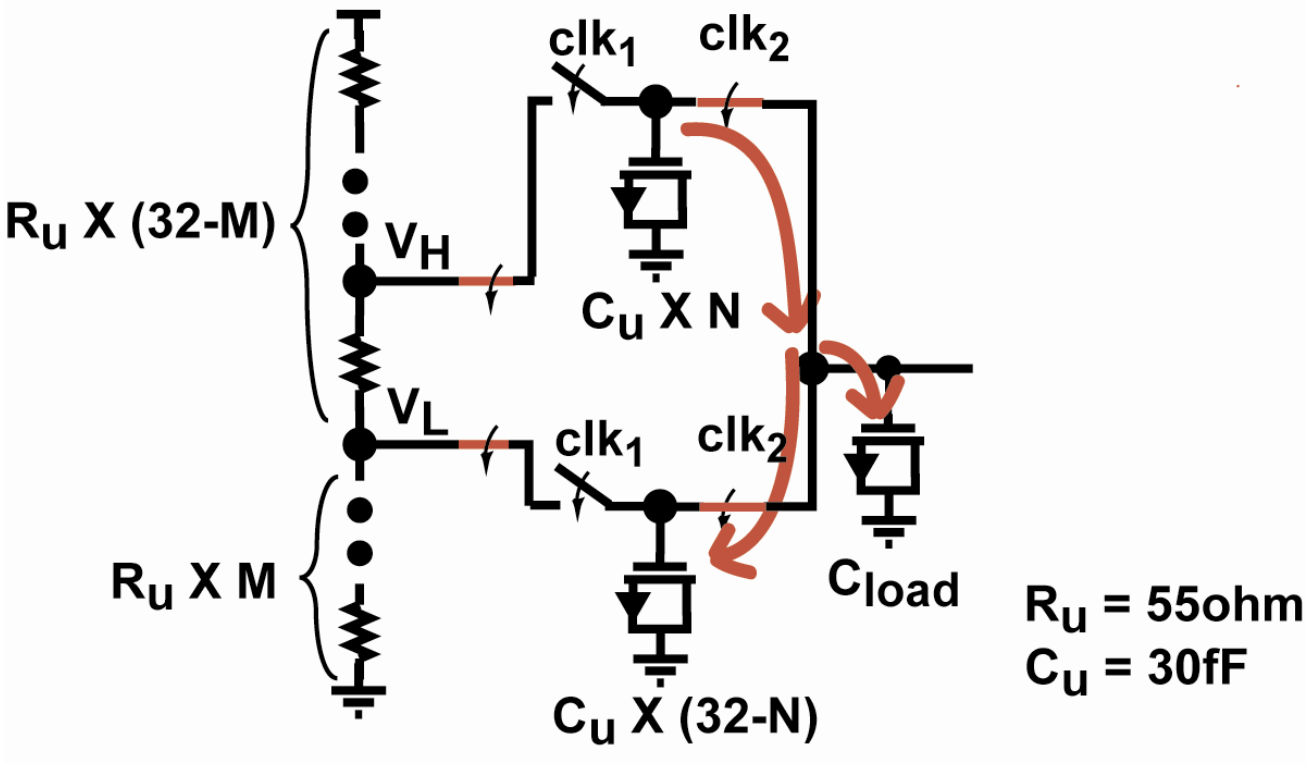
- Goals of 10-bit DAC
  - Monotonic
  - Minimal active circuitry and no transistor bias currents
  - Full-supply output range

Operation of 10-bit Passive DAC (Step 1)



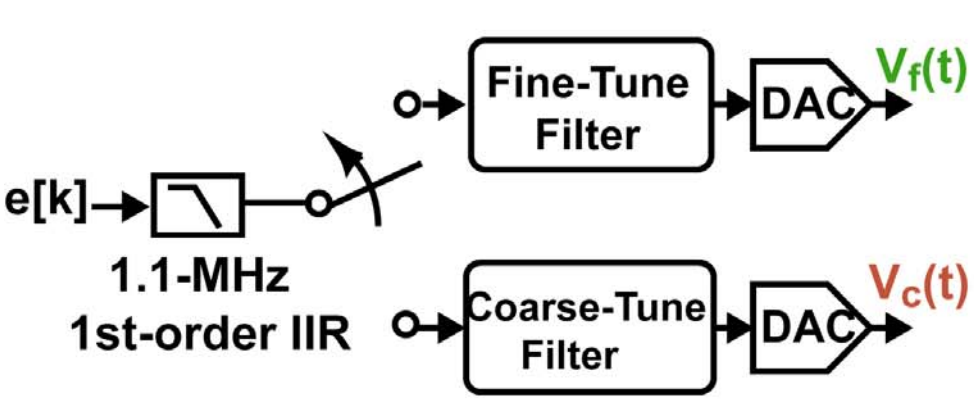
- 5-bit resistor ladder; 5-bit switch-capacitor array
- Step 1: *Capacitors Charged*
  - Resistor ladder forms $V_L = M/32 \cdot V_{DD}$ and $V_H = (M+1)/32 \cdot V_{DD}$, where M ranges from 0 to 31
  - N unit capacitors charged to V_H, and (32-N) unit capacitors charged to V_L

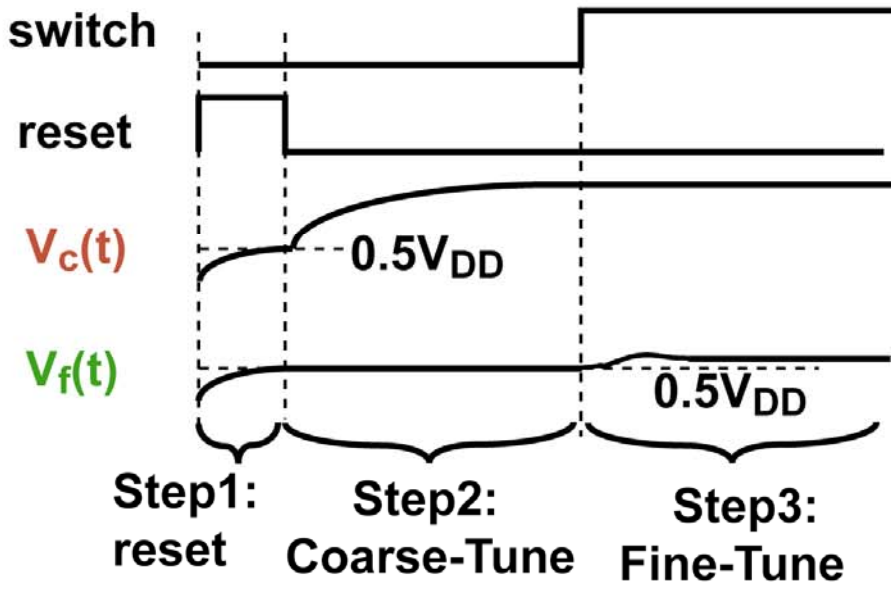
Operation of 10-bit Passive DAC (Step 2)



- **Step 2:** ***Disconnect Capacitors from Resistors, Then Connect Together***
  - **Achieves DAC output with first-order filtering**
  - **Bandwidth = 32• C_u/(2π•C_{load})•50MHz**
    - Determined by capacitor ratio
    - Easily changed by using different C_{load}

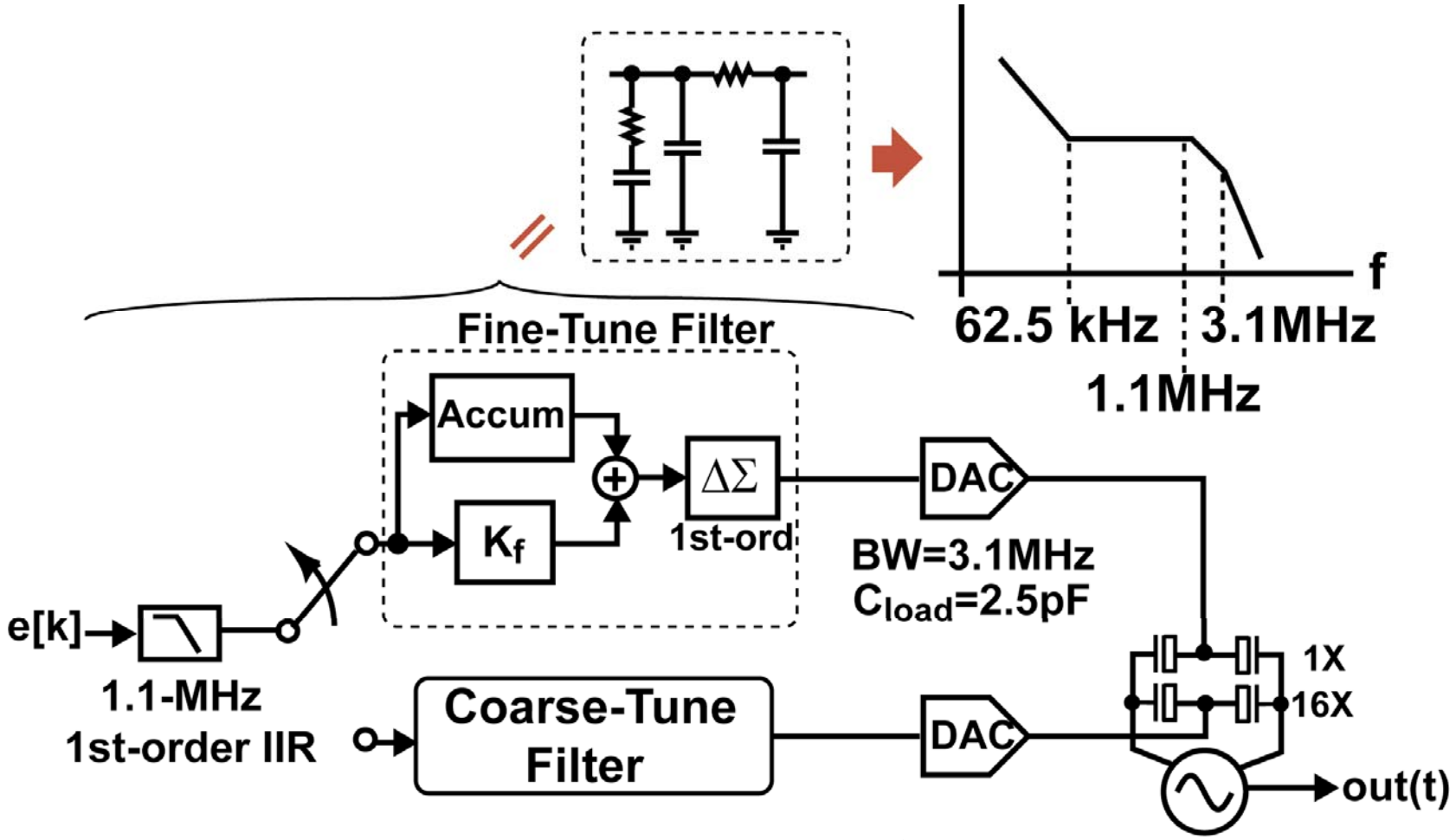
Dual-Path Loop Filter





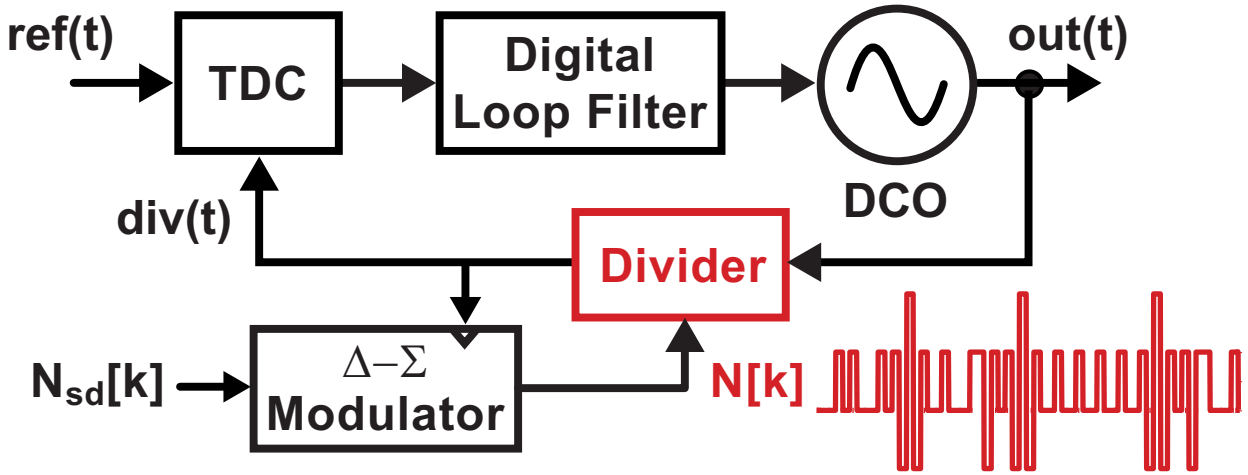
- Step 1: reset
- Step 2: frequency acquisition
  - $V_c(t)$ varies
  - $V_f(t)$ is held at midpoint
- Step 3: steady-state lock conditions
  - $V_c(t)$ is frozen to take quantization noise away
  - ΔΣ quantization noise cancellation is enabled

Fine-Path Loop Filter



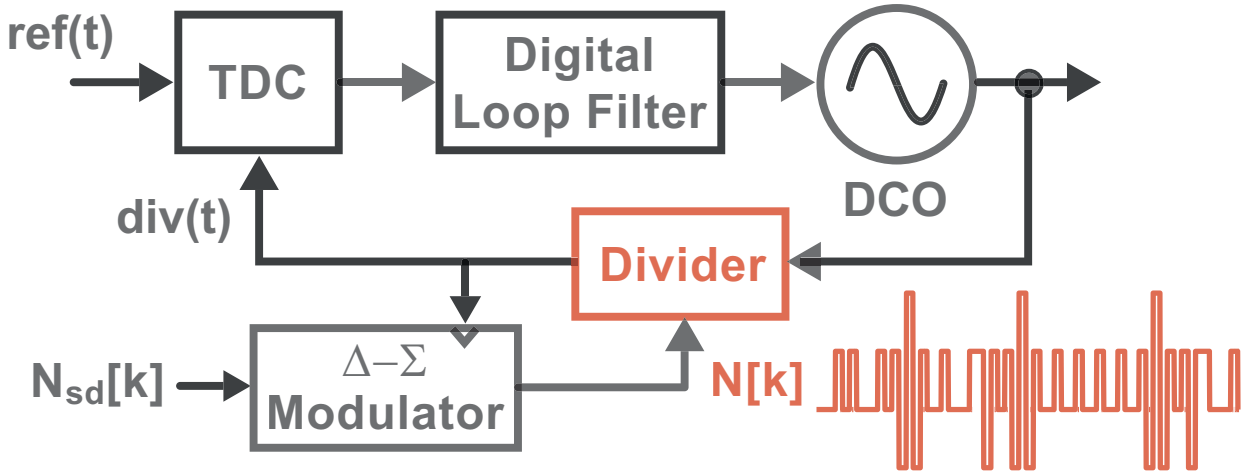
- Equivalent to an analog lead-lag filter
  - Set zero (62.5kHz) and first pole (1.1MHz) digitally
  - Set second pole (3.1MHz) by capacitor ratio
- First-order ΔΣ reduces in-band quantization noise

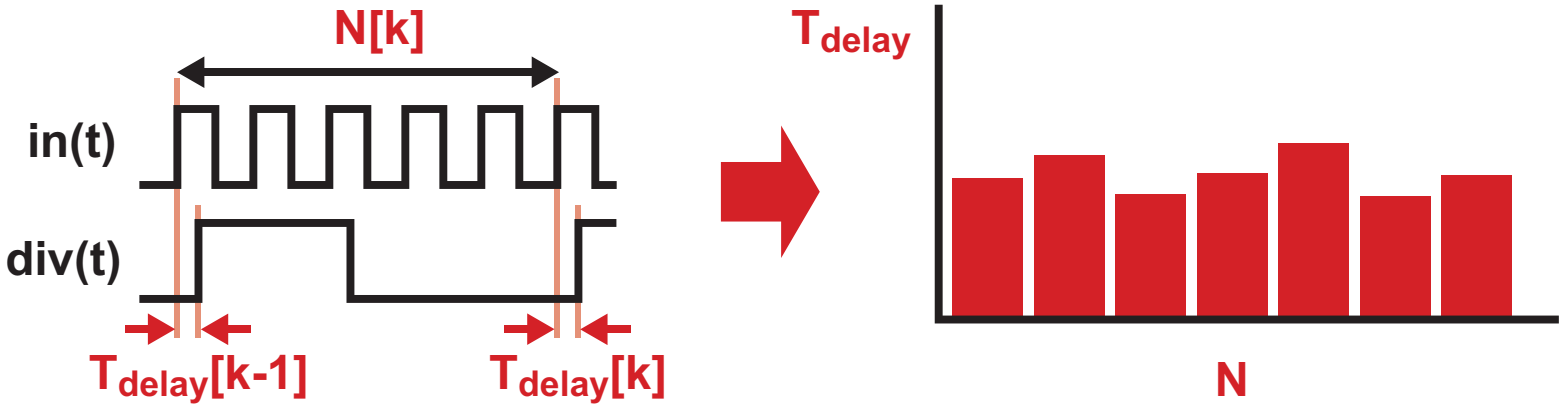
A Closer Look at the Frequency Divider



- Delta-Sigma modulator dithers the divider value
  - Divider must support a range of divide values
  - Want to maintain low jitter as divide value changes

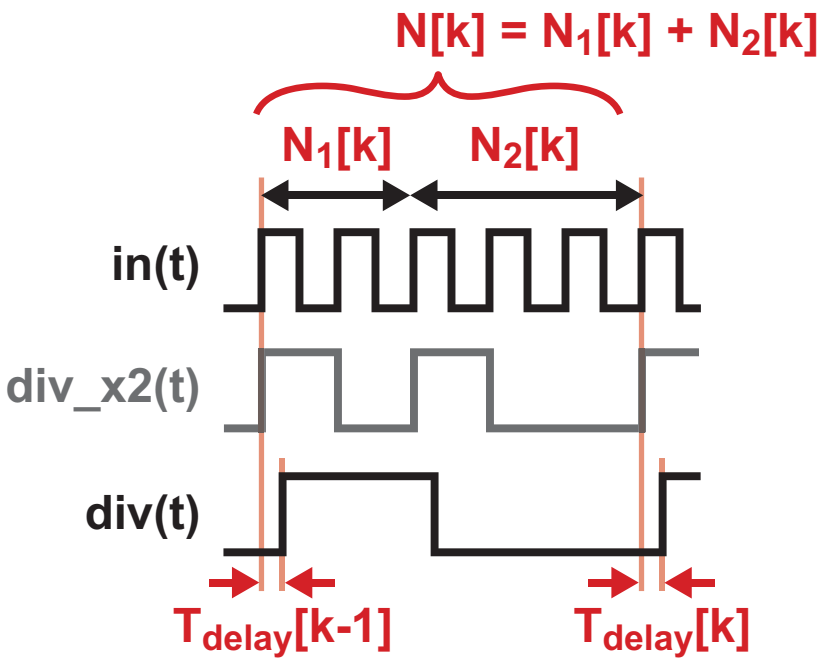
The Issue of Divide Value Delay Variation





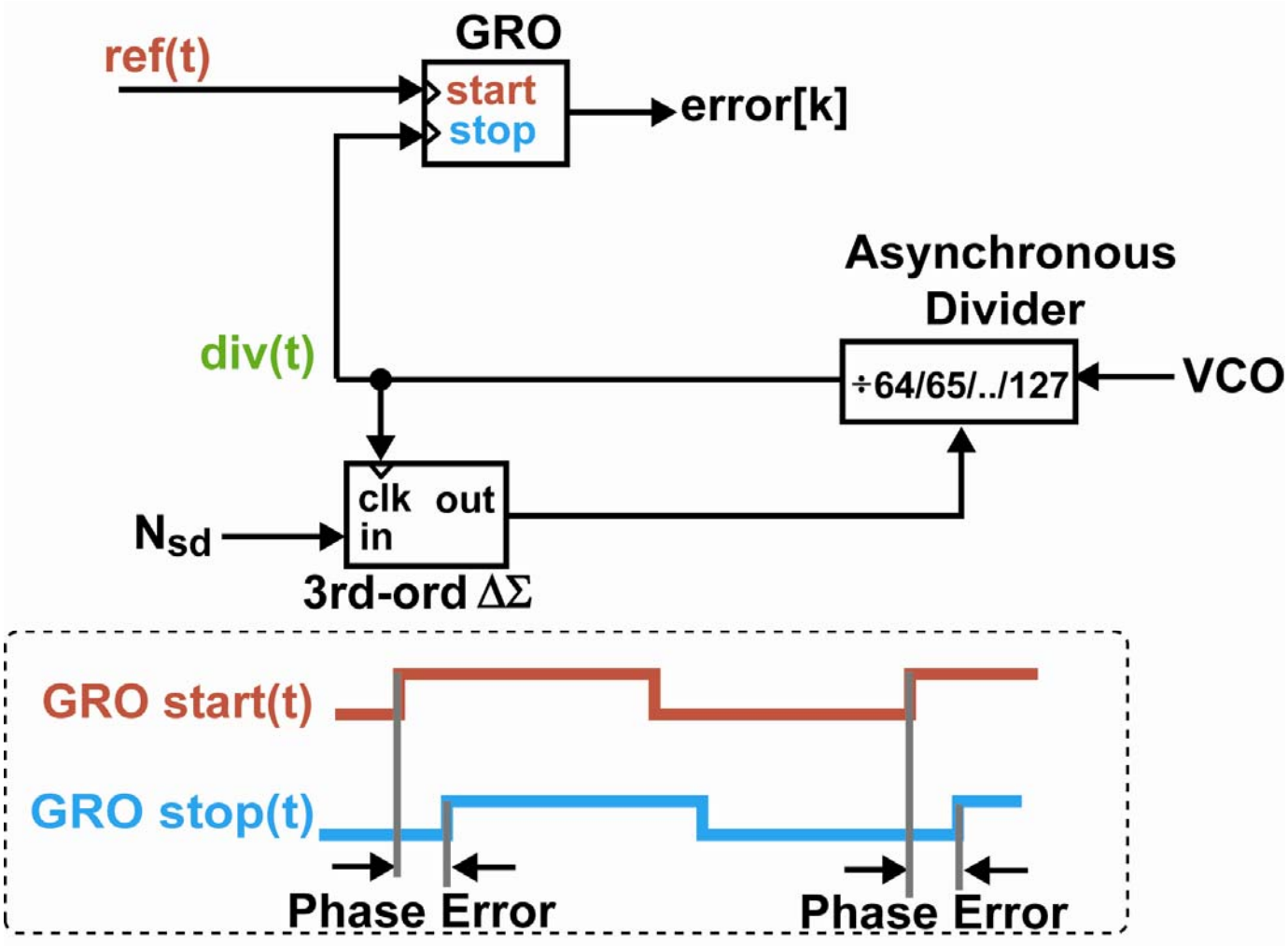
- Divider input to output delay is a function of divide value
  - Adds significant jitter for dynamic divide value variation

Key Observation



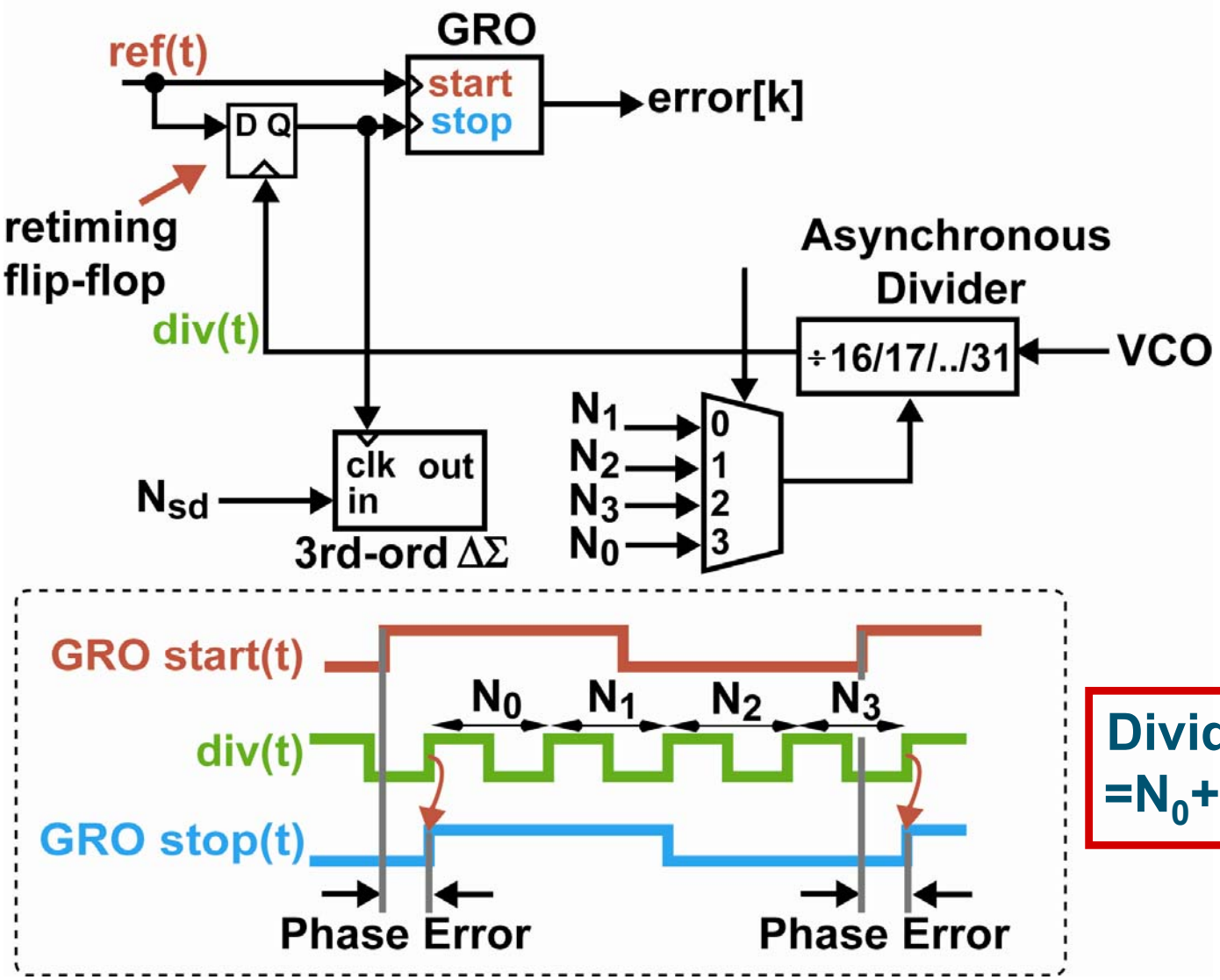
- We can realize a given divide value as the sum of lower divide values
  - Only pass select edges from higher frequency divider

Application of Divider Concept to Digital PLL



- Example: desired frequency division range is 64 to 127
  - Dithered by a third order Delta-Sigma modulator

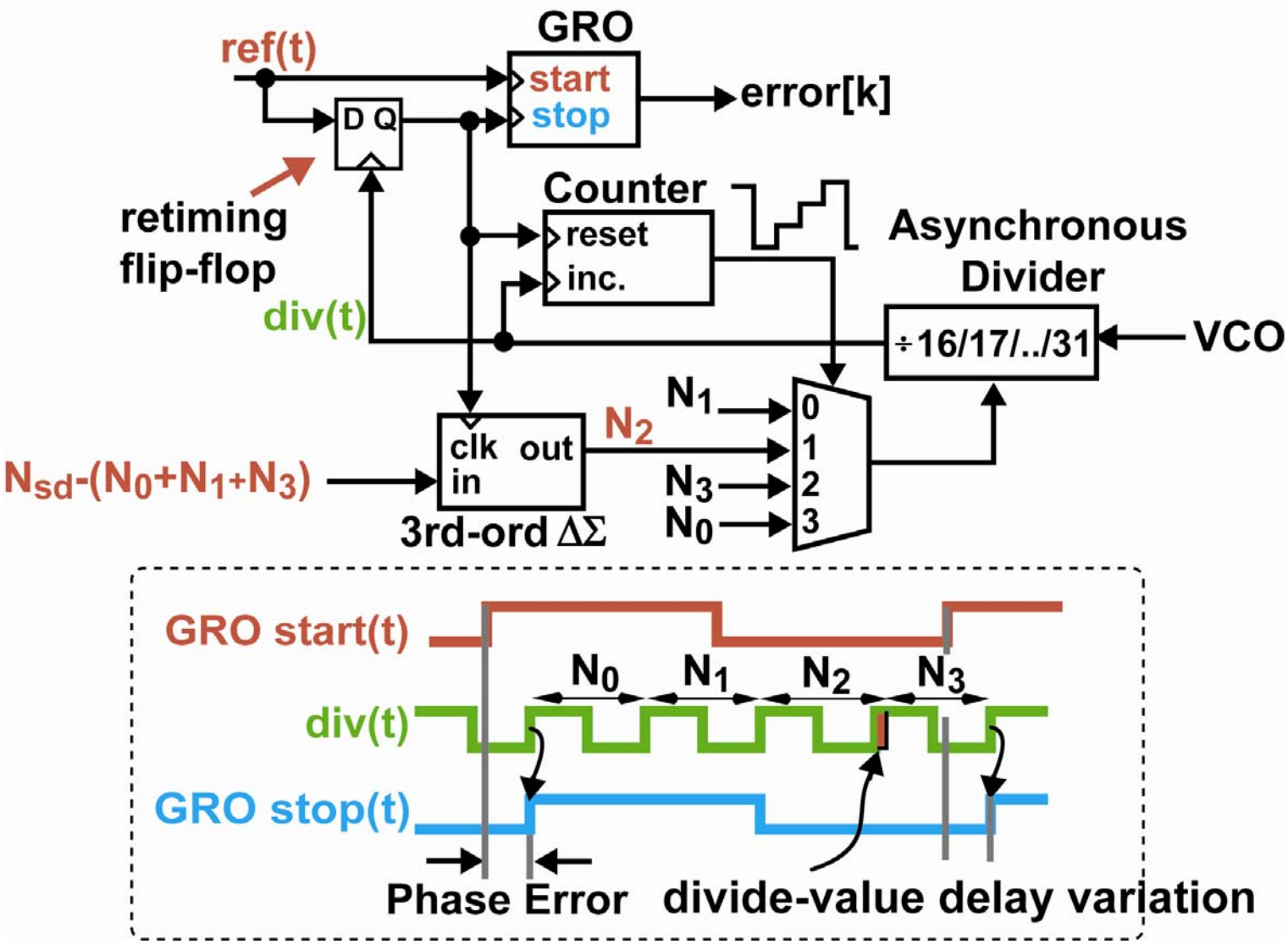
Proposed Divider Structure



Divide value
$=N_0+N_1+N_2+N_3$

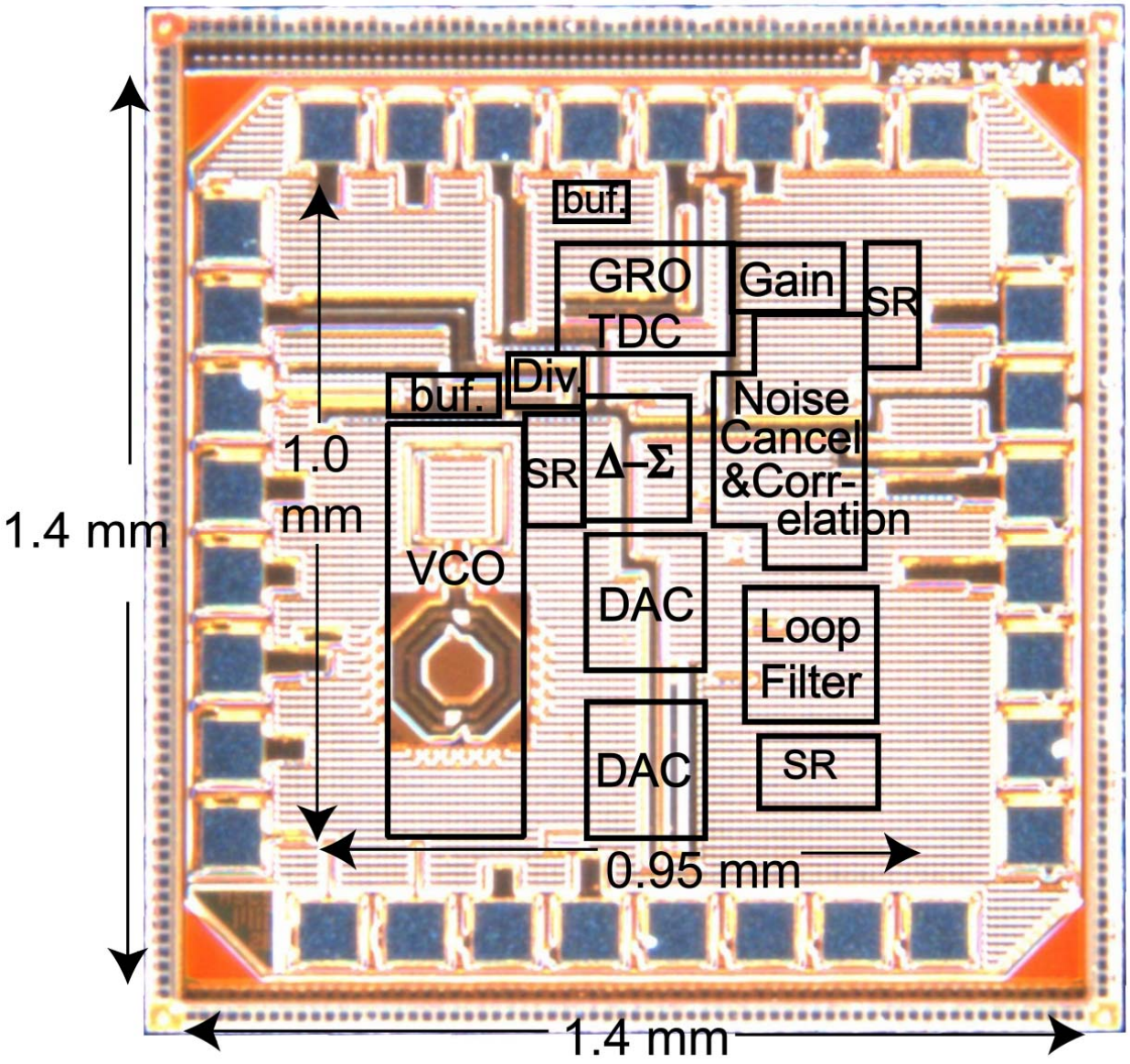
- **Increase division frequency by a factor of 4**
  - **Only pass one of four divider edges to GRO TDC**

Removal of Divide Value Delay Variation



- Place ΔΣ dithered edge (N_2) on edge *not* passed to GRO
  - Divide value (N_3) is *constant* for edge that passes to GRO

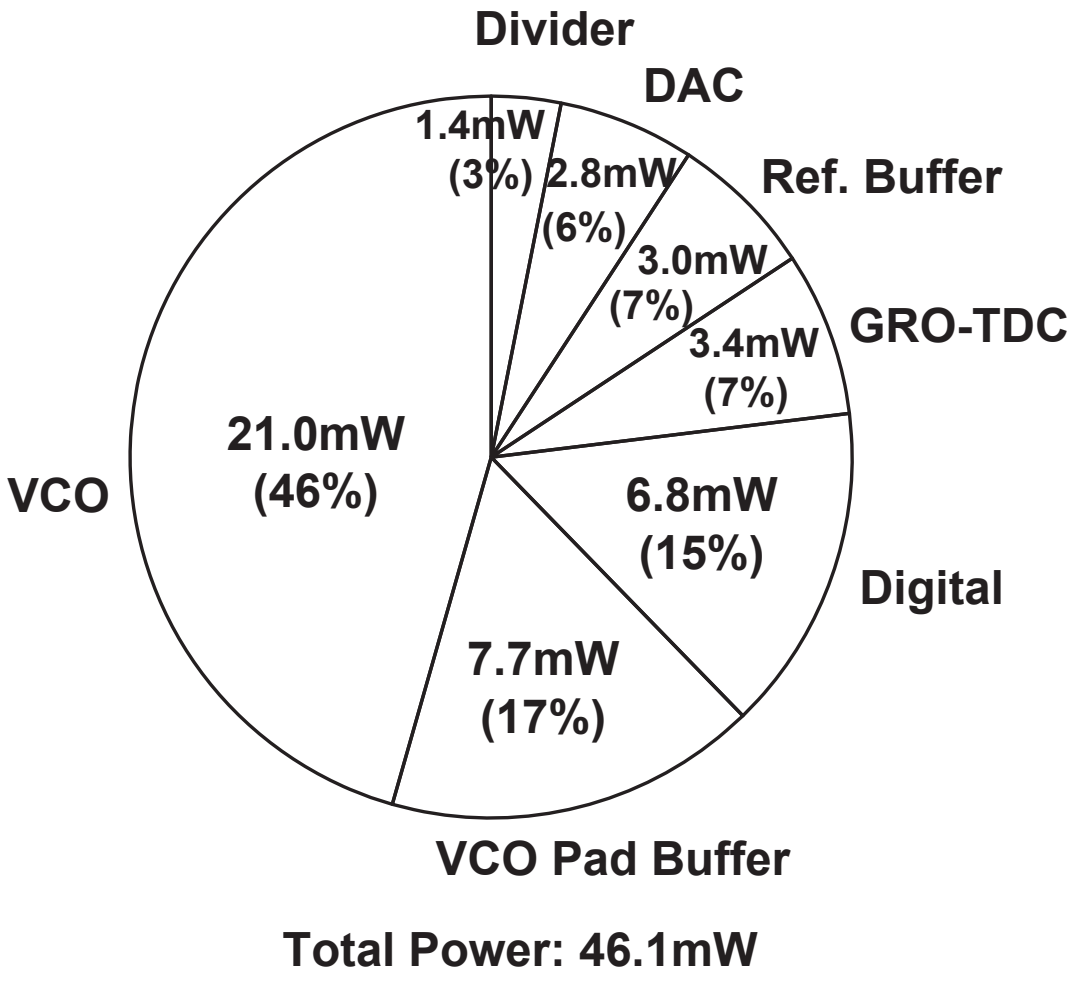
Die Photo of Prototype



- 0.13-μm CMOS
- Active area: 0.95 mm^2
- Chip area: 1.96 mm^2
- V_{DD}: 1.5V
- Current:
  - 26mA (Core)
  - 7mA (VCO output buffer at 1.1V)

GRO-TDC:
- 2.3mA
- 157X252 um^2

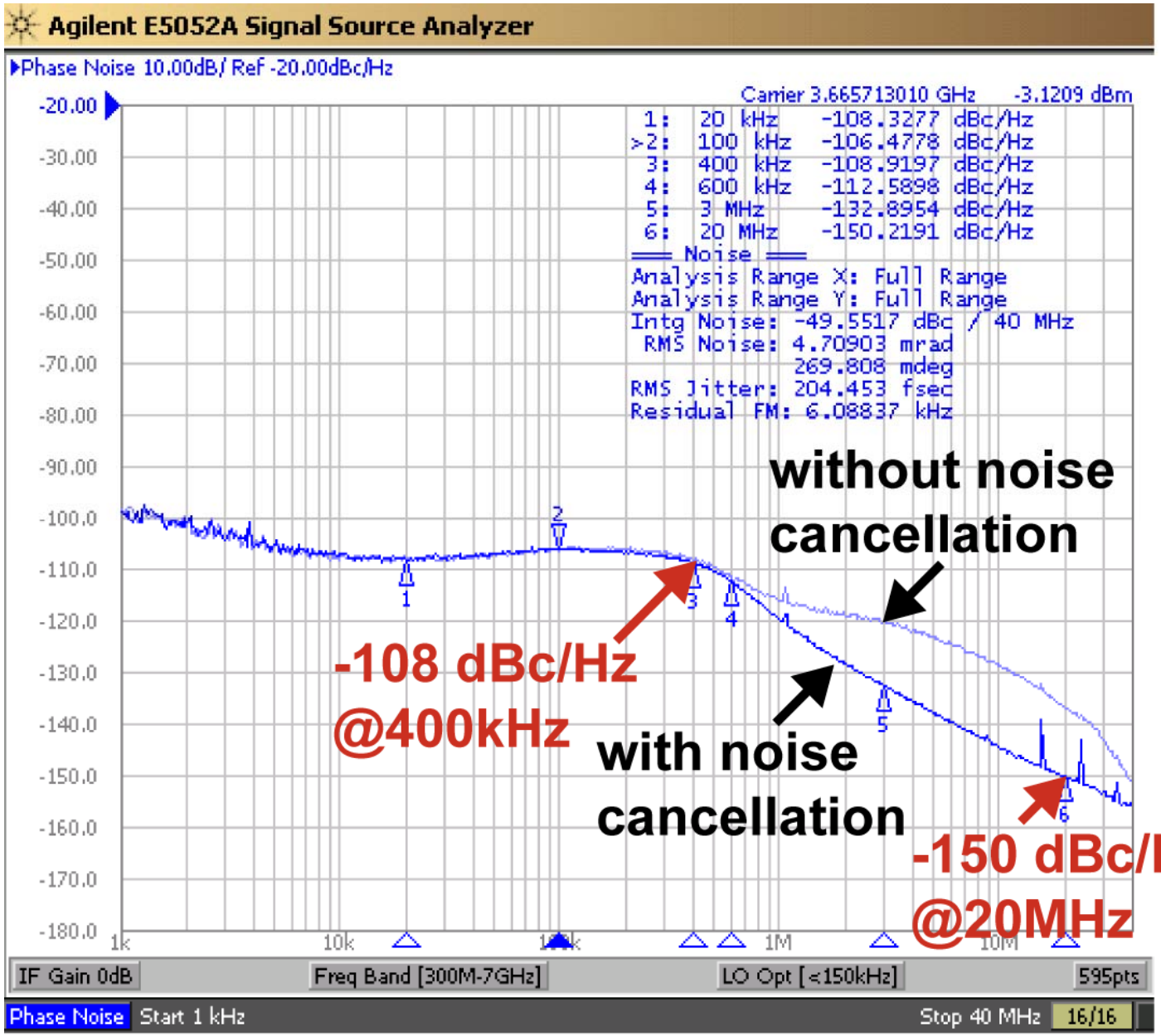
Power Distribution of Prototype IC



Total Power: 46.1mW

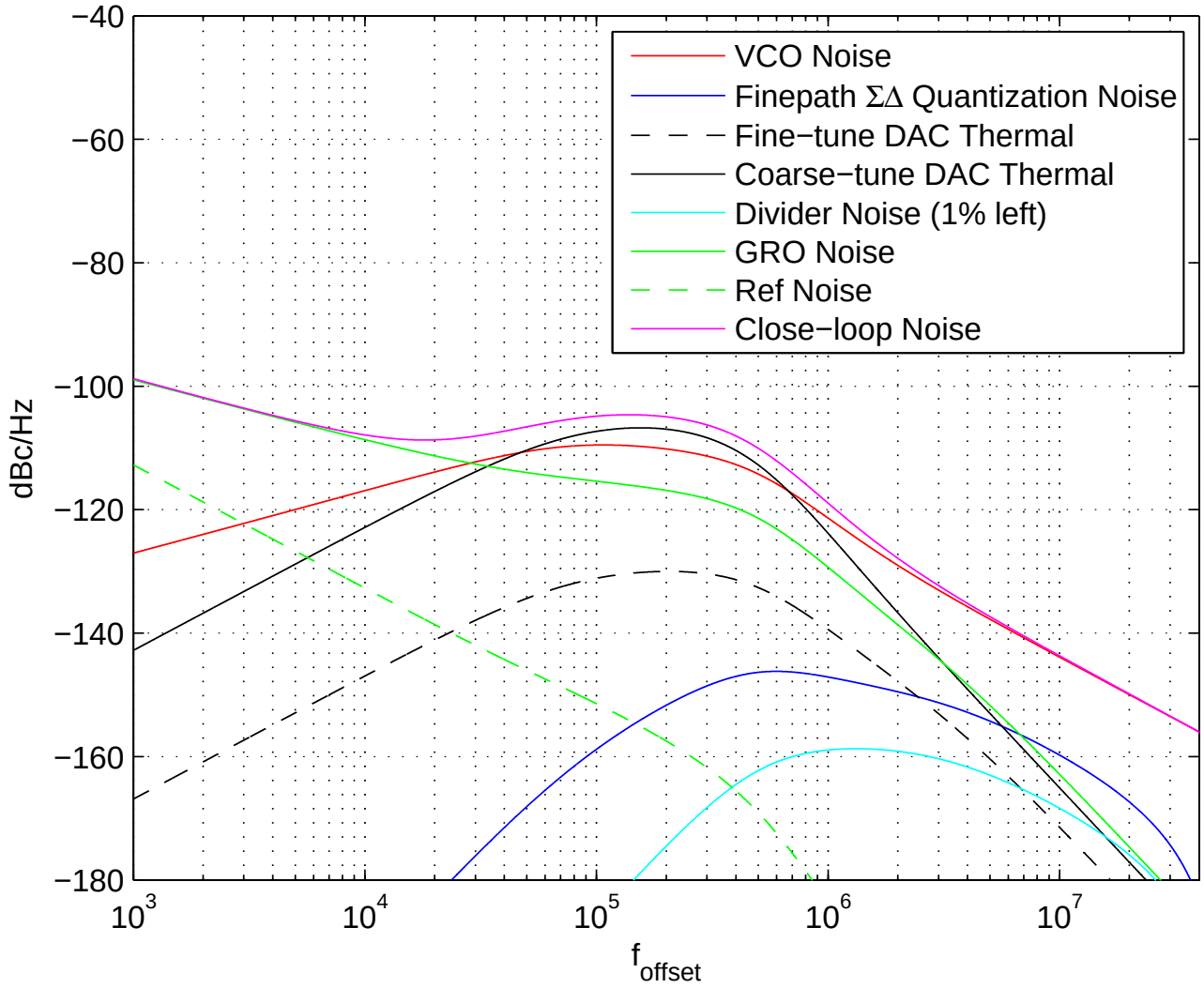
- **Notice GRO and digital quantization noise cancellation have only minor impact on power (and area)**

Measured Phase Noise at 3.67GHz



- Suppresses quantization noise by more than 15 dB
- Achieves 204 fs (0.27 degree) integrated noise (jitter)
- Reference spur: -65dBc

Calculation of Phase Noise Components



- **See wideband digital synthesizer tutorial available at http://www.cppsim.com**

Conclusions

- **Digital Phase-Locked Loops look extremely promising for future applications**
  - **Very amenable to future CMOS processes**
  - **Excellent performance can be achieved**

- **A low-noise, wide-bandwidth digital ΔΣ fractional-N frequency synthesizer is achieved with**
  - **High performance *noise-shaping* GRO TDC**
  - **Quantization noise cancellation in *digital* domain**

- **Key result: < *250 fs* integrated noise with 500 kHz bandwidth**

Innovation of future digital PLLs will involve joint circuit/algorithm development