Future Directions for Silicon Radio Frequency Electronics

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Outline

- Challenge Driven Research
- RF Systems on a Chip:
  - **Focused on silicon CMOS technology**
  - **New paradigms for analog/RF circuit design**
- Opportunities for silicon electronics
  - **Scalable, reconfigurable, adaptive circuits (Digital RF)**
  - **Autonomous, low-power radio**
  - **High-speed networking**
- Summary

Challenge Driven Research

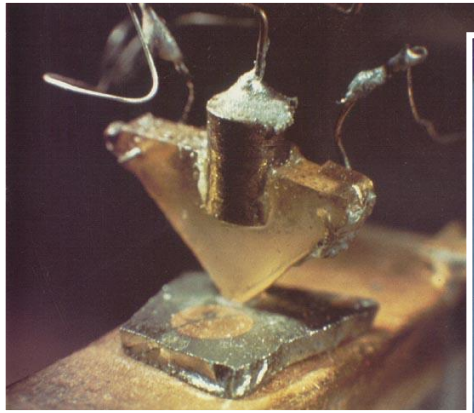
- *Grand Challenges* address important social and environmental problems. They are not defined, assessed or solved by a single scientific or technical discipline.
- Two of the 12 themes identified for challenge driven research and innovation are:

  - Counteracting climate change
  - Ensuring well being and quality of life

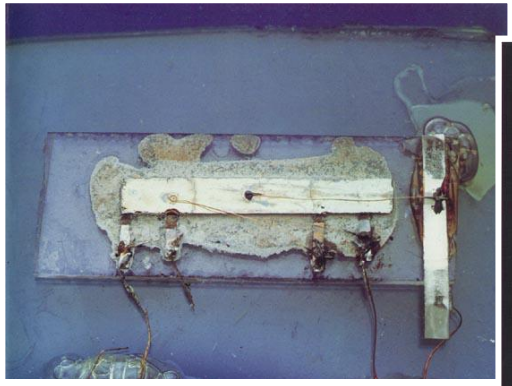
- **Energy**: Conservation in the generation, distribution, storage and consumption of energy
- **Healthy Ageing**: Improve healthcare delivery to an ageing population

Moore's Law Made Transistors Cheap

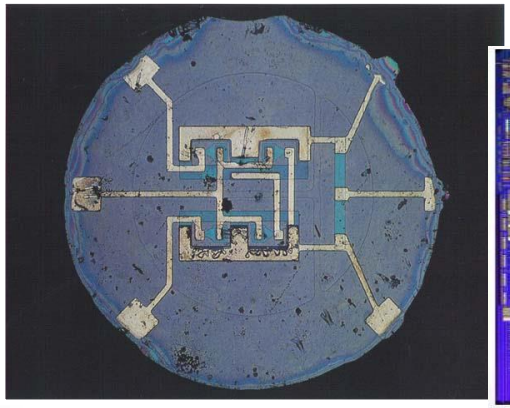
1947
Point-Contact Transistor
Bell Labs



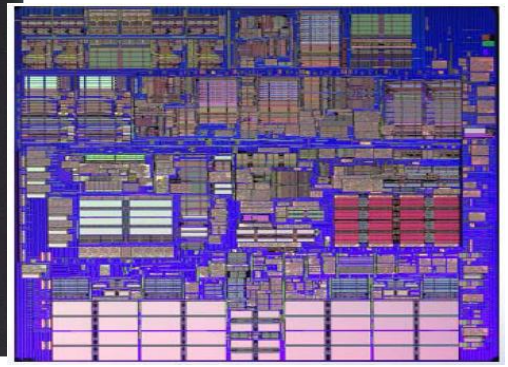
1958
First IC
Texas Instruments

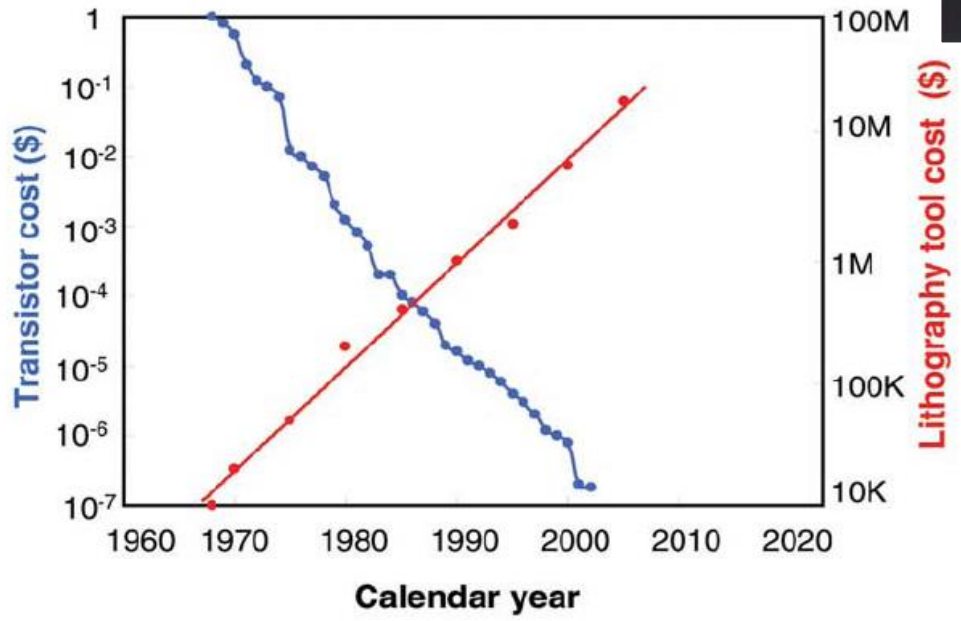


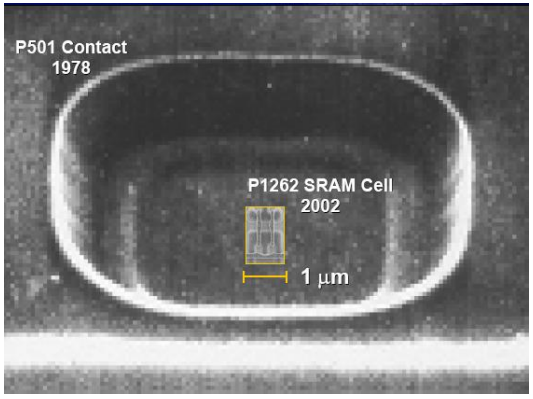
1961
First Planar IC
Fairchild



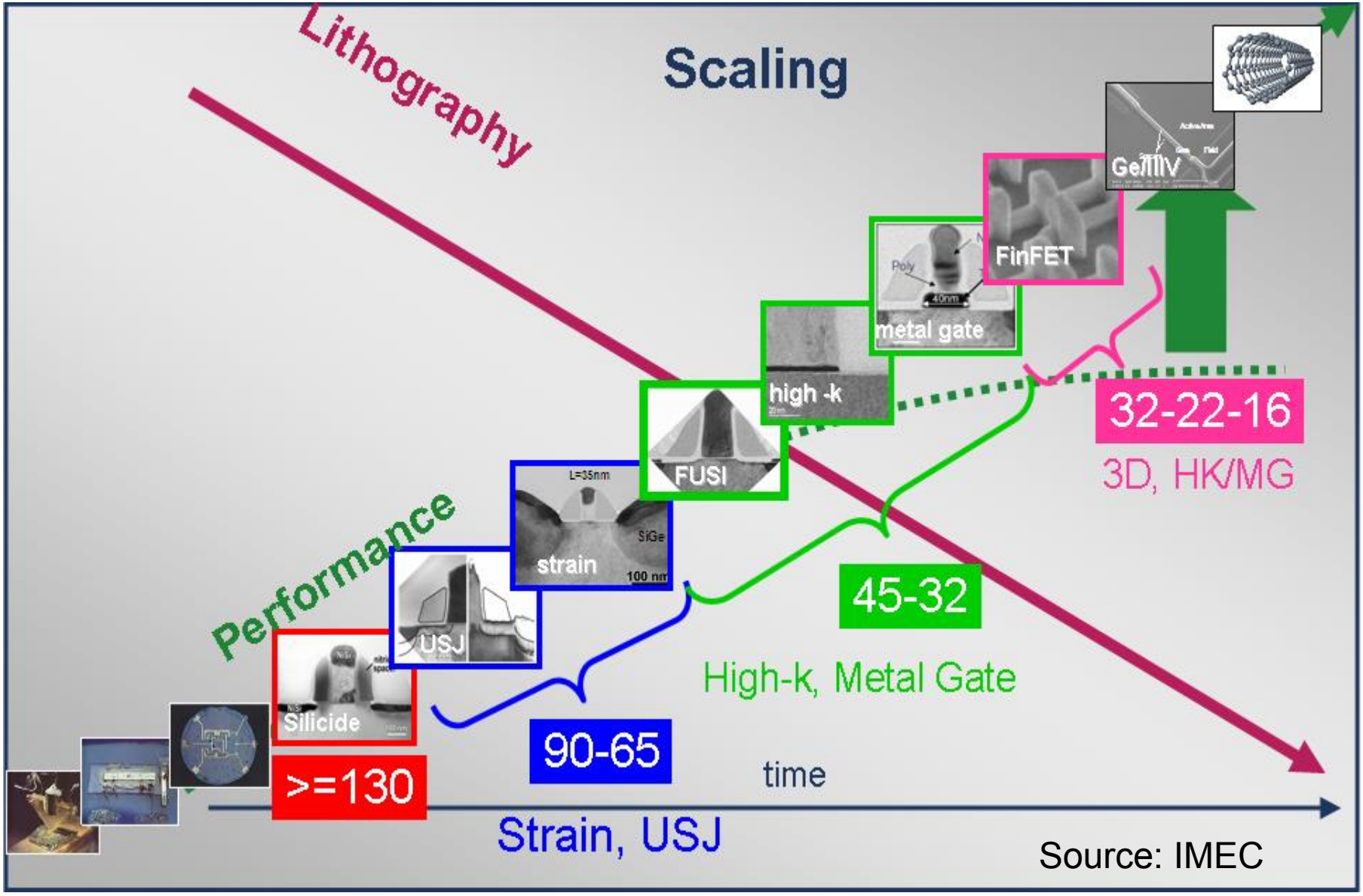
2014
Power PC
IBM





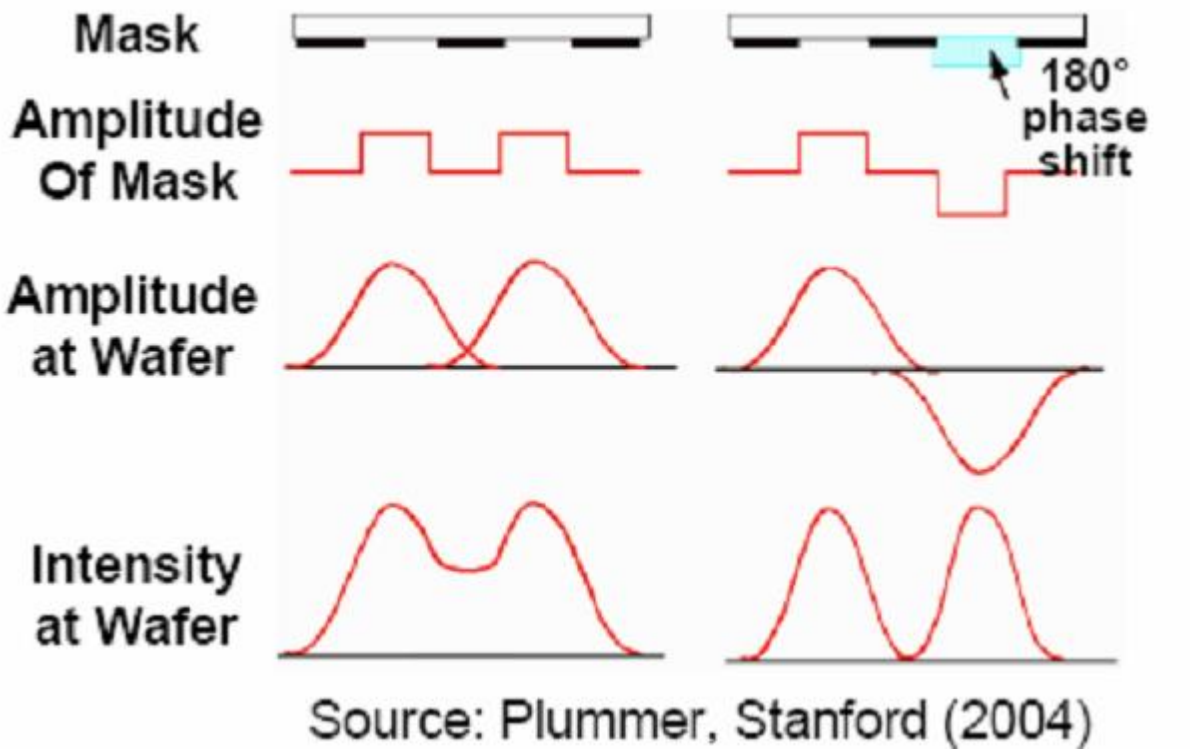


Scaling CMOS to the Limit



What You See is *Not* What You Get!

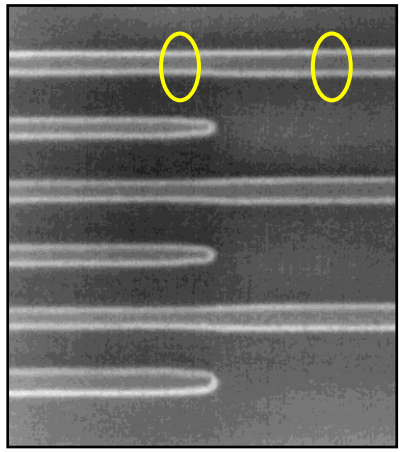
Phase-Shift Masking



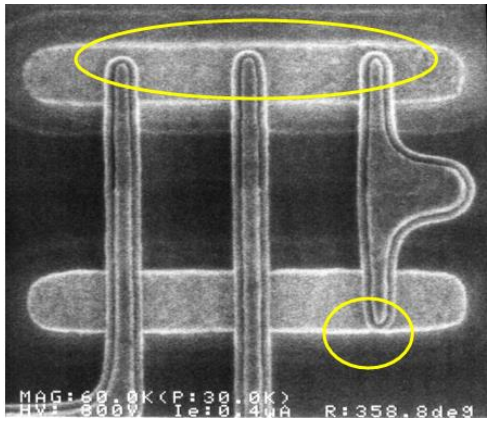
- Sharp features lost because diffraction attenuates and distorts higher spatial frequencies (mask acts as a narrowband optical filter).

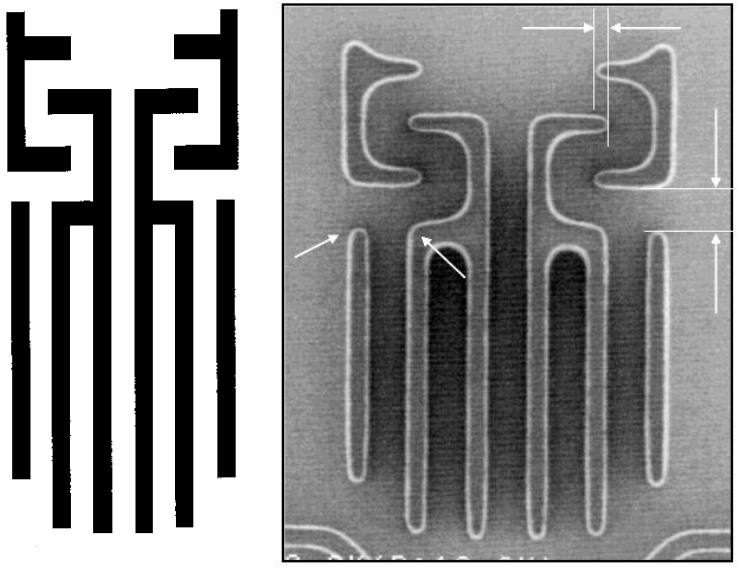
Optical Correction Techniques

Dense vs. Isolated CD Offset

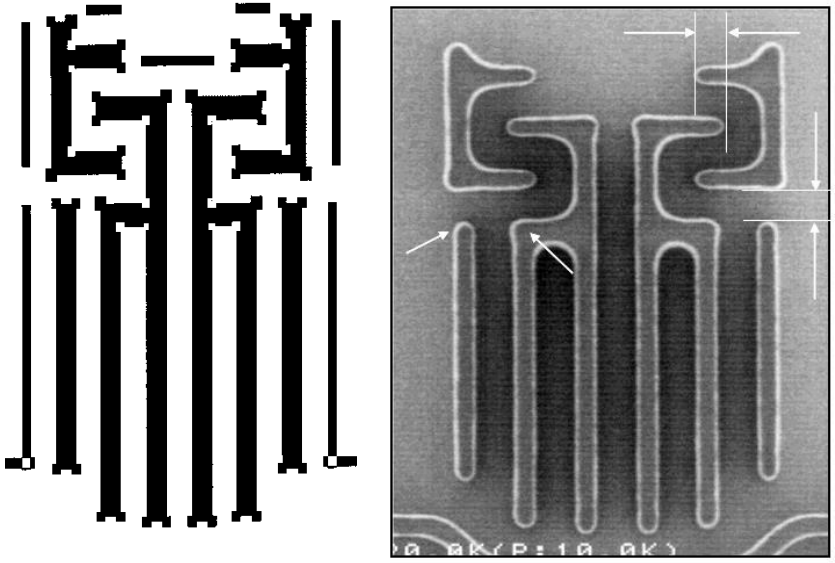


End-Of-Line Shortening





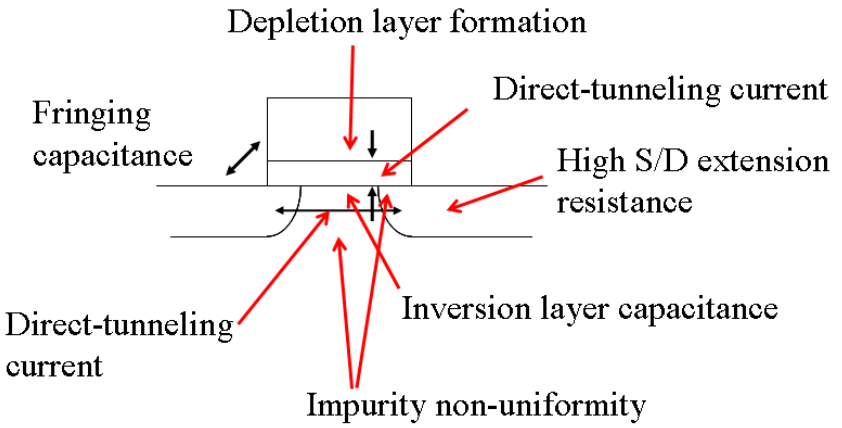
Non-Corrected

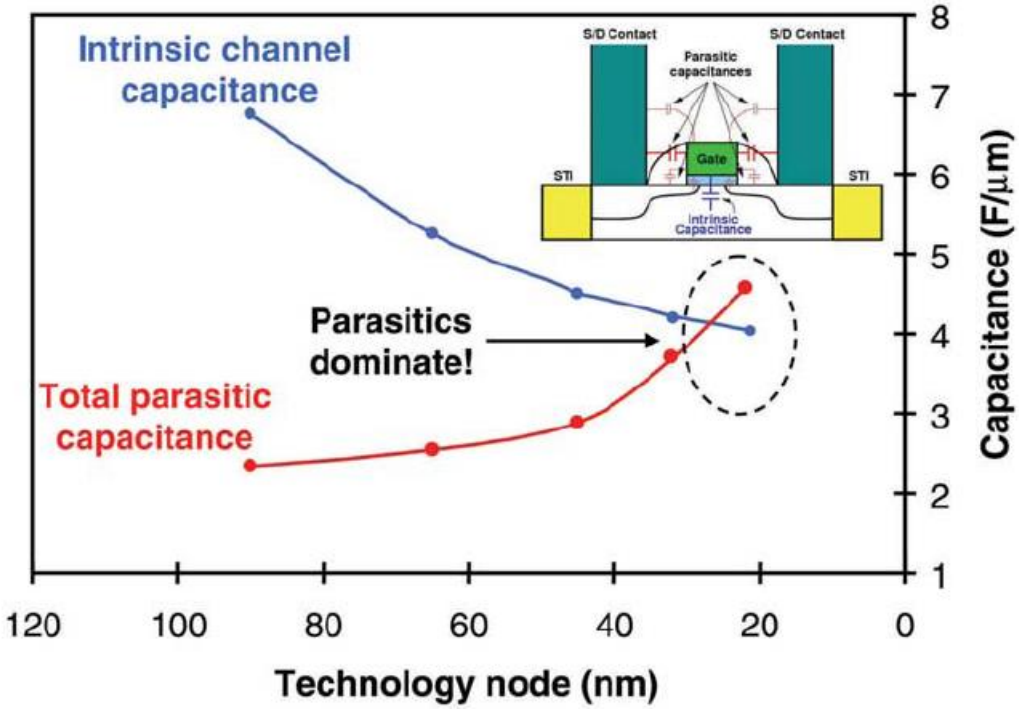


With Sub-resolution Assisting Features

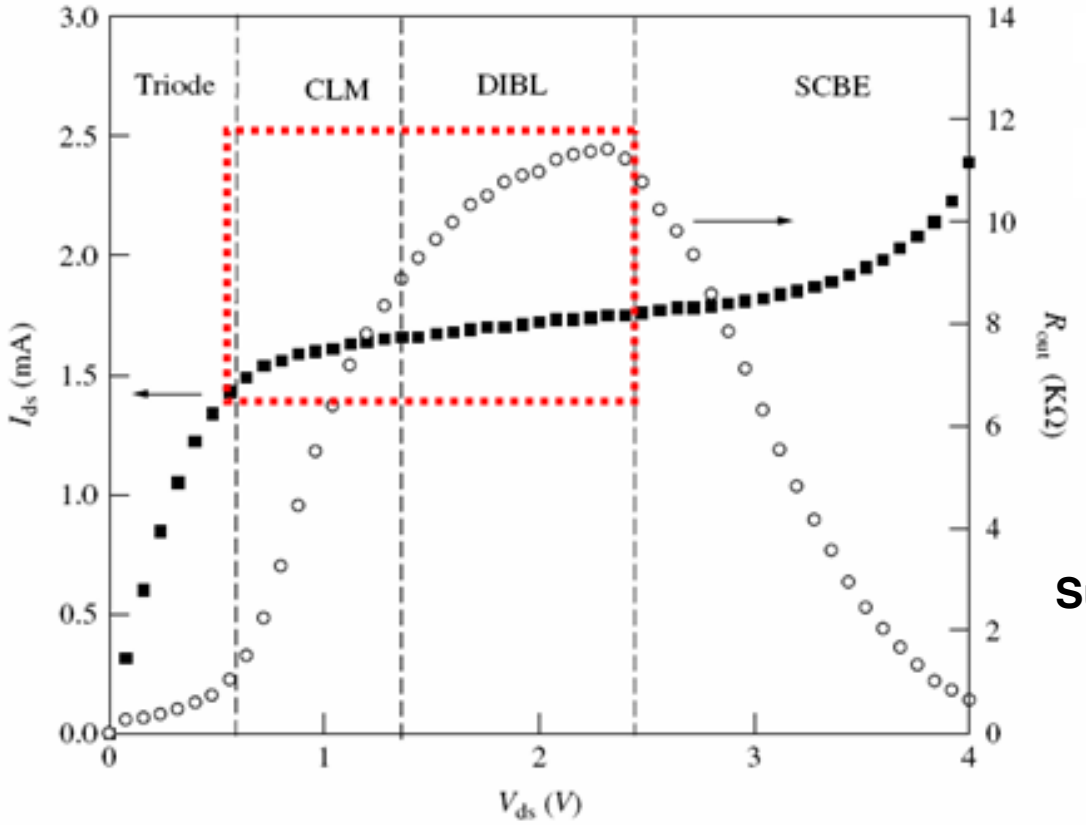
Deep Submicron/Parasitic Effects

- Reduction of Design Headroom
- (Reverse) Short Channel Effect (SCE and RSCE)
- Drain Induced Barrier Lowering (DIBL)
- Early Voltage and Output Resistance (V_A , r_{out})
- Polysilicon Depletion and Quantum Effects
- Gate Current Tunneling
- Mobility Reduction (doping, field..)
- Series Resistances (R_g, R_s) (NiSi can scale)
- Parasitic Capacitances (FE/BE)
- Electrical FOMs for Analog and RF
- Systematic Variability
  - Well Proximity
  - Strain
  - STI stress
- Stochastic Variability: mismatch, noise
- etc. ….





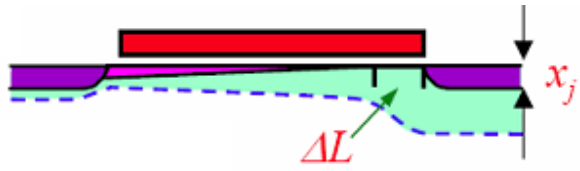
Output Resistance



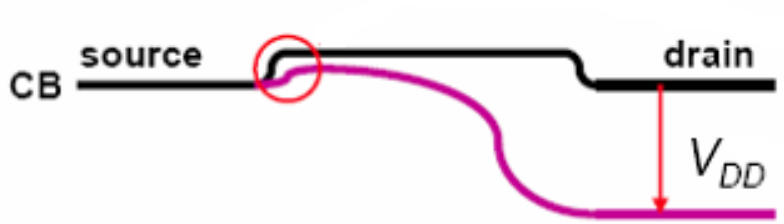
Output conductance behavior of a MOSFET at different bias regions

J. H. Huang, *et al. [BSIM]*

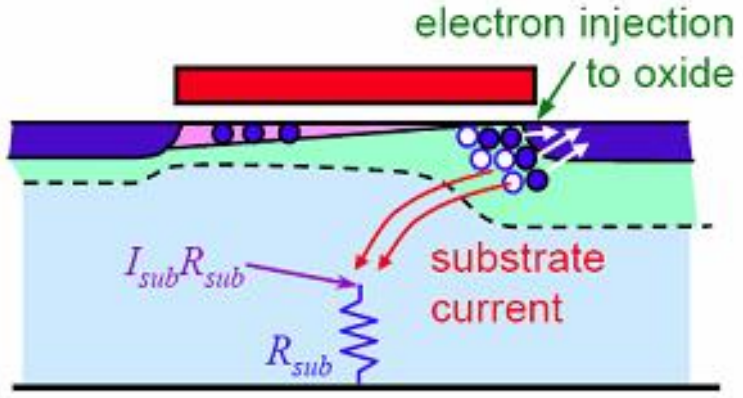
Channel Length Modulation (CLM)



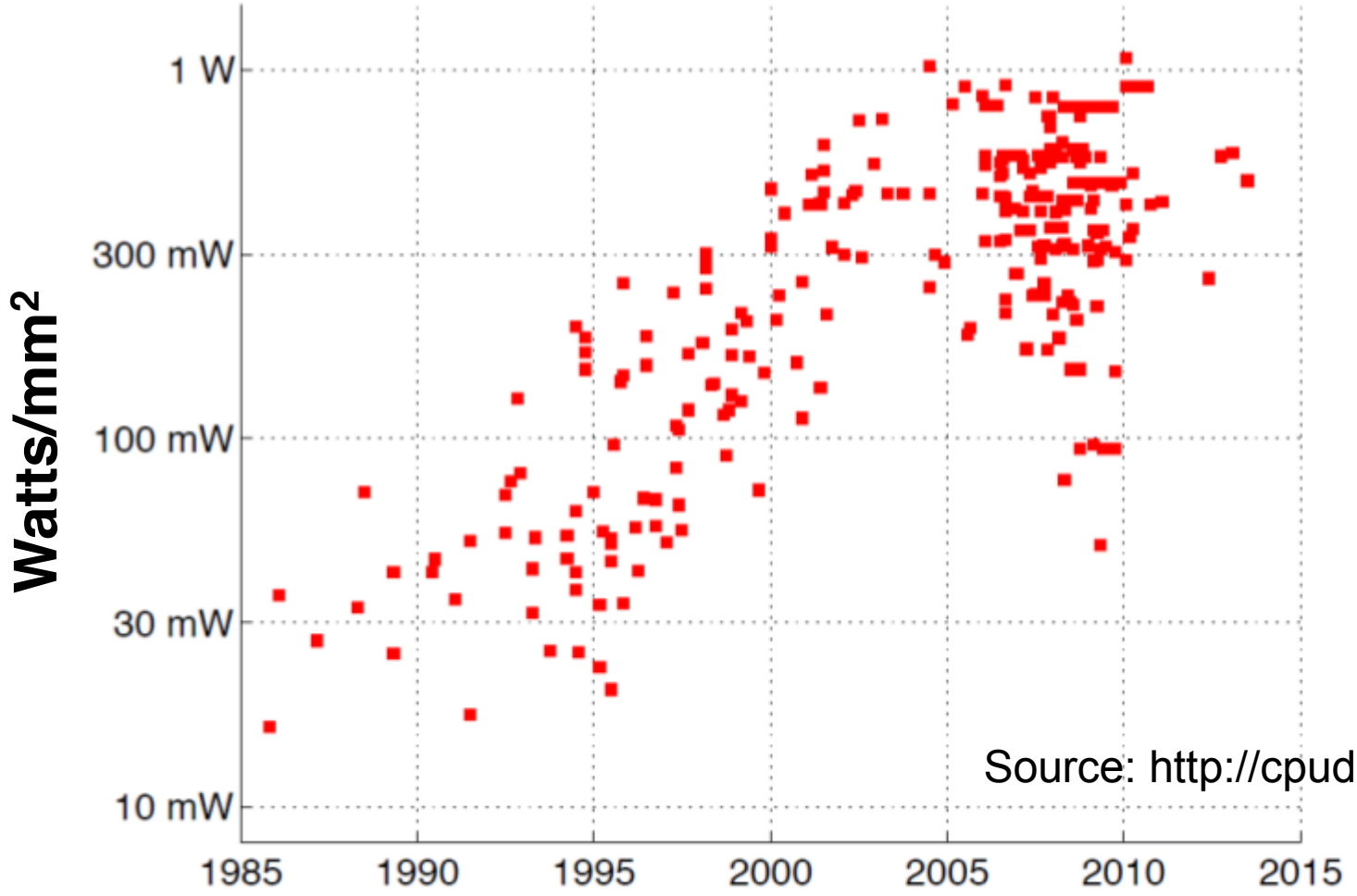
Drain Induced Barrier Lowering (DIBL)



Substrate Current Induced Body Effect (SCBE)

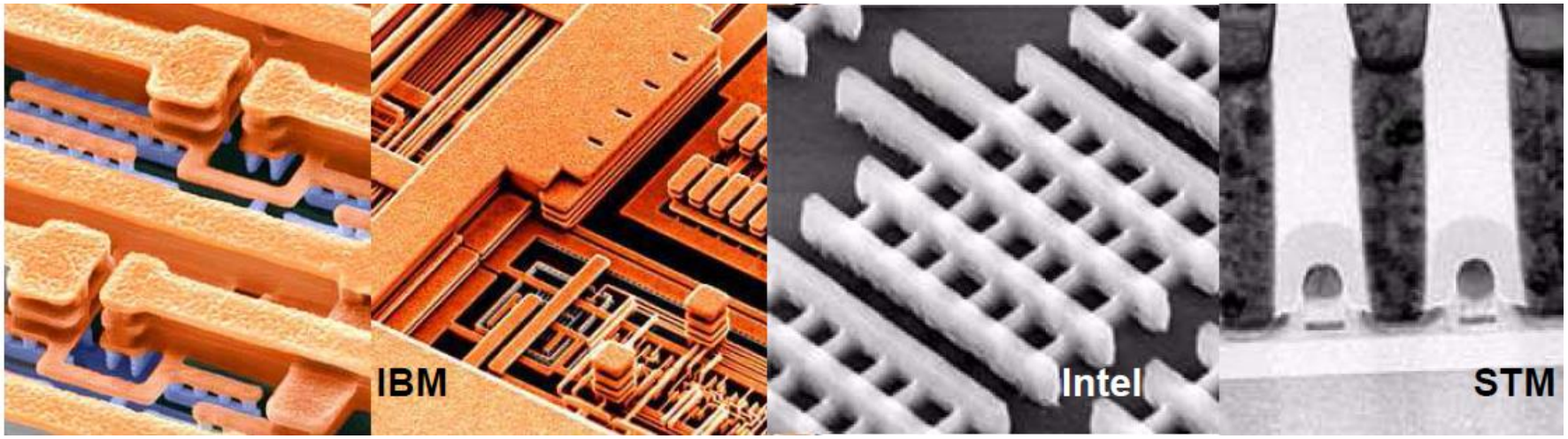


The Power Dissipation Problem



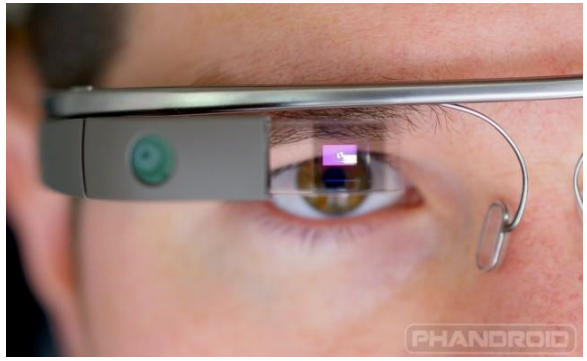
- Power consumption α $Cf_{clk}VDD^2$. Heat dissipation is limiting the complexity of SoCs.

Future Silicon Technology Generations

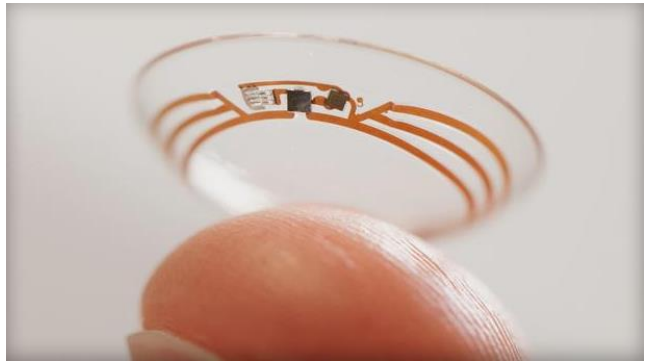


- CMOS/BiCMOS offers outstanding performance: fJ/gate, < 10 ps gate delay, > 10^9 working devices/chip. A new device which outperforms the MOSFET is proving difficult and costly to develop.
- CMOS is ***not*** a mature technology. It continues to drive the exponential growth of electronics and many applications. Scaling of CMOS to its limits will proceed for the forseeable future.
- The electrical behavior of scaled CMOS devices is different with each new generation (i.e., every 18-24 months).
- Analog/mixed-signal/RF circuits must be developed which are: 1) scalable, 2) capable of sub-1V operation, and 3) robust to PVT variations.

Recent Innovation Examples



Glass



Glucose Sensor

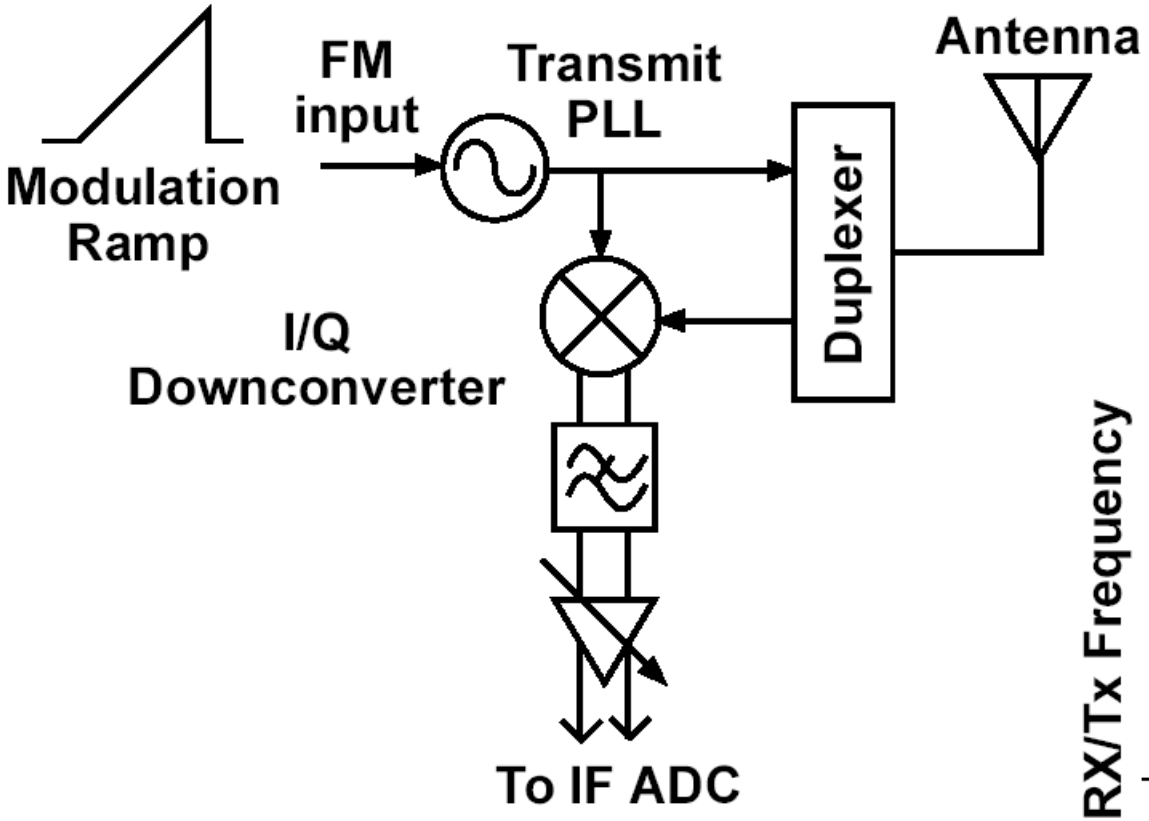
Self-Driving Car

- 3 of Googles' high-profile projects are sourced from on-going university research projects: wearable computing; Brian Otis (U Washington) autonomous sensors; Sebastian Thrun (Stanford) artificial intelligence.
- Technological innovation in IC design is becoming rare within large corporations. Universities are often chaotic and inefficient, but now lead design innovation.

Reinventing the Automobile

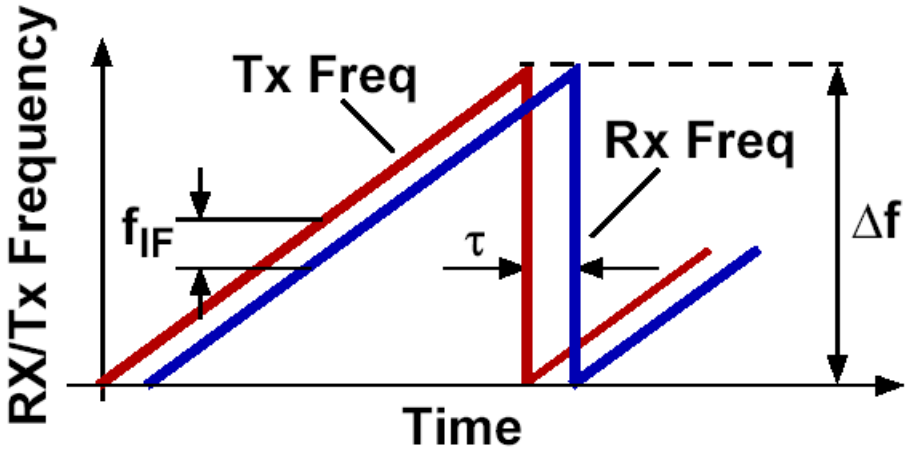
- Only ~5% of a highway's surface is covered by vehicles.
- From 2001-2009, American roads claimed 369,629 lives; "human errors" cause 93% of all crashes.

FM Continuous Wave Radar



$$\Delta R \geq \frac{c}{2\Delta f}$$

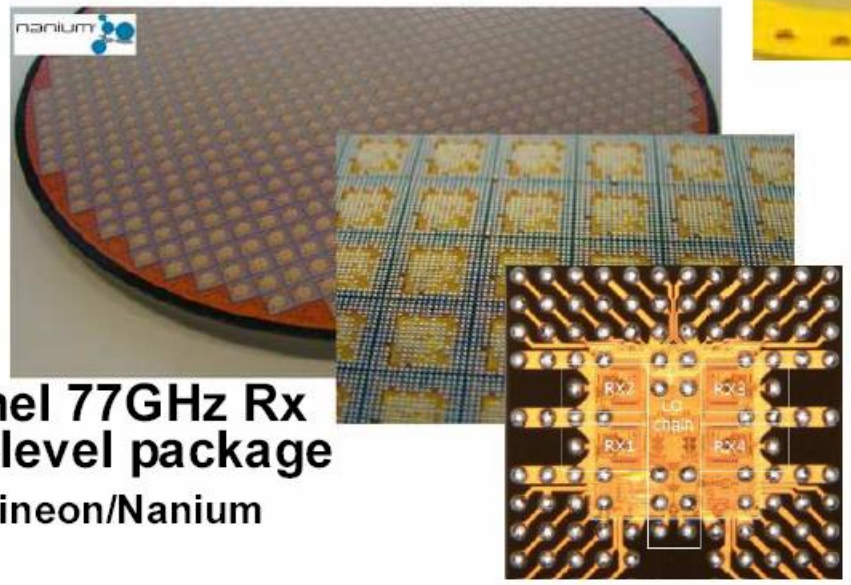
ΔR = range resolution



- Range is determined by round trip propagation time; relative speed is measured via Doppler frequency shift. Applied in automotive collision avoidance radar.
- Higher frequency radio waves give finer resolution images (e.g., for health, security, and quality control applications).

Commercial Example: 77GHz FMCW Radar

- Tx and Rx circuits integrated into a four-channel SiGe chip
- 4 microstrip patch antennas angled at 45° to reduce interference for on-coming vehicles
- Lens in module focuses antenna beams
- 2-Tx/4-Rx chip P_D ~ 3.3W at 5.5V; -40° to > 85°C operating range



4-channel 77GHz Rx in wafer-level package

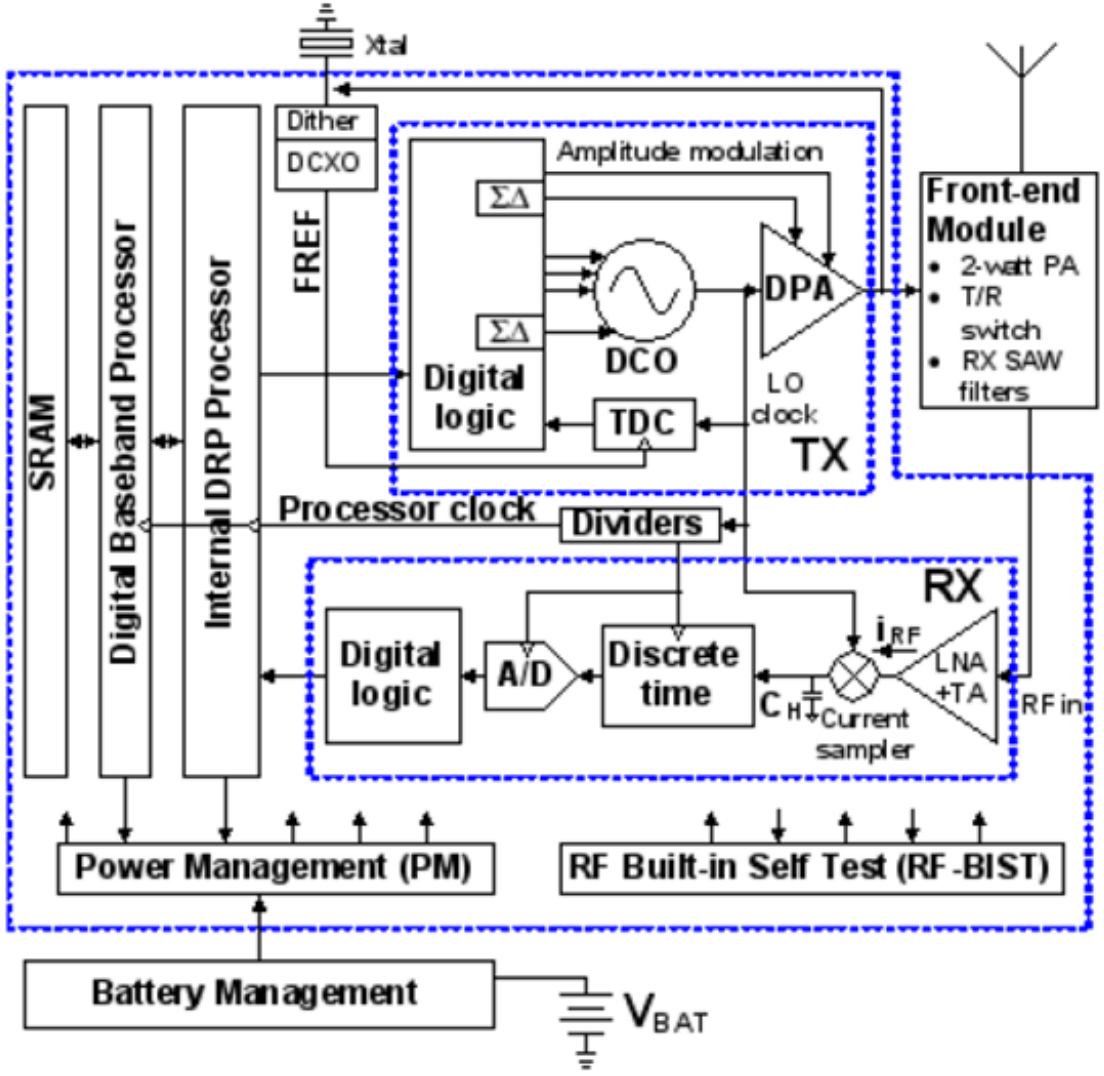
Infineon/Nanium

Digital Helping Analog

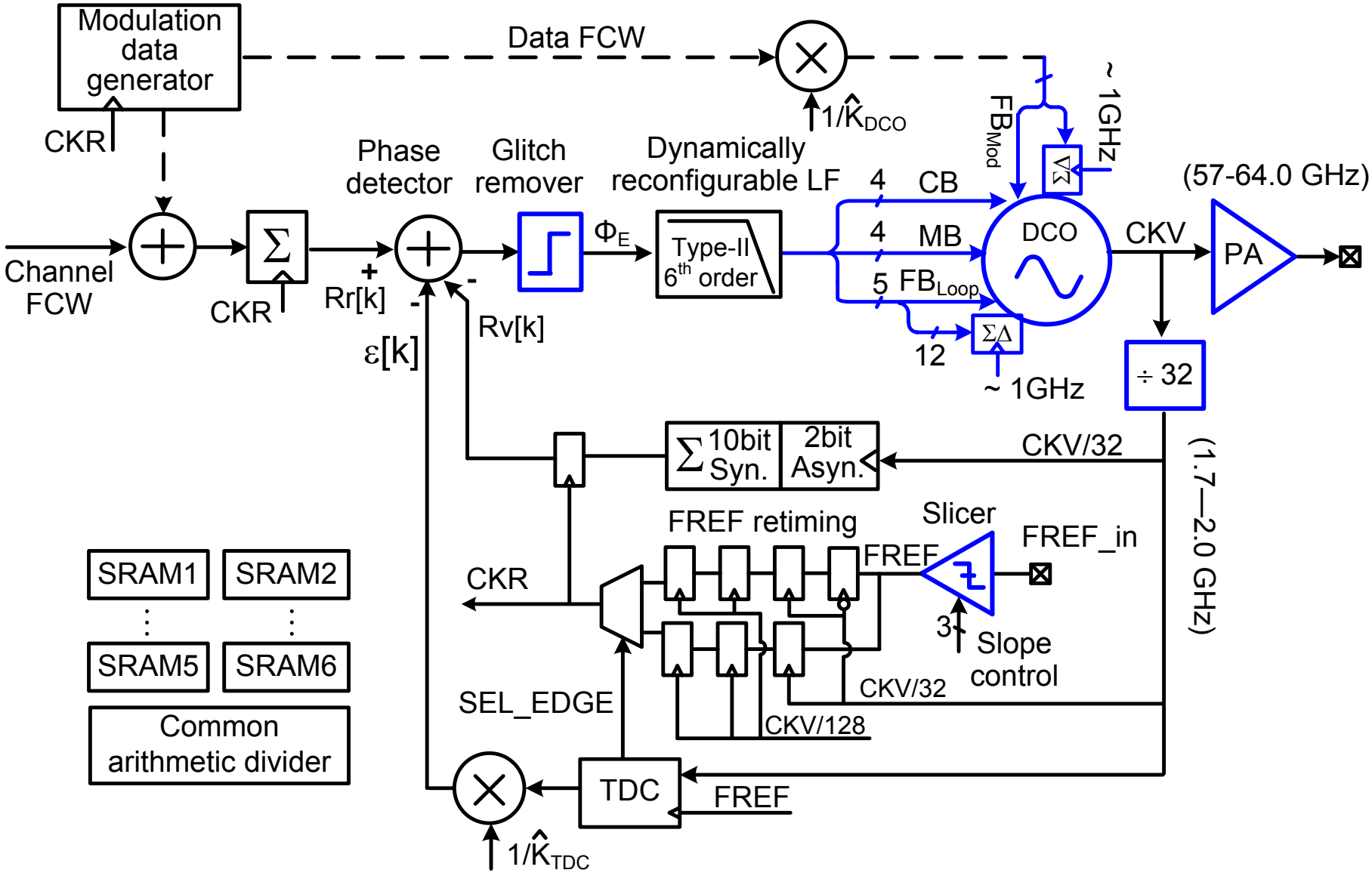
- Digitally–assisted RF circuits trade-off analog quality/precision for digital complexity:
  - on-chip calibration
  - built-in self-test
  - predistortion and post-processing
  - digital equivalents for analog functions
- Improves the portability and re-use of RF circuits between technology nodes. Can identify and cope with impairments dynamically.
- Minimizes analog signal conditioning and A/D converter resolution by adding digital pre- and postprocessing to compensate for loss in performance.

Digital-RF Transceiver (TI)

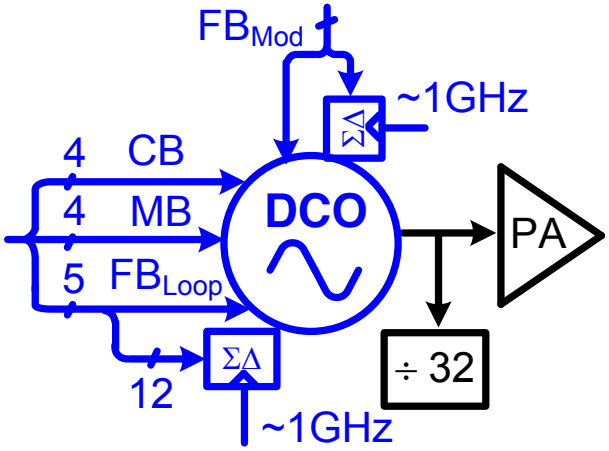
- Mainly-digital implementations of RF circuits are amenable to scaling; use digital flow.
- Digital polar tx; all-digital PLL and sampled-RF receive chain.
- Factory and power-up auto calibrations and per-burst calibrations.
- RF built-in self-test.
- Lower power consumption, chip area and cost.



60GHz ADPLL Block Diagram



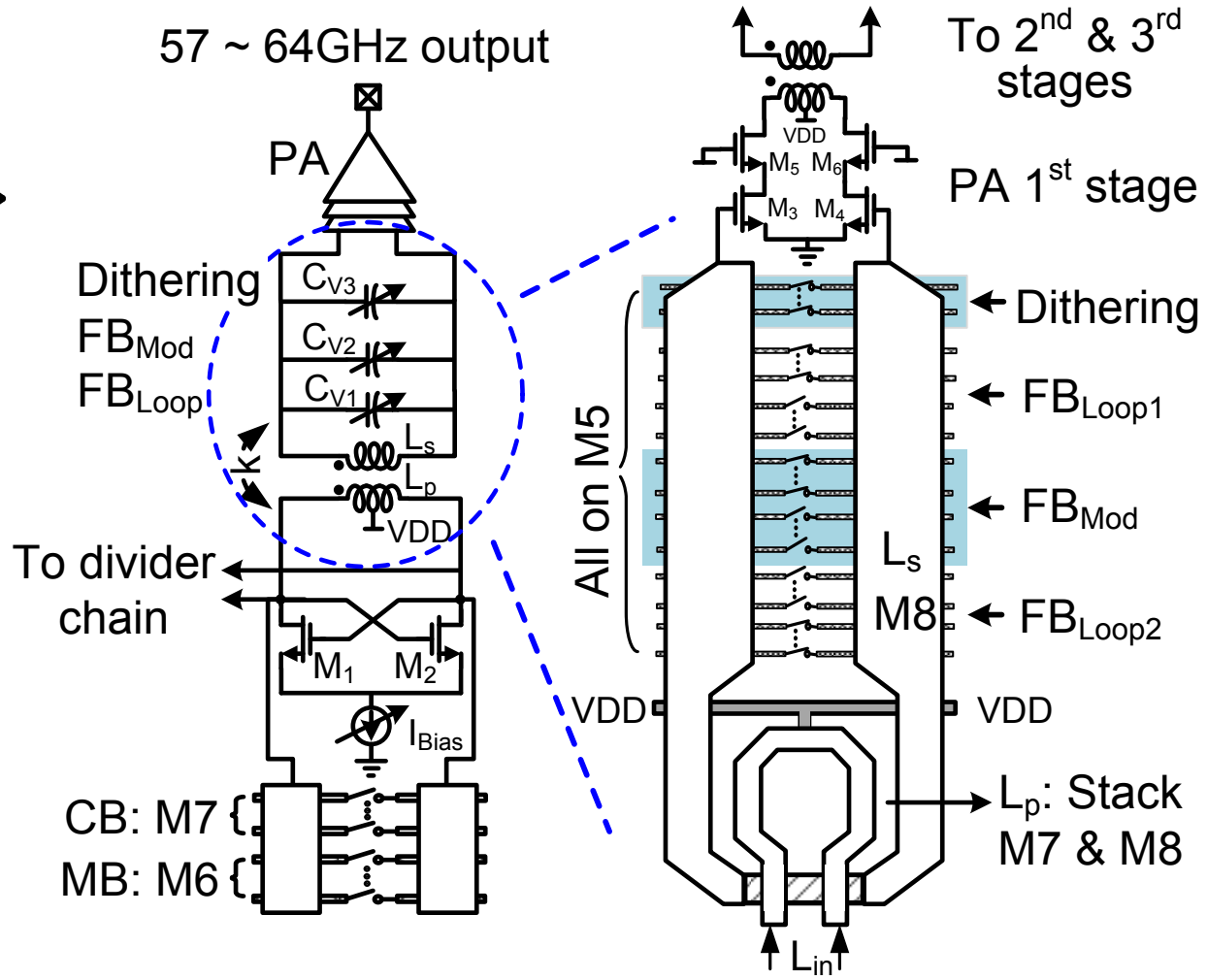
60GHz Digitally-Controlled Oscillator



k_{DCO} (MHz/bit)

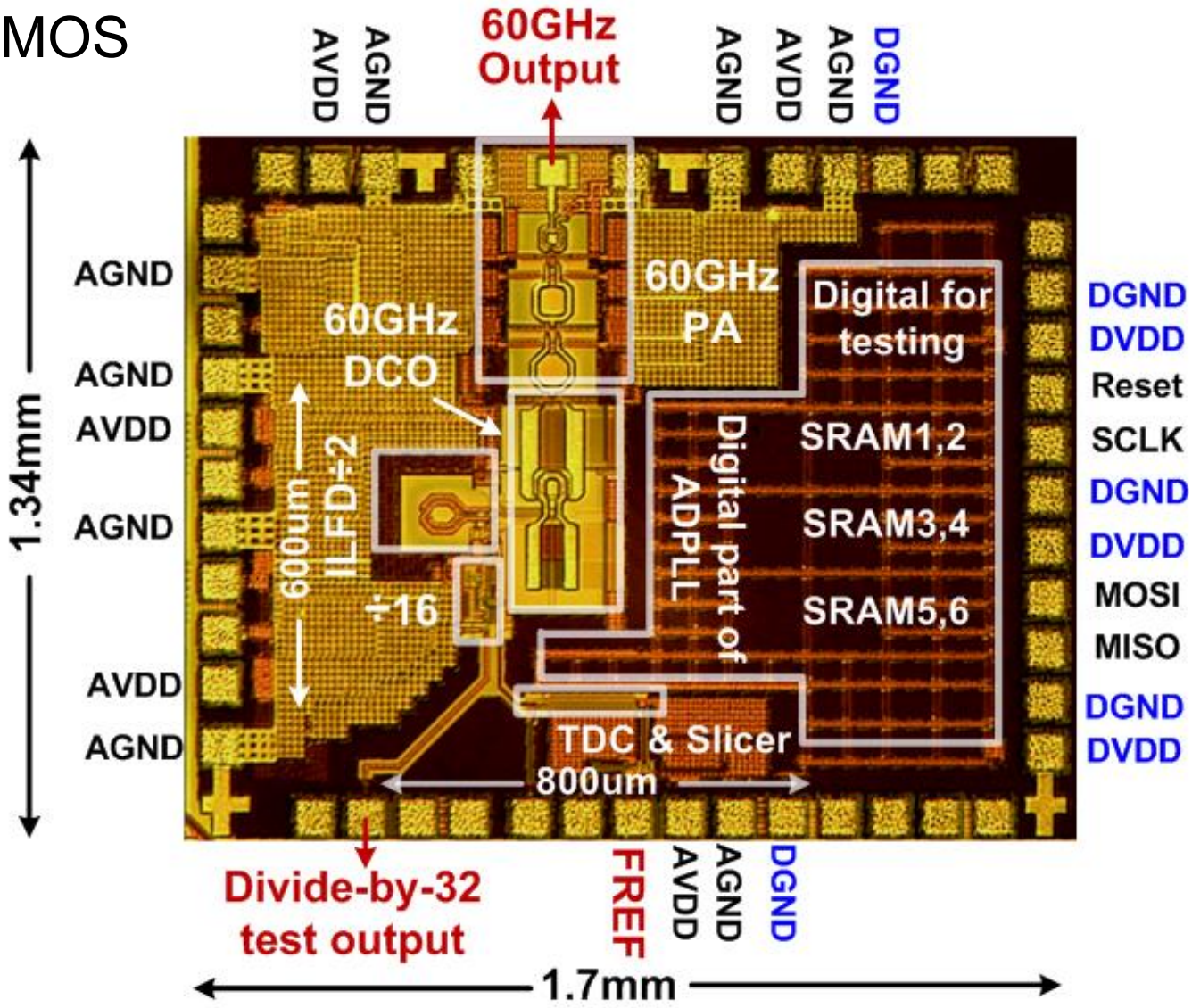
CB	367
MB	35
FB_{Loop}	1.75
FB_{Mod}	1.64

$\Delta\Sigma \rightarrow f_{res}$ = 400Hz

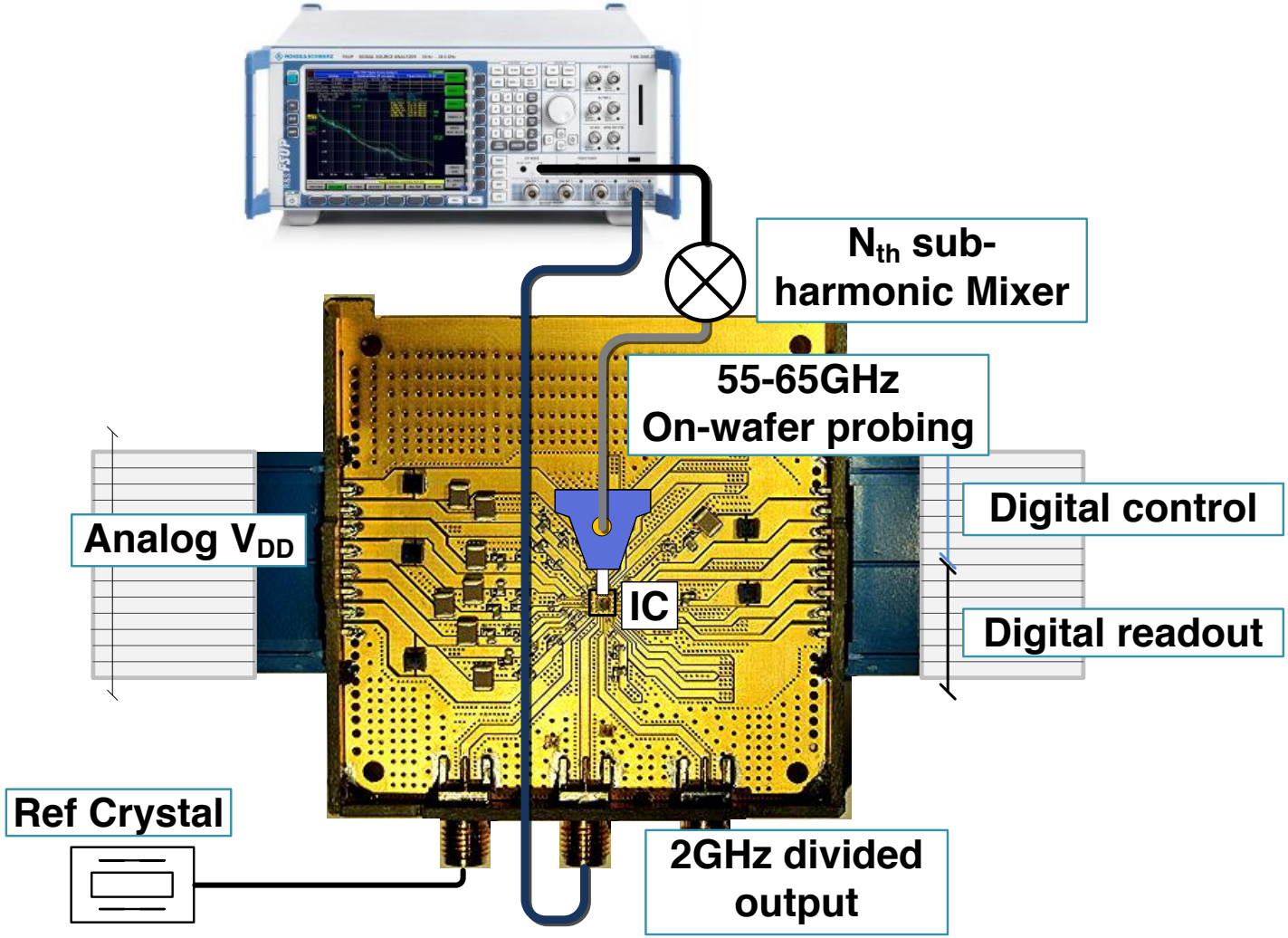


60GHz ADPLL Chip Micrograph

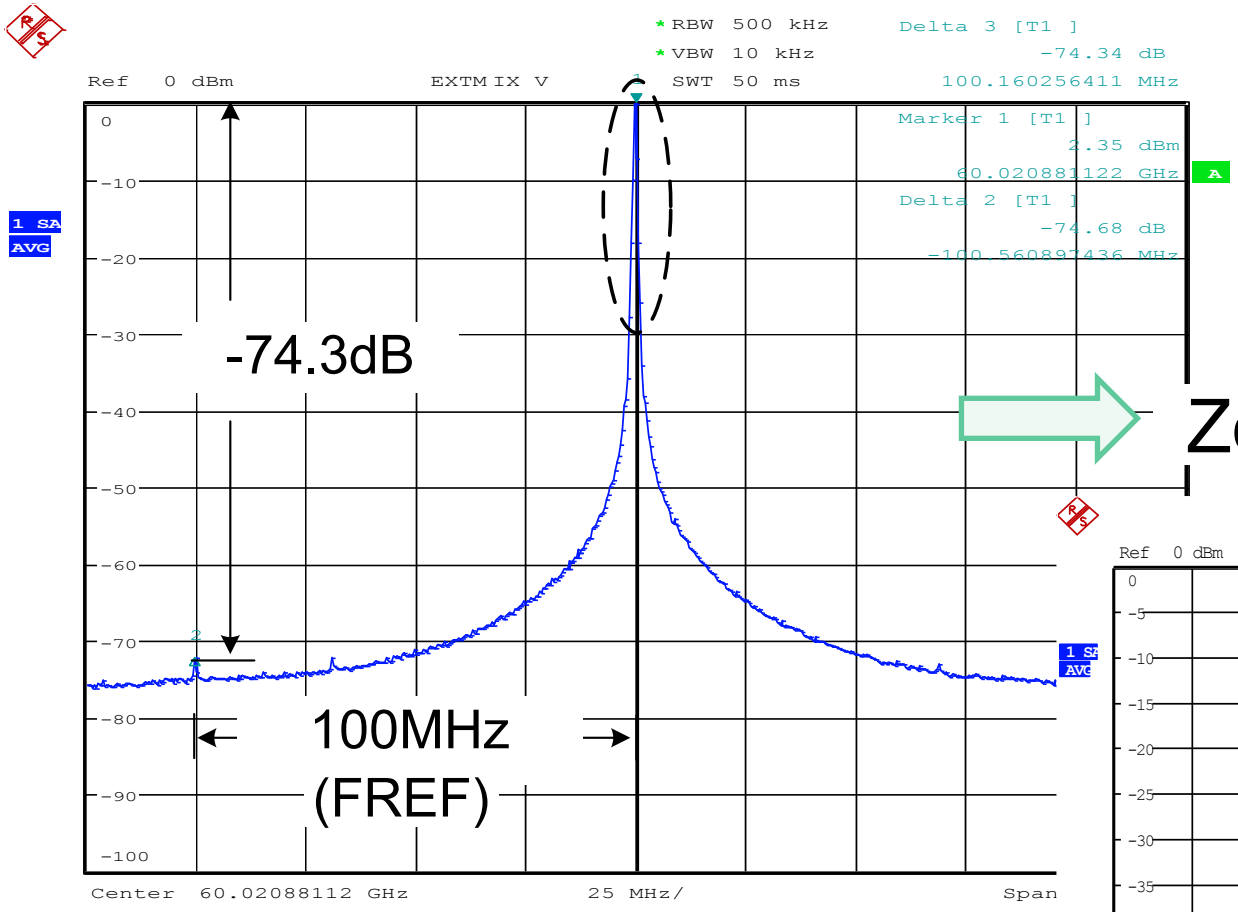
65nm CMOS



60GHz ADPLL Testing

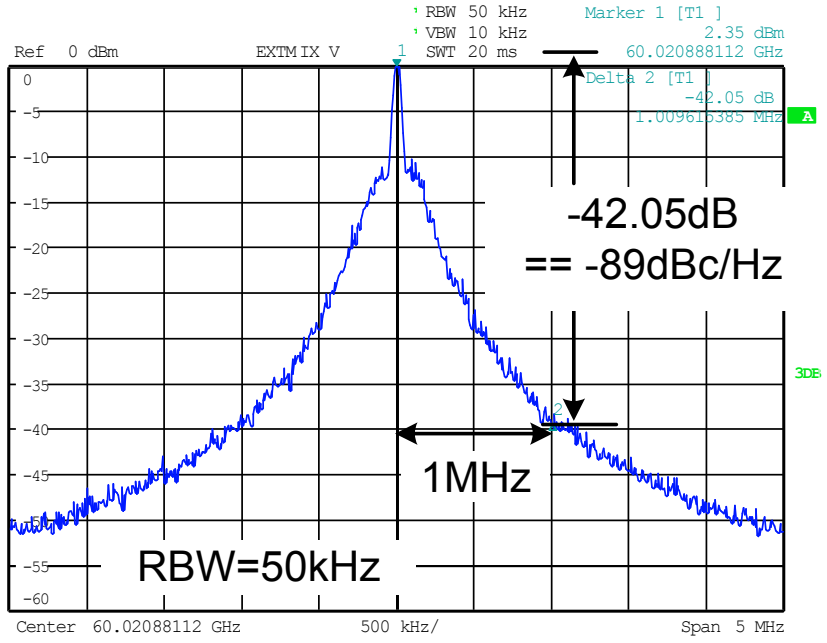


Measured Frequency Spectrum



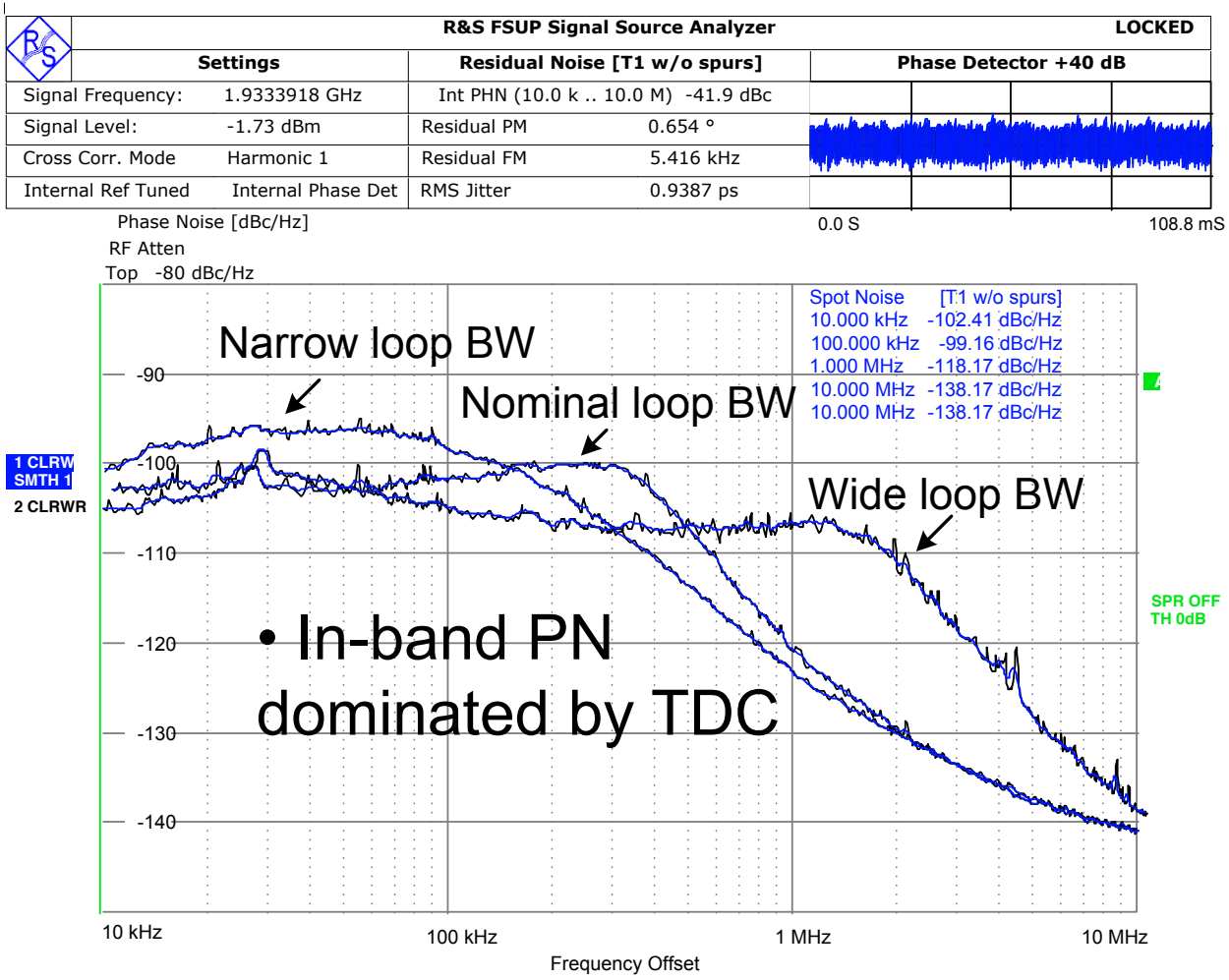
- f_{out} = 60.0209GHz
- PN = -89 dBc/Hz @1MHz offset

Zoom in



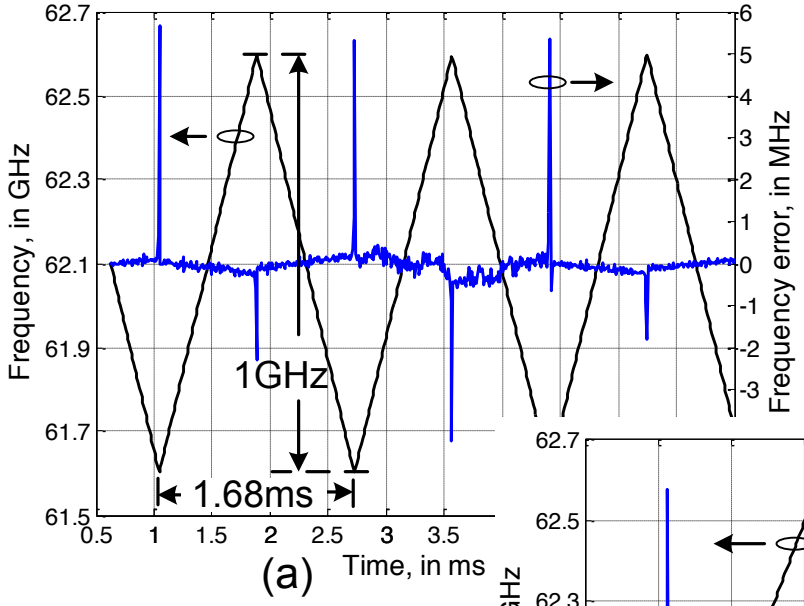
- FREF = 100MHz
- Reference spur = -74.3dBc

Measured Phase Noise



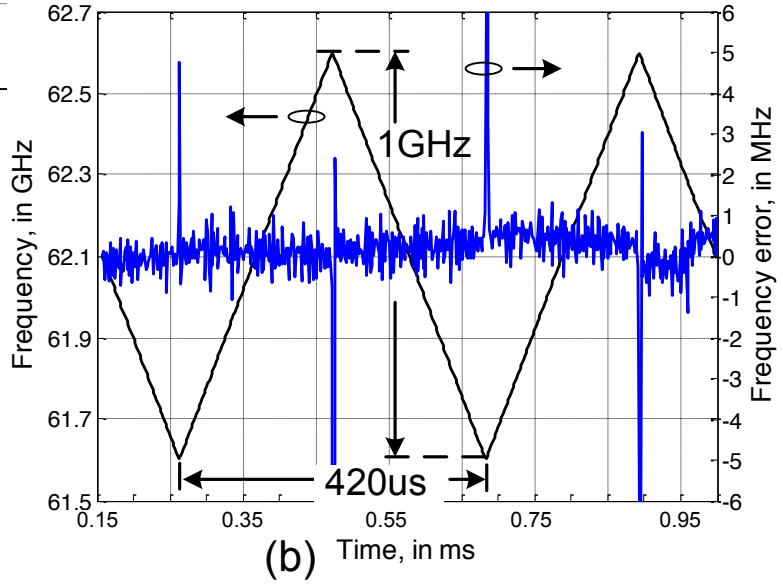
- TDC resolution 12ps, f_{ref}=100MHz → in-band PN=107dBc/Hz.

FMCW ADPLL Synthesizer Performance



Summary

BW	T_{mod}	Freq. error
1.22GHz	8.2ms	117kHz$_{rms}$
1GHz	1.68ms	180kHz$_{rms}$
1GHz	0.42ms	384kHz$_{rms}$

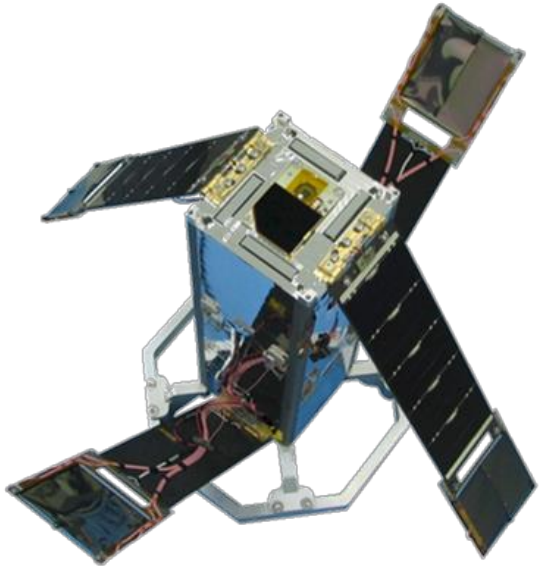


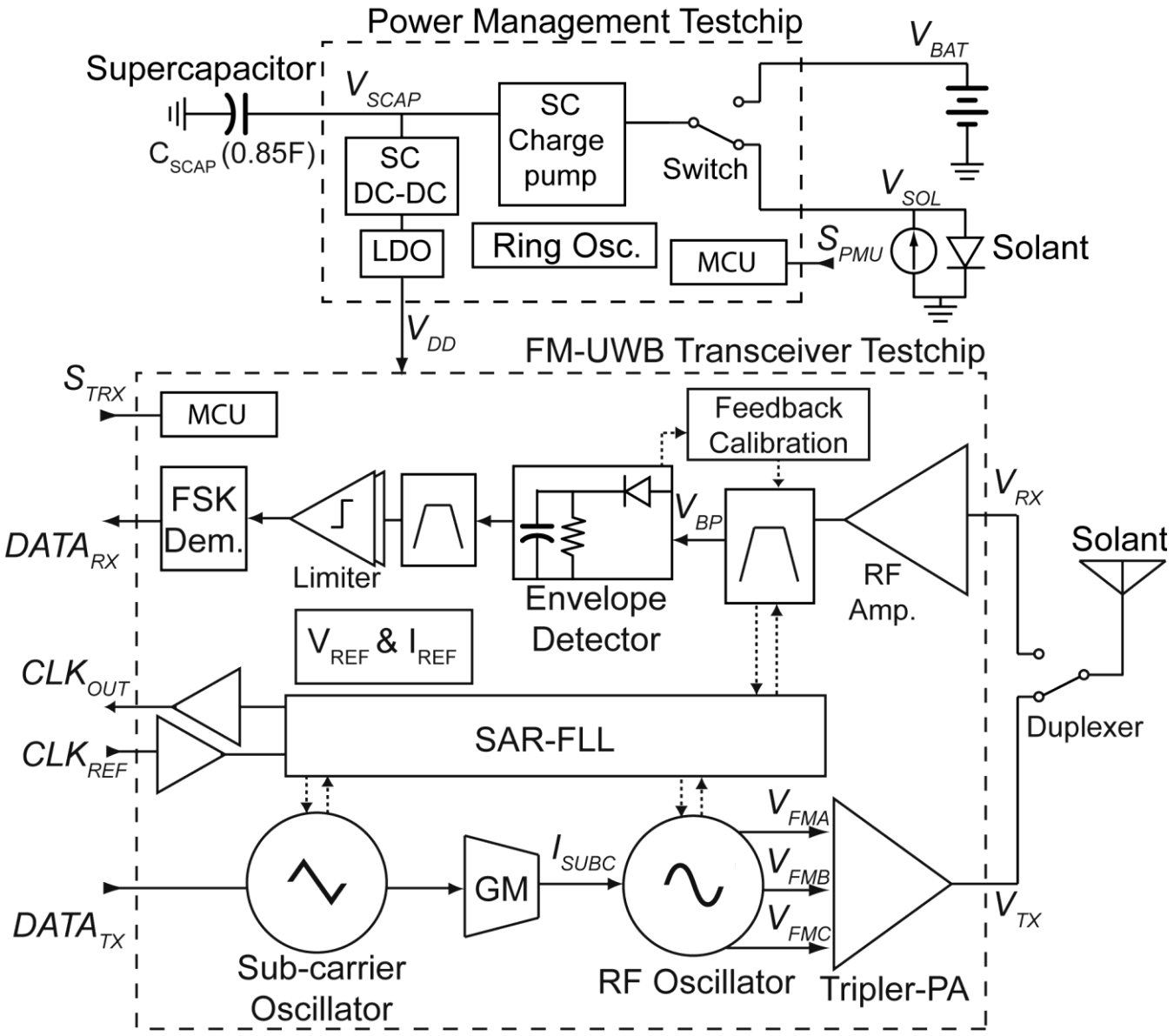
FMCW Synthesizer Comparison

	This Work	ISSCC'11 [6]	JSSC'10 [4]	ISSCC'10 [5]
Architecture	ADPLL + multi-rate 2-point mod.	Mixed-mode	DDFS+PLL	Fractional-N
Frequency (GHz)	56.4-63.4	82.1-83.8	78.1-78.8	75.6-76.3
CMOS	65nm	65nm	90nm	65nm
Reference	40MHz	26MHz	77MHz	700MHz
Modulation slope (k_m)	Fast:1GHz/ 0.21ms Slow:1.22GHz/ 4.1ms	Fast:1.5GHz/ 1ms Slow: 0.5GHz/ 5ms	700MHz/ 0.22ms	500MHz/ 0.5ms
Frequency error (r.m.s)	Fast: 384kHz Slow:117kHz*	Fast: 179kHz Slow:170kHz	1.05MHz*	<300kHz*
PN @ 1MHz	-90dBc/Hz	-84dBc/Hz	-85dBc/Hz	-84.6dBc/Hz
Supply	1.2V	1.2V	1.2V	1.2V
P_{DC} (mW)	48+41 (PA)	152 with buffer	101+305(TX)	73+115(PA)
Output power (50Ω)	+5dBm	NA	-2.8dBm	+10.5dBm

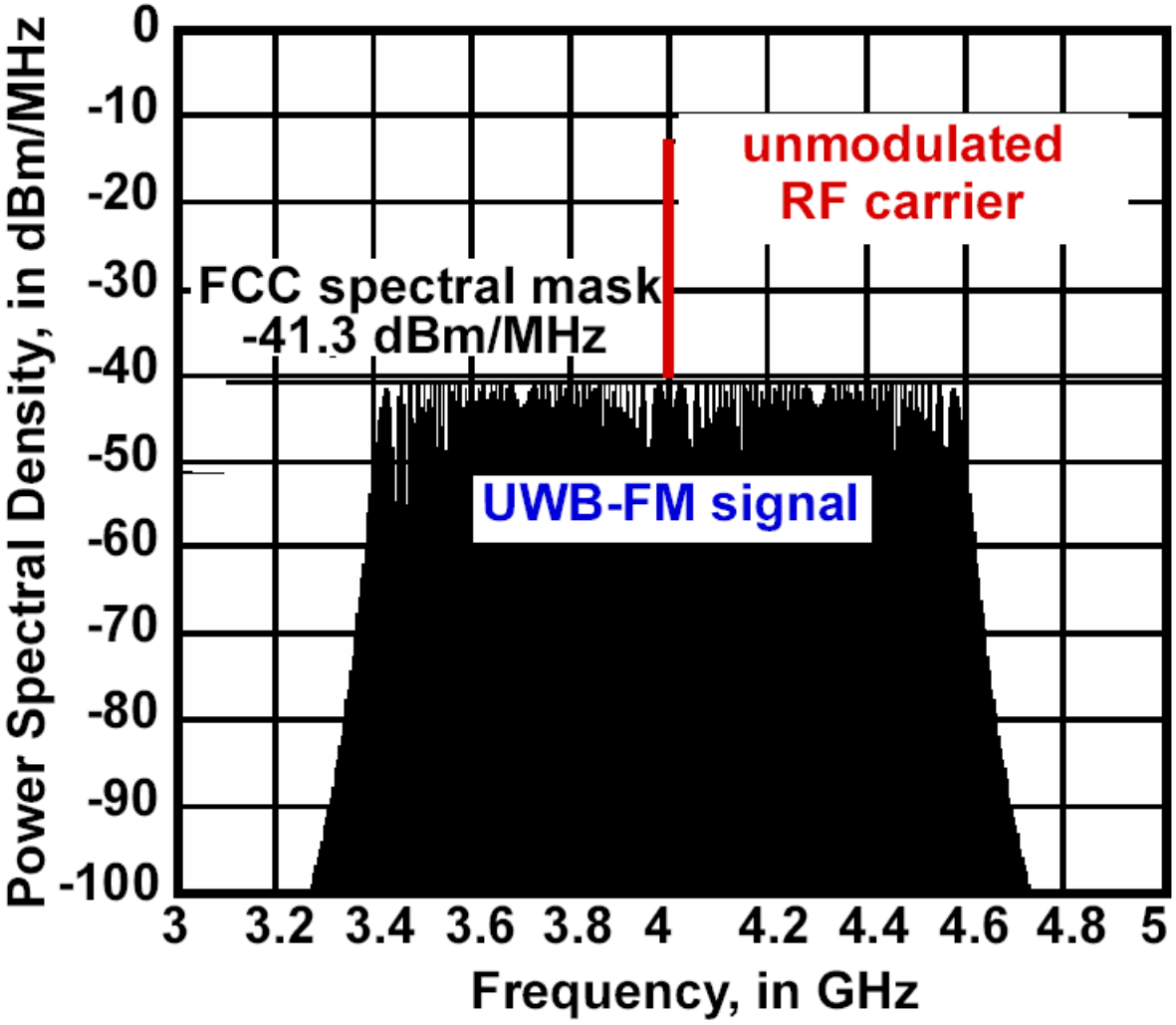
* Includes turn around point

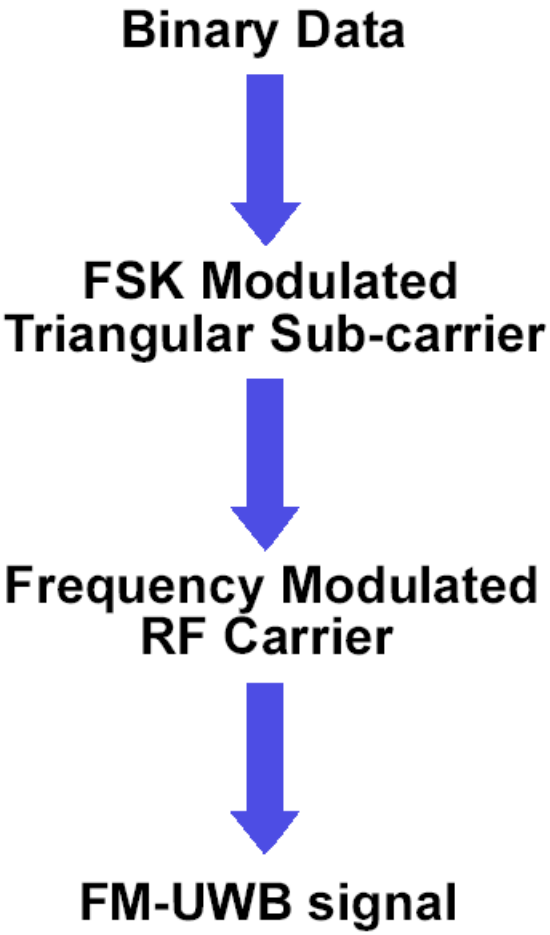
Autonomous Wireless Tx/Rx



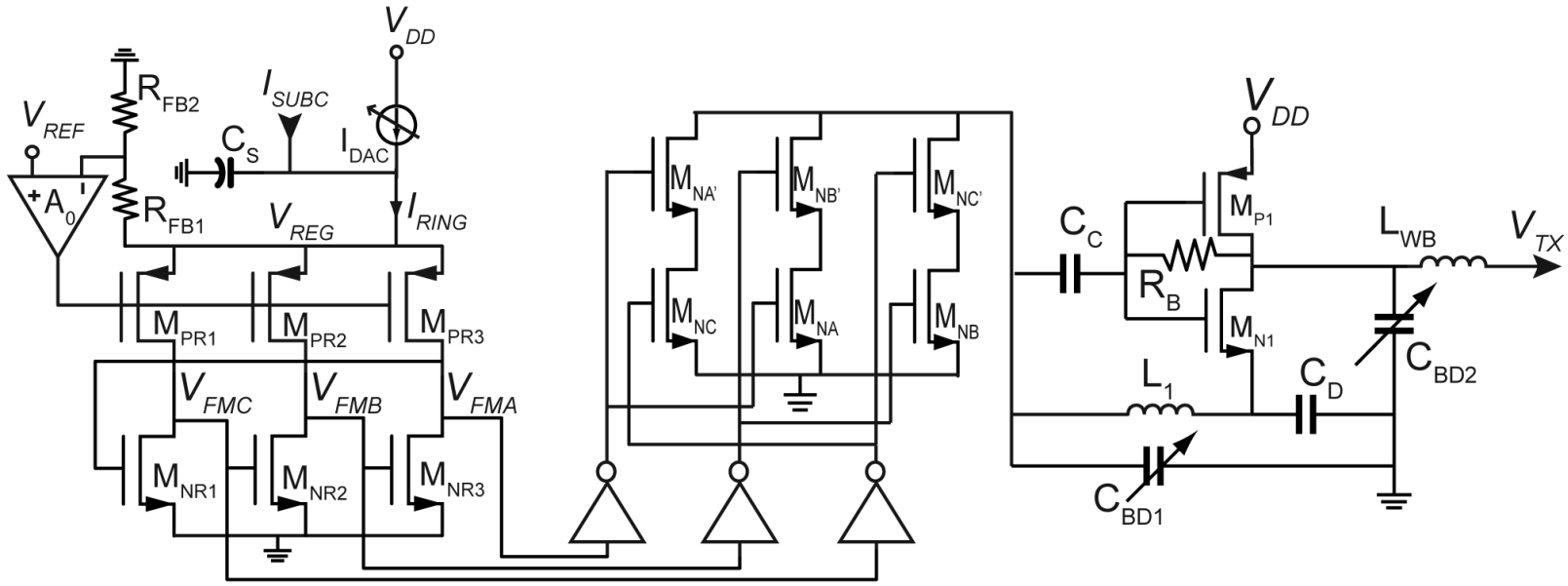


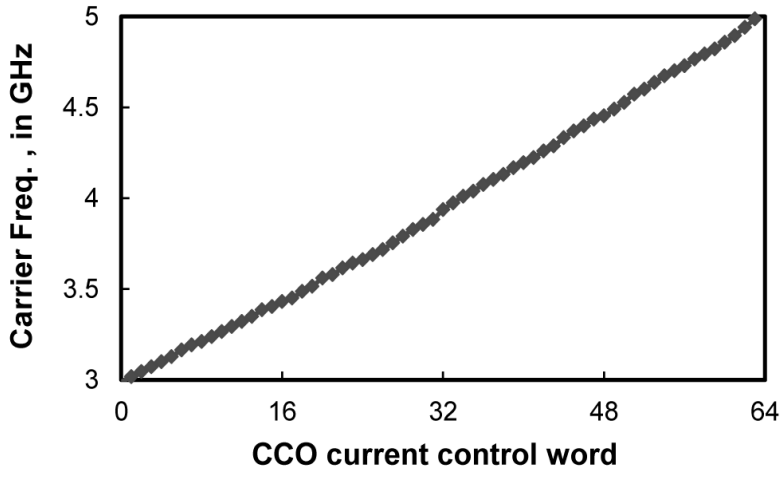
FM Ultrawideband (FM-UWB)

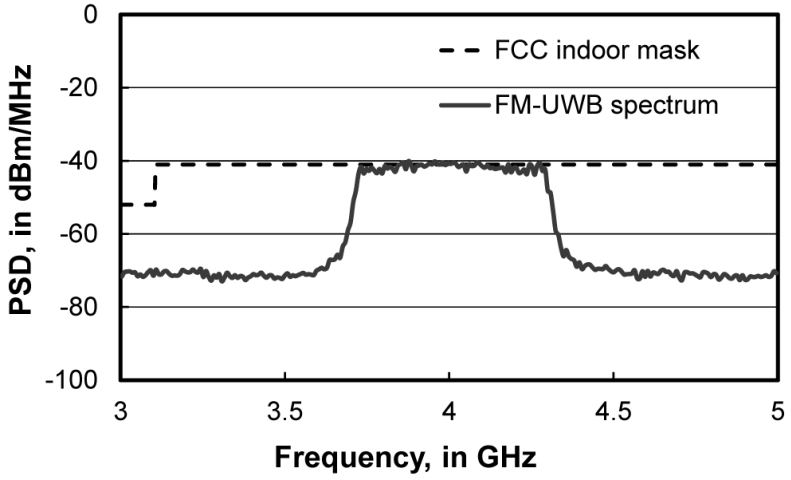




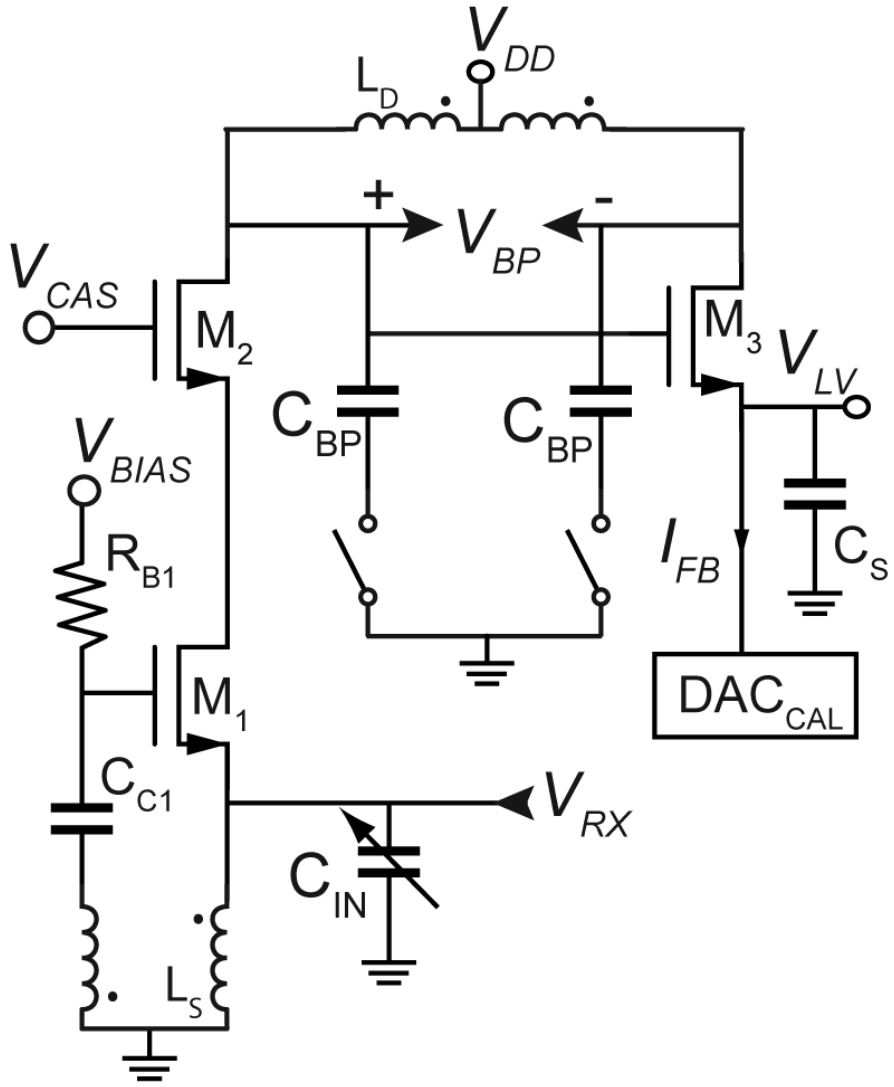
FM-UWB Transmitter

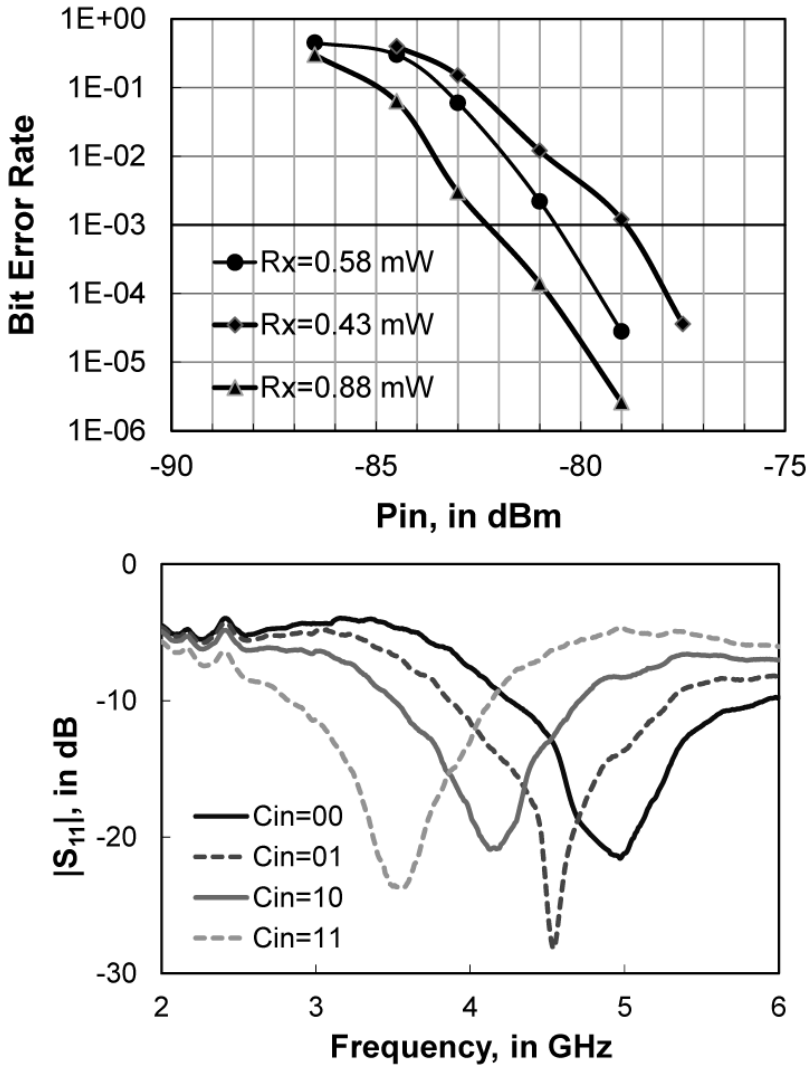




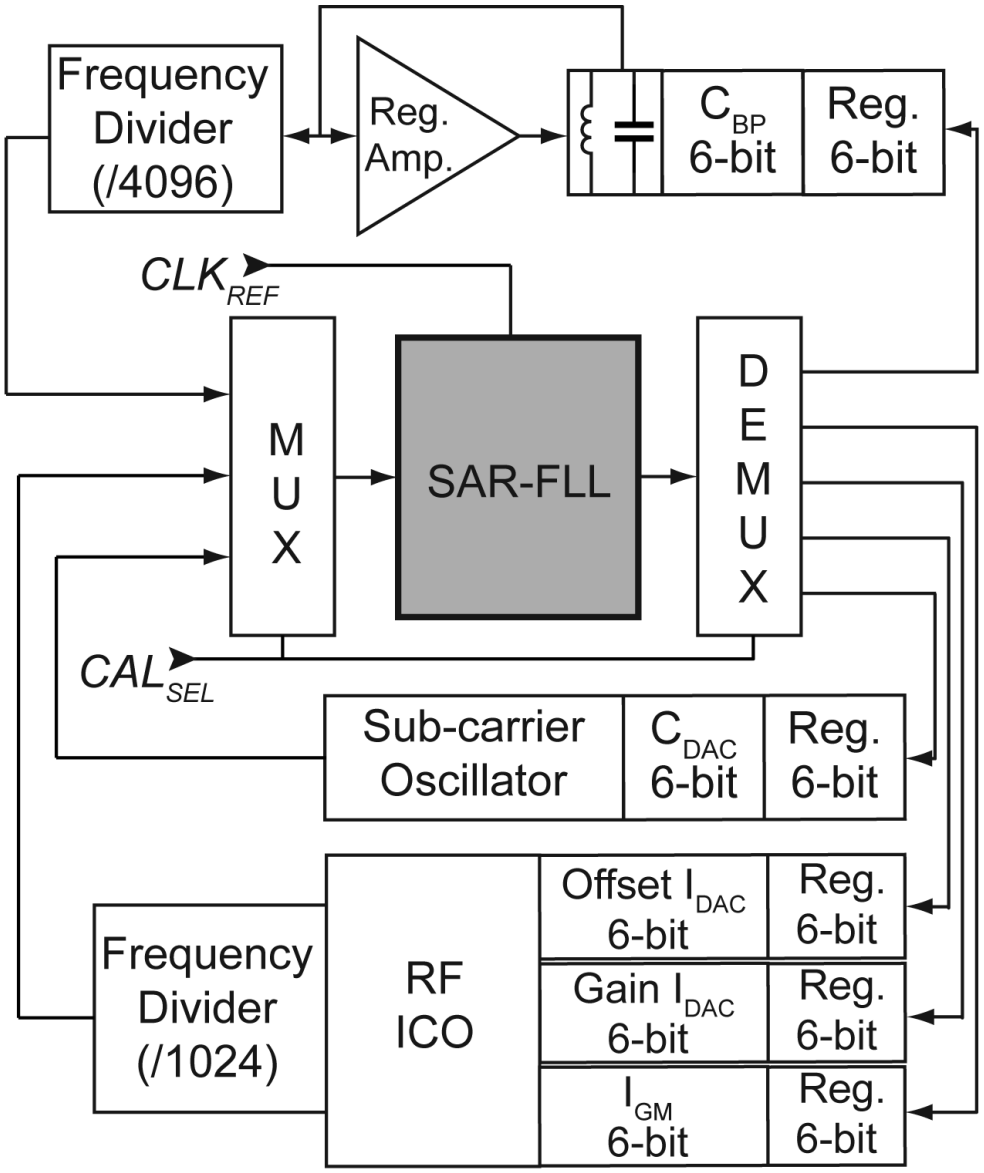


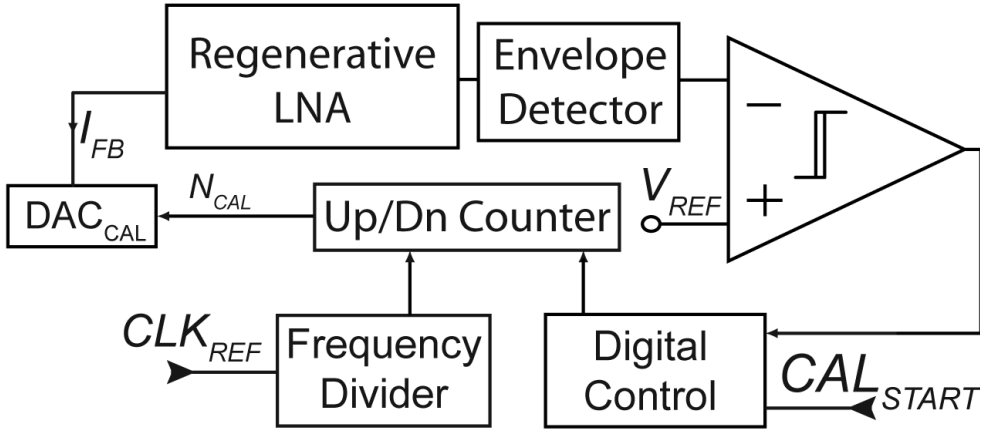
FM-UWB Receiver Front-End

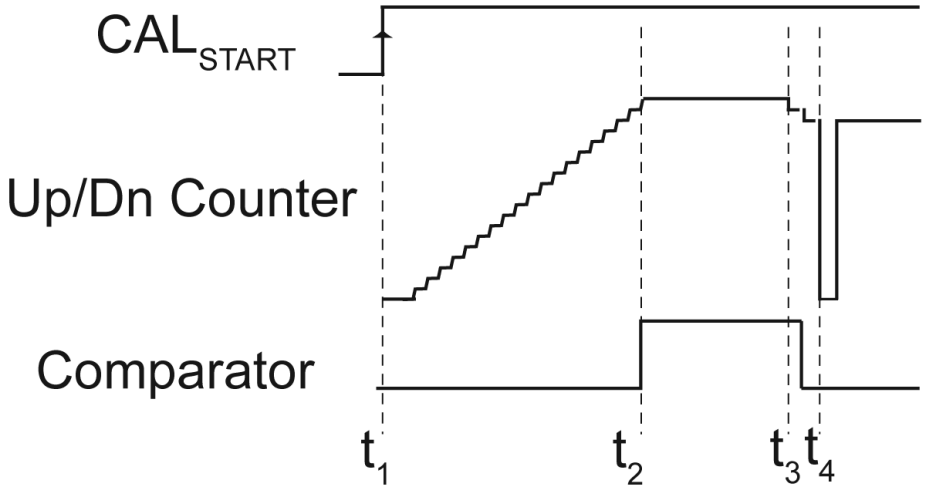




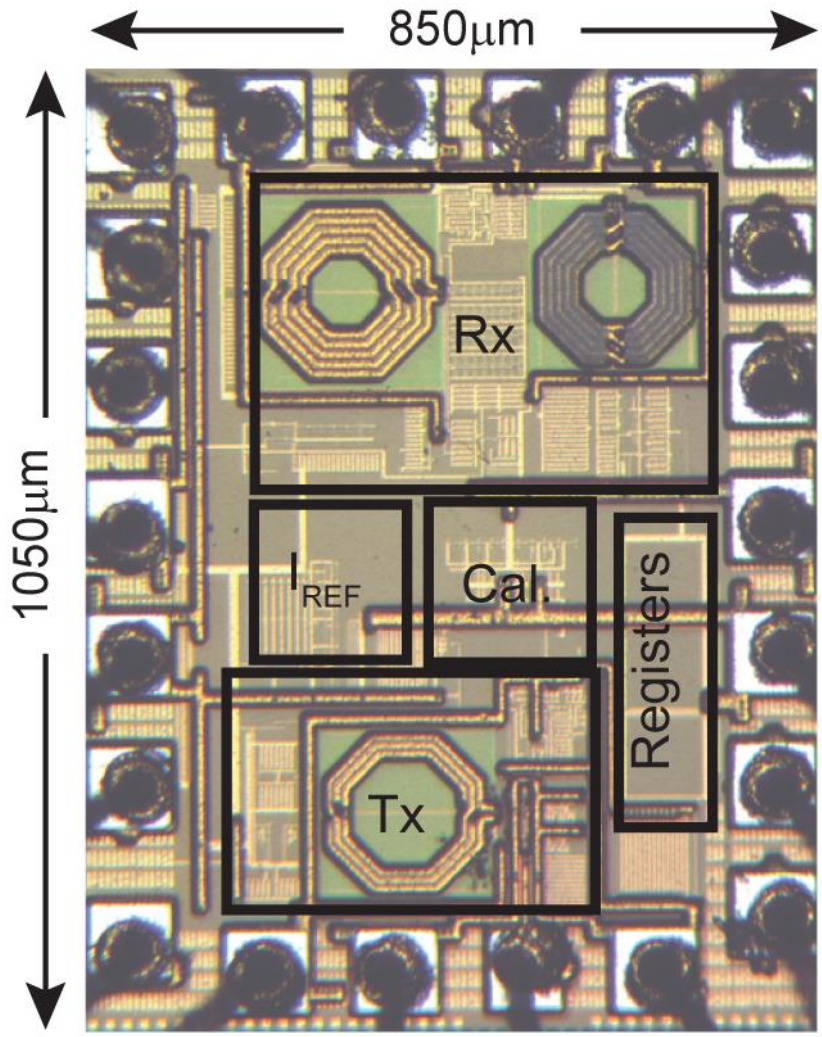
Full On-Board Calibration



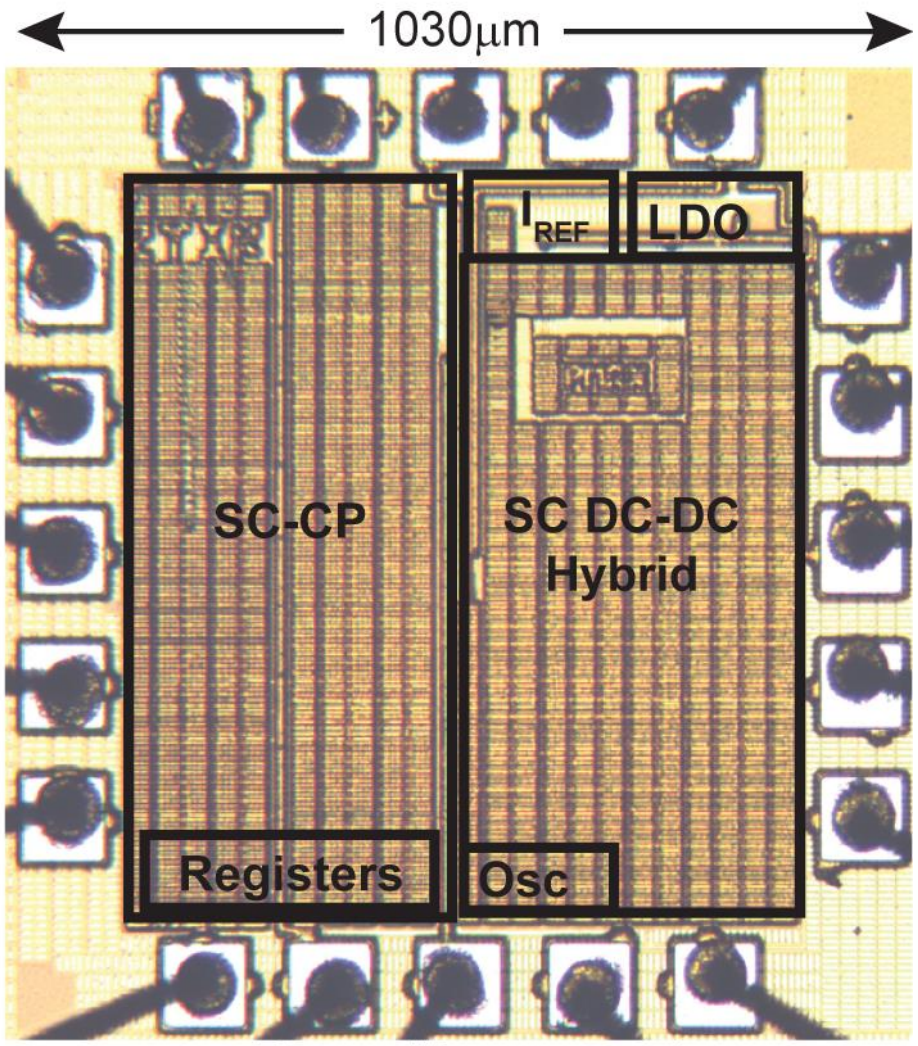




90nm CMOS Prototype ICs

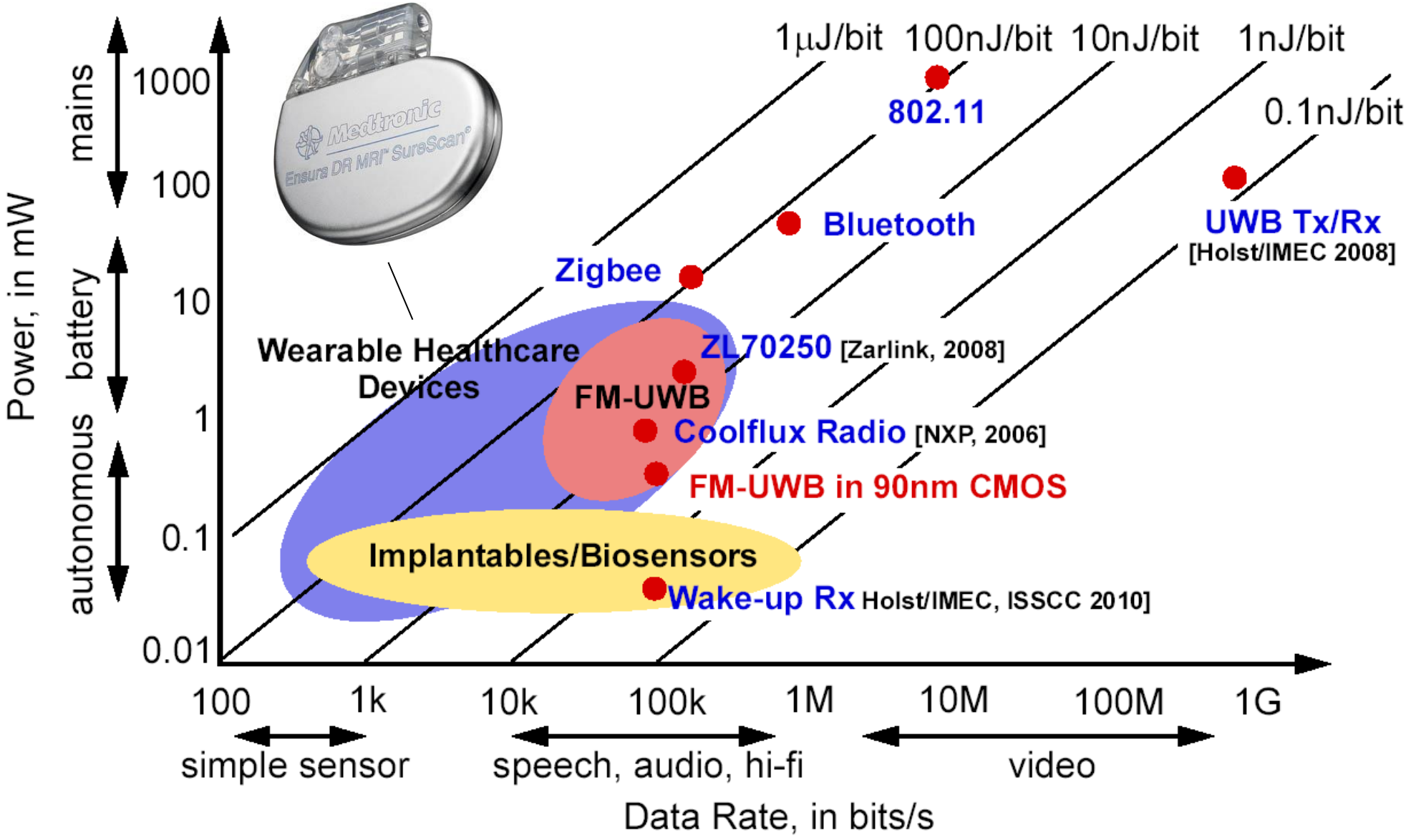


Transceiver

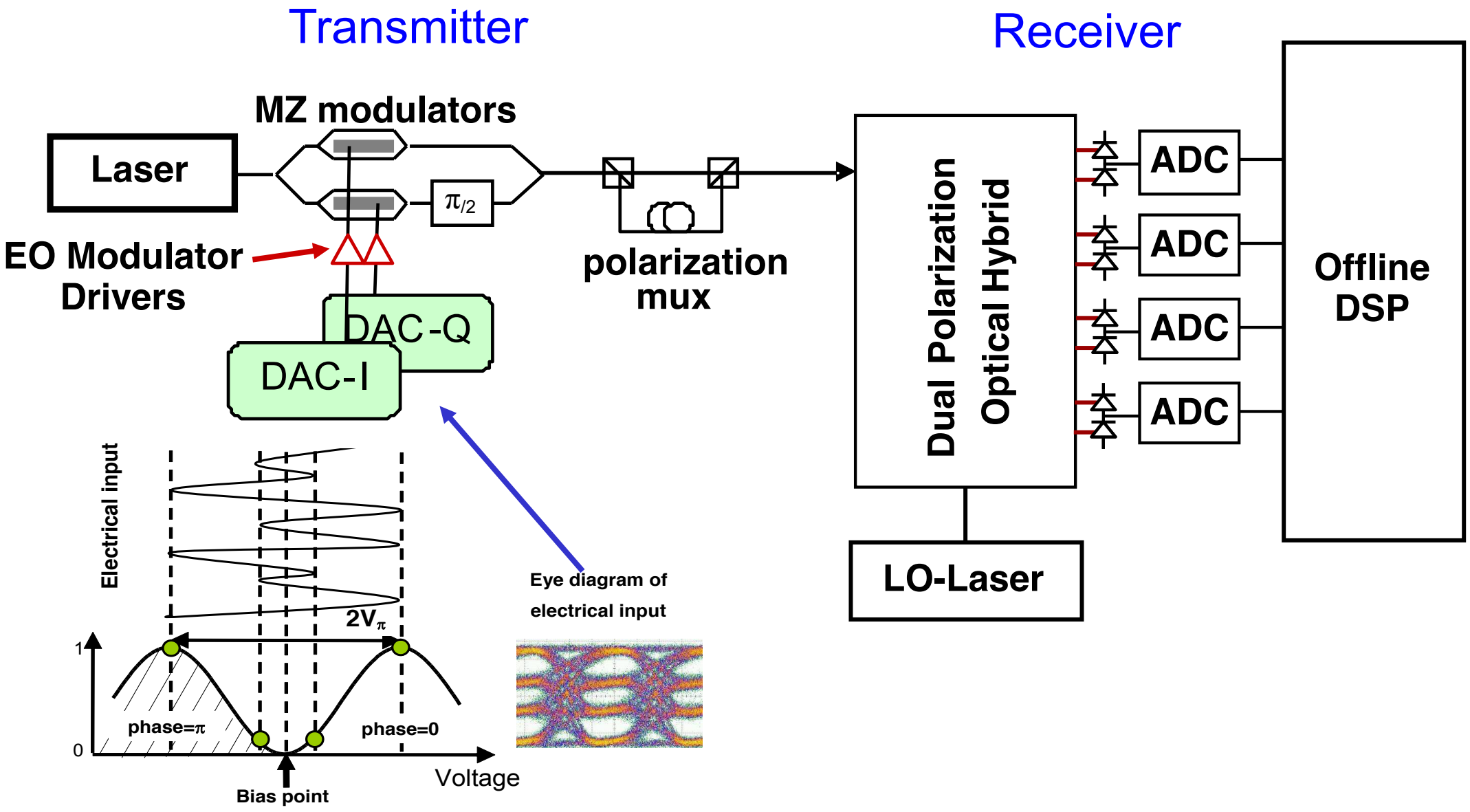


Power Management

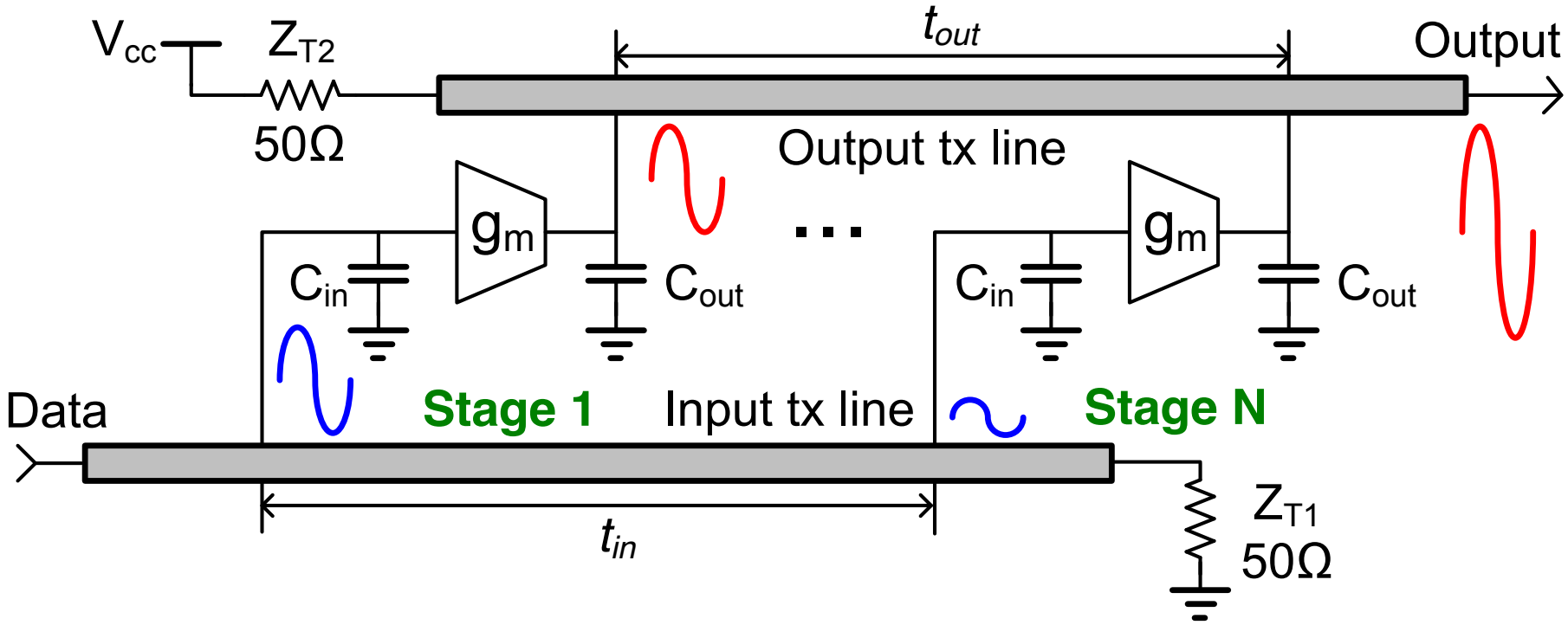
Low-Power Radio Technologies



400GE

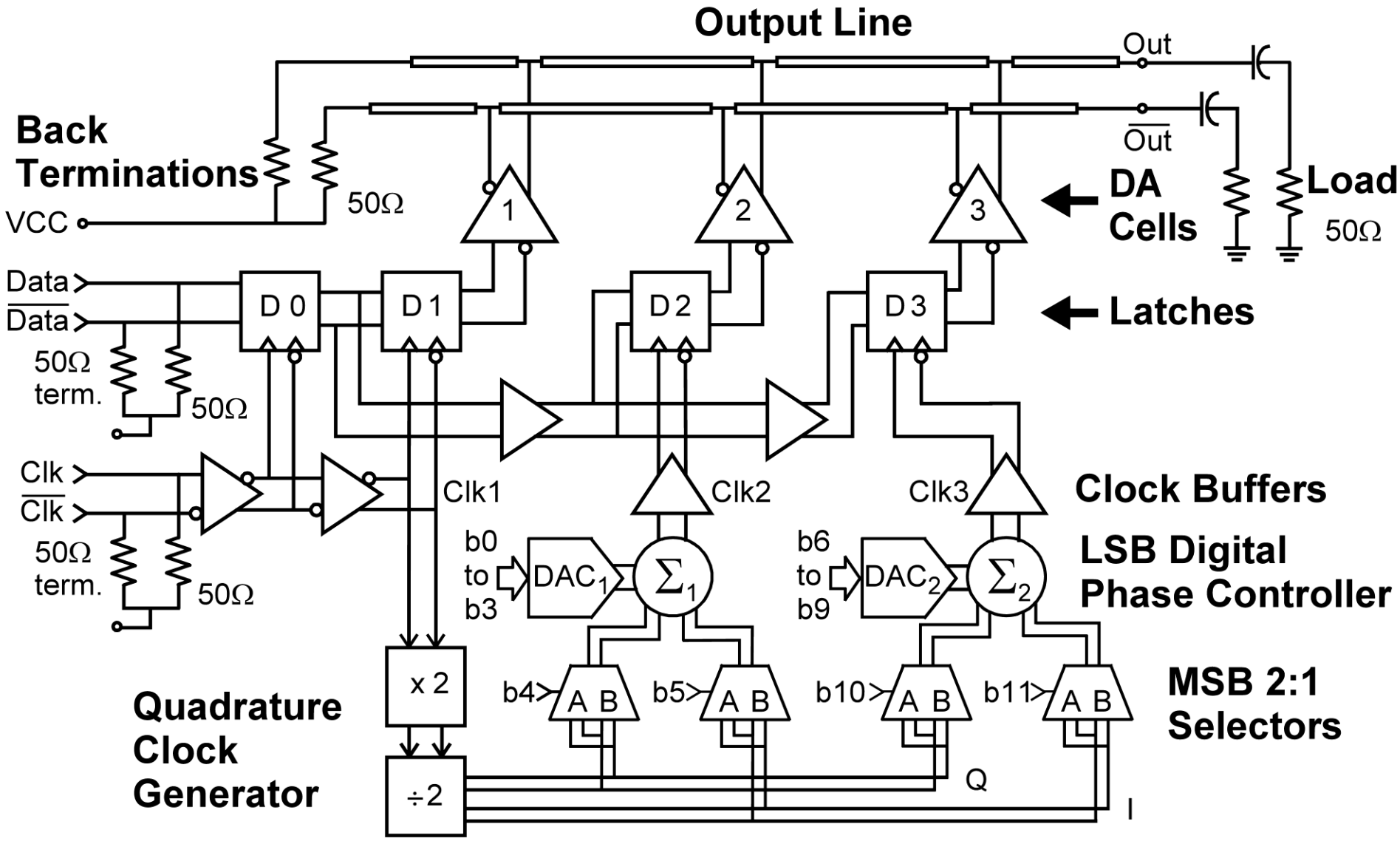

Transmitter
Receiver
MZ modulators
Laser
EO Modulator Drivers
π/2
polarization mux
DAC-Q
DAC-I
Dual Polarization Optical Hybrid
ADC
ADC
ADC
ADC
Offline DSP
LO-Laser
Electrical input
2Vπ
1
0
phase=π
phase=0
Bias point
Voltage
Eye diagram of electrical input

The Distributed Amplifier

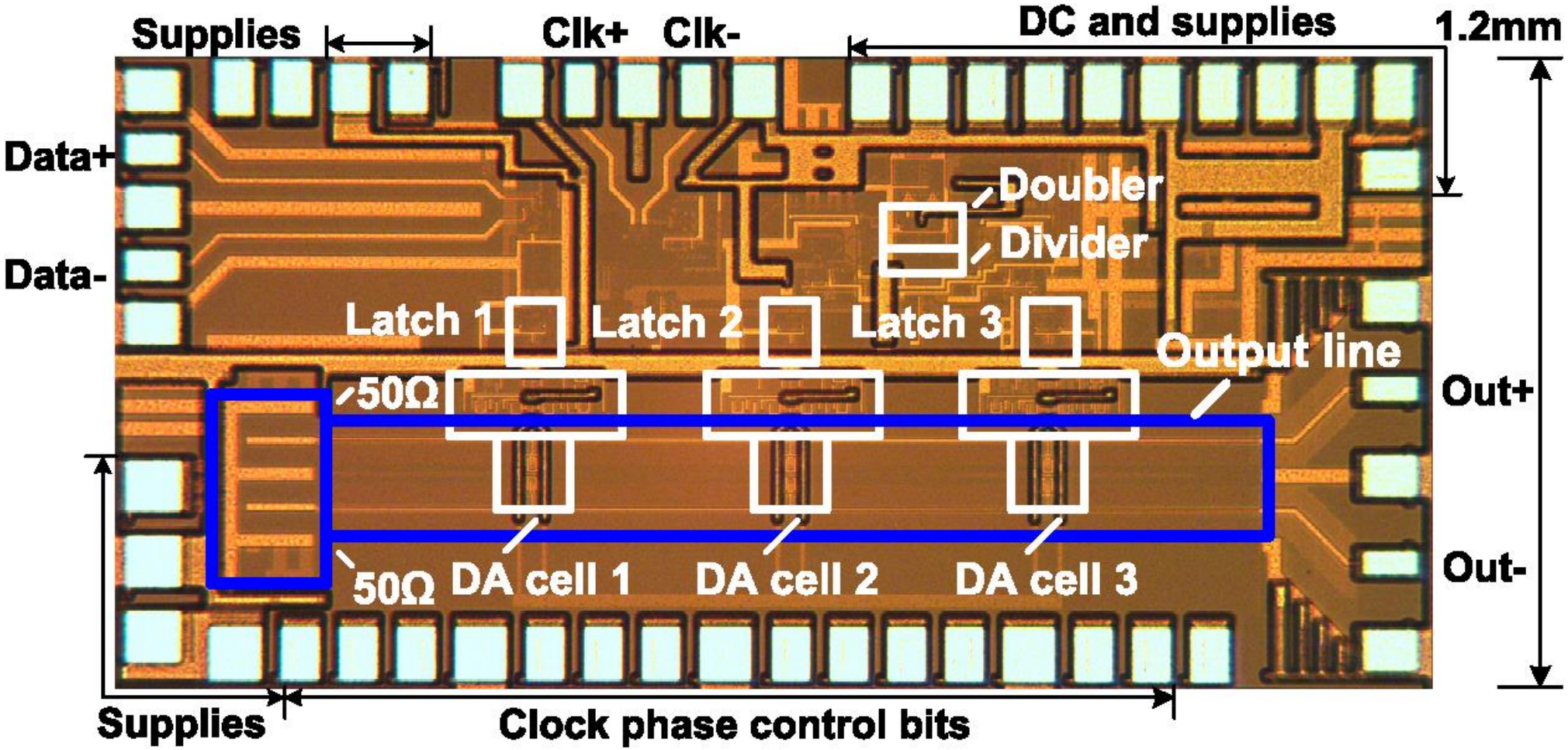


- Input line limits bandwidth when $C_{in} > C_{out}$ ($\omega_{max} = 2/\sqrt{LC}$). Attenuation of transmission lines limits maximum number of stages.
- Precise analog matching required (i.e., $t_{in} = t_{out}$).
- Reflections from Z_{T1} and Z_{T2} affect signal quality.

Digitally-Controlled DA

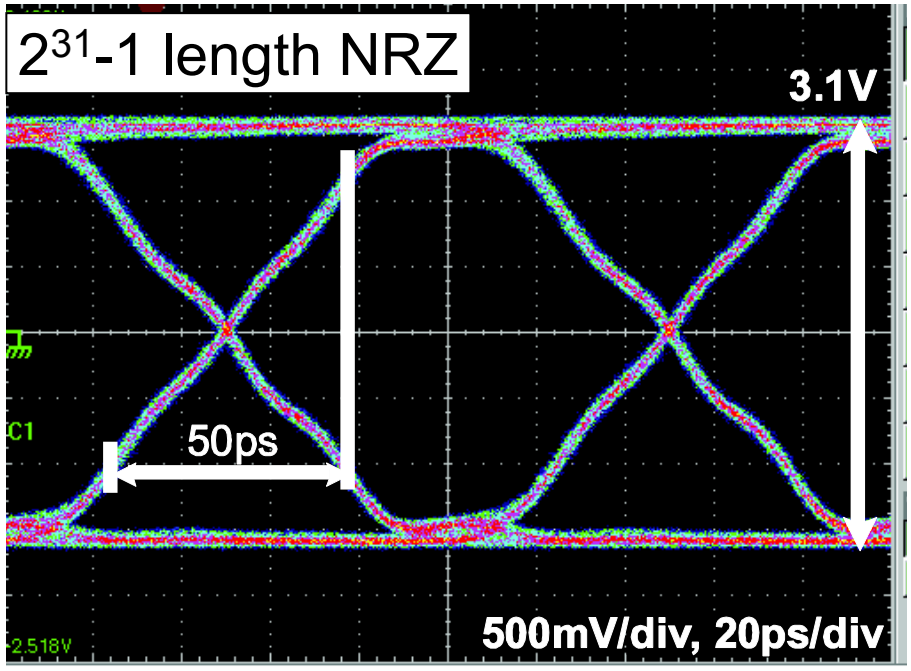


Prototype Photomicrograph

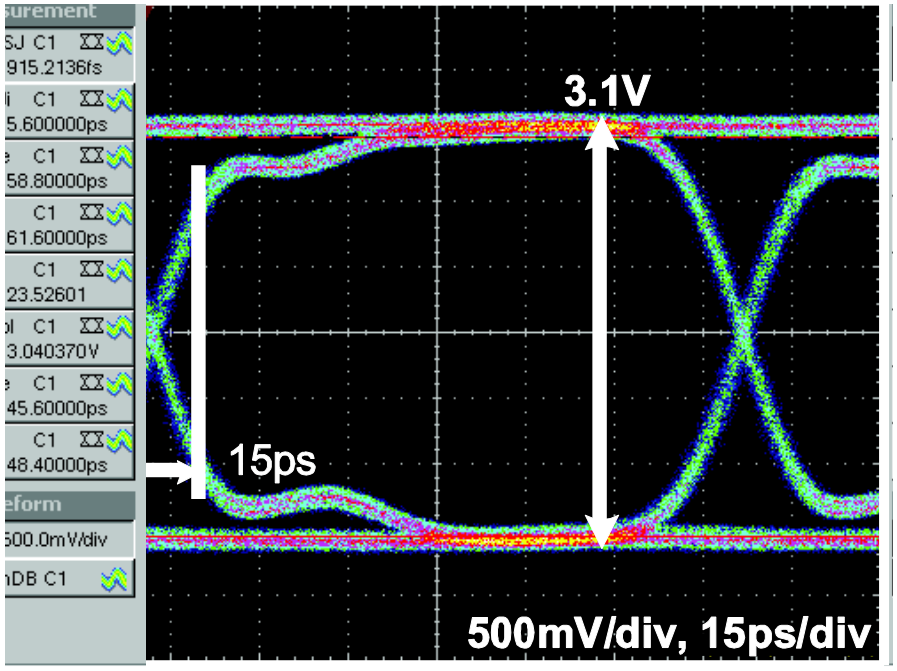


- 2.8mm^2 prototype in IBM-7WL 0.18µm SiGe-BiCMOS (f_T= 60GHz).

Measured Electrical Eye Patterns



Clocks set for max. rise/fall time



Clocks set for min. rise/fall time

- Adjustable edge speed via clock phase control realized by changing the DAC input settings externally.
- 20%-80% rise/fall times (incl. test set-up) are min. 15ps with a tuning range of 35ps.
- Measured jitter is $0.9ps_{rms}$ and $5ps_{pk\text{-}pk}$.

Modulator Driver Comparison

	Digital DA	TGA4954-SL TriQuint	5865 Picosecond Pulse Labs	Nortel JSSC 1996	Mandegaran JSSC 2007	Li JSSC 2006
Data rate (Gbps)	**10**	10	12.5	10	10	10
Output swing (V_{p-p})	**6**	6	8	6	7.6	8
Sensitivity (mV)	**65**	250	250	-	250	600
RMS/Pk jitter (ps)	**0.9/5**	1.61/10	0.7/4	1-2	-/-	0.7/14
Rise/fall time (20%-80%, ps)	**15/15**	25	32/36 (10-90%)	38/38	40/40*	42/42
Output return loss (dB)	**>10, <35GHz**	>10, <20GHz	>10, <20GHz	>10, <20GHz	-	-
P_{DC} (W)	**2.13**	1.1	2.3	3.2	3.7	0.6
Area (mm^2)	**2.8**	-	-	13.2	1.2	0.68
Topology	**Digital-input DA**	Single-ended	Single-ended	Diff. DA	Single-ended	Single-ended
Technology	**0.18µm BiCMOS**	III-V	III-V	AlGaAs/ GaAs	0.18µm BiCMOS	0.18µm CMOS

Summary

- RF and high-speed IC directions in future:
  - **Integrating transceivers for 4G - and beyond 4G systems - in the low-GHz bands used for mobile communication.**
  - **Circuits, devices, sub-systems and packages for emerging low-power and broadband applications using silicon as a platform - but not limited to silicon technologies alone.**
- Challenge-driven research fosters a multi-disciplinary approach to research project definition and execution.
- System, circuit and device development is supporting scaling of silicon CMOS to its limits, until technologies scalable beyond CMOS emerge.

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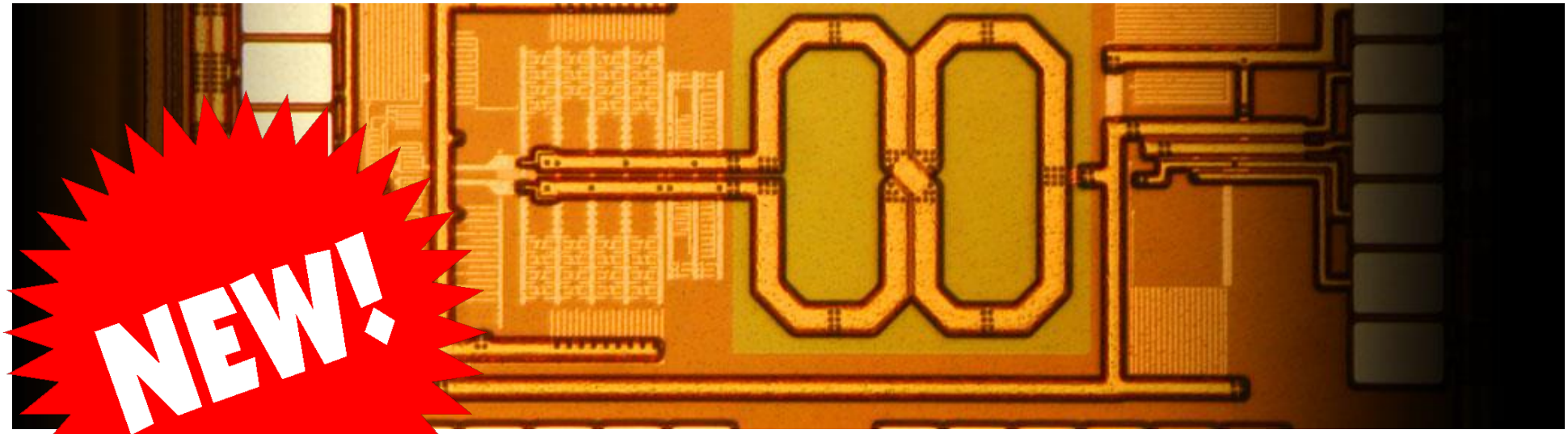

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