Designing Crystal Oscillators

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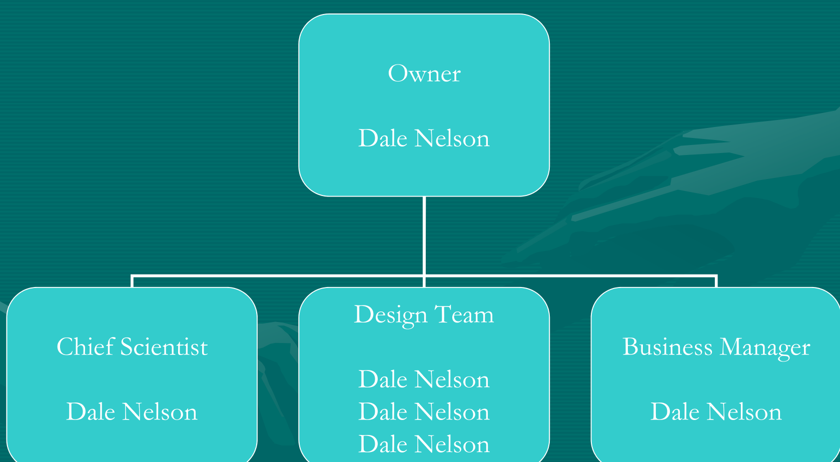
DHN Integrated Circuit Design

DHN Integrated Circuit Design

- Established in Sept. 2005
- Design Expertise:
  - Crystal Oscillators
  - Phase Locked Loops
  - General Analog/Mixed Signal Design
- Dale Nelson
  - Ph.D. in Electrical Engineering from Purdue Univ.
  - Over 27 patents
  - Worked for Bell Labs → Lucent → Agere, and Innovative Wireless Technologies
  - Adjunct Professor at the University of Pennsylvania

DHN Integrated Circuit Design

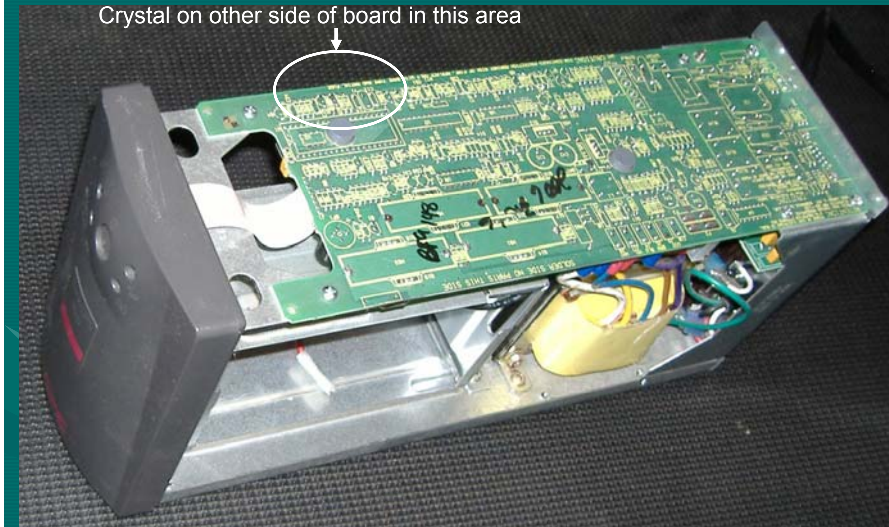
Mandatory Organization Chart



Crystal Oscillators

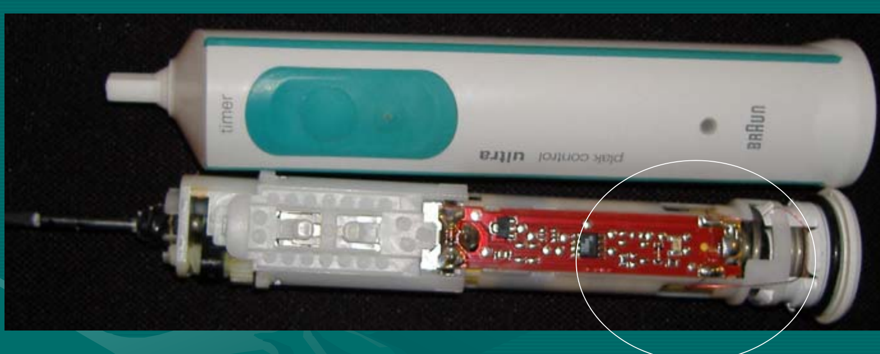
- Found in almost all electronic devices:
  - Disk drives
  - Computer mother boards
  - Telephones
  - Cell phones
  - Televisions, Radios
  - Watches, Clocks
  - Coffee Makers
  - Uninteruptible Power Supplies (UPS)
  - Electric Toothbrushes

U.P.S.

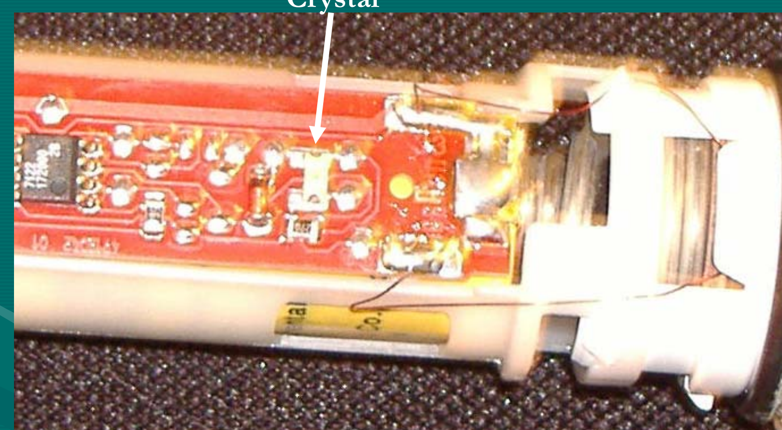


Board in UPS

Electric Toothbrush



Electric Toothbrush



Why use a crystal?

- Accuracy with respect to:
  – Temperature
  – Supply Voltage
  – Time (Aging)
- Quality Factor "Q"

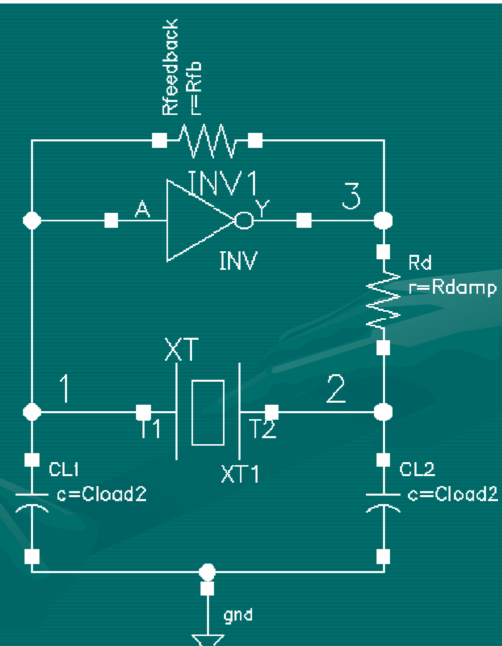
$$Q = 2\pi \frac{\text{Energy stored during a cycle}}{\text{Energy lost during a cycle}}$$

Crystal "Q"

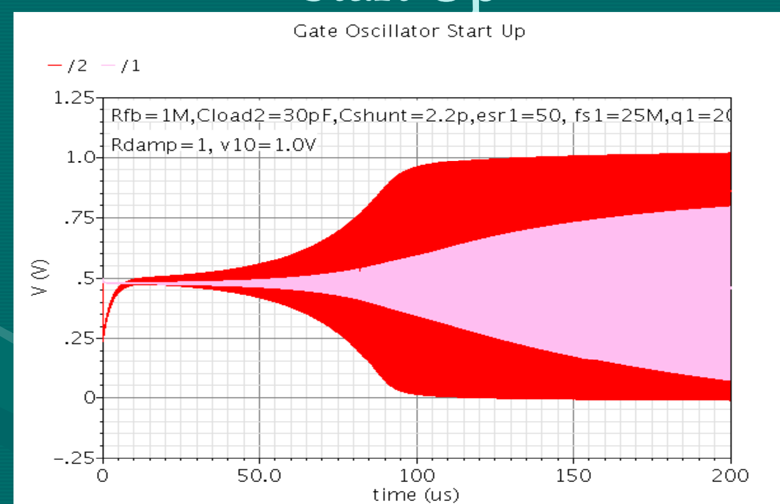
"Q" Value Ranges

RC passive circuit	0-0.5
IC Inductors	4-25
Golf ball	10
Discrete Inductors	20-1000
Church Bell	5000
Crystals	10k-3M

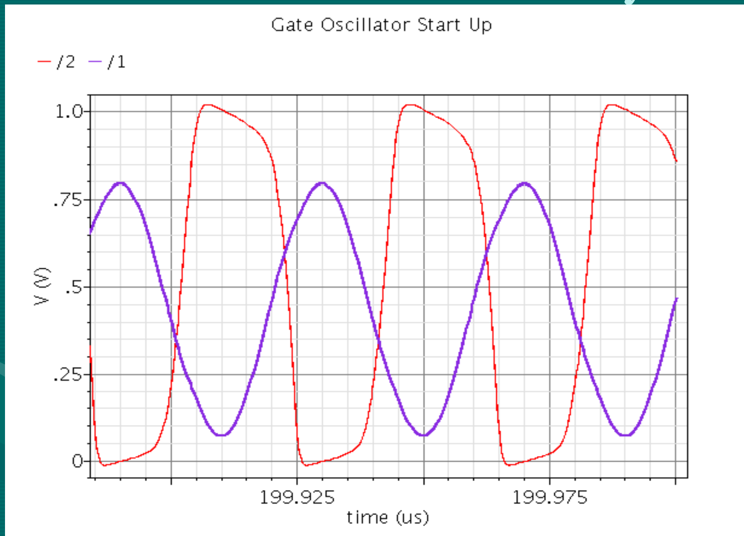
Basic Gate Crystal Oscillator



Basic Gate Crystal Oscillator Start Up



Basic Gate Oscillator Steady State



Crystal Oscillator Transient Simulations

- Good for:
  - Determining signal amplitude, duty cycle
  - Crystal Drive Level (power dissipation of crystal)
  - Start up characteristics (start up time???)
  - Chewing up lots of computer simulation time
- Does NOT tell much about:
  - Margins over PVT (Process, Voltage, Temperature)
  - Useful frequency range of design
  - Why your circuit does not work

Crystal Oscillator Transient Simulation Suggestions

- Select “Options” in Analysis→Choose “tran”
  - Use “traponly”
  - Set “maxstep” to ~1% of target period
- For fast starting, you may need to set an “initial condition” on the “1LC” node in the crystal model.
  - In ADE window: Simulation→Convergence Aids… opens “Select Initial Condition Set”
  - Set voltages so some current flows through the inductor.

Crystal Oscillator Transient Simulation Suggestions (cont)

- I like to use the “Enable” input to start the simulation with the oscillator “off”, and then turn it “on”.
- Some have used a pulsed current source across the crystal to start.
- Turning on “transient noise” for the “tran” simulation can be useful if you want to start at DC “on” equilibrium, high Q.

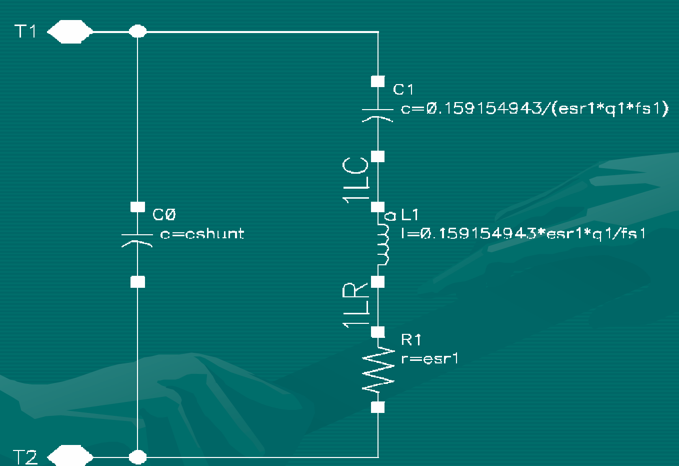
Crystal Specifications

- Typically, Crystal Manufacturers provide:
  - Fundamental or Overtone (Harmonic)
  - Target Frequency at a specified C_{LOAD}
  - Target Frequency accuracy (in ppm)
  - Maximum ESR (Effective Series Resistance)
  - Maximum C_{SHUNT}
  - Maximum Drive Level
  - Temperature Range, Δppm over temperature, or a plot of frequency versus temperature
  - Mechanical information for mounting to PWB
  - Other information pertinent to manufacturing such as soldering temperature information

Crystal Information

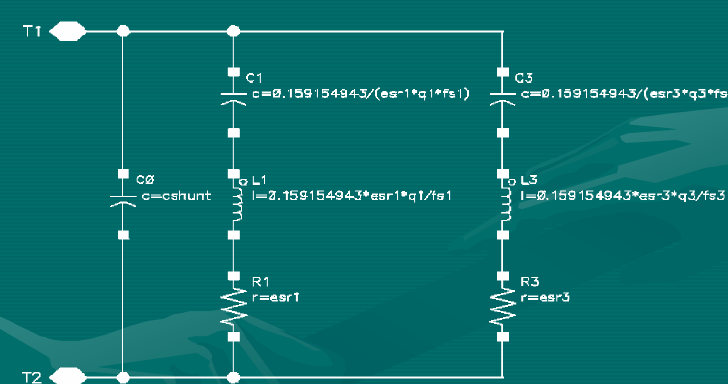
- Typical Data Sheets do **NOT** include:
  - All Crystal Equivalent Circuit Parameters
  - Q value or range
  - Any information about overtones for fundamental mode crystals
  - Any information about fundamental mode for overtone crystals
- Sometimes you can get more information by contacting the manufacturer.

Typical Crystal Model



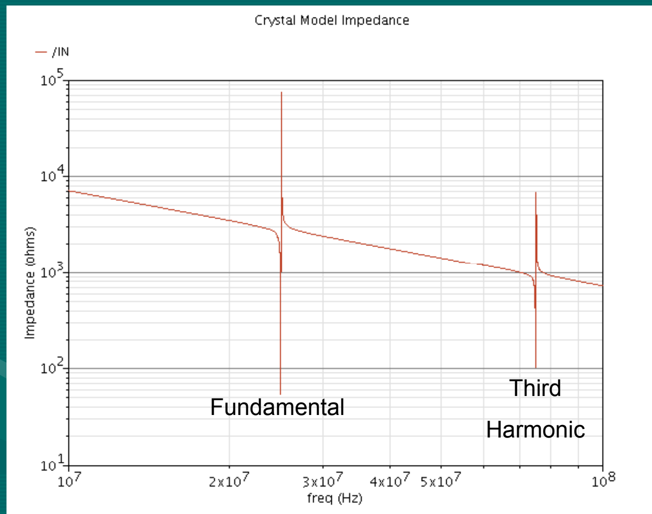
Parameters: cshunt, fs1, esr1, and q1

Fundamental and 3rd Harmonic Crystal Model

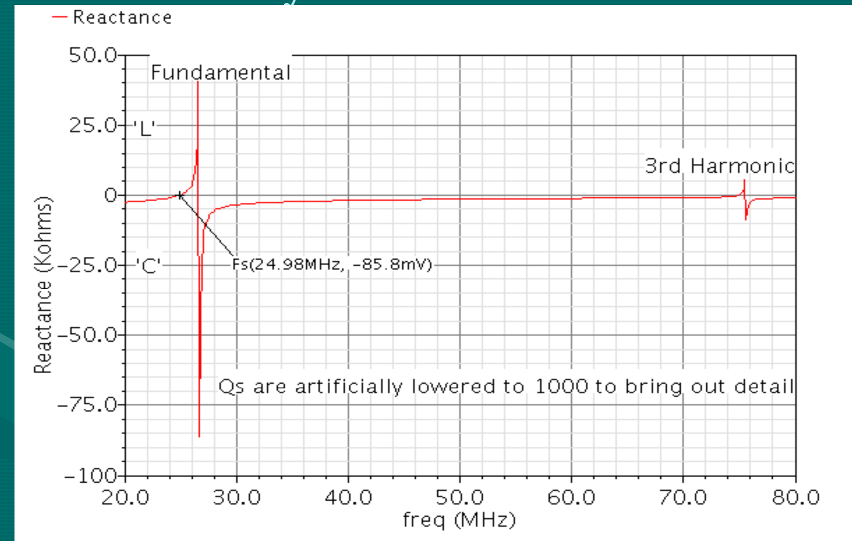


Parameters: cshunt, fs1, esr1, q1, fs3, esr3, and q3

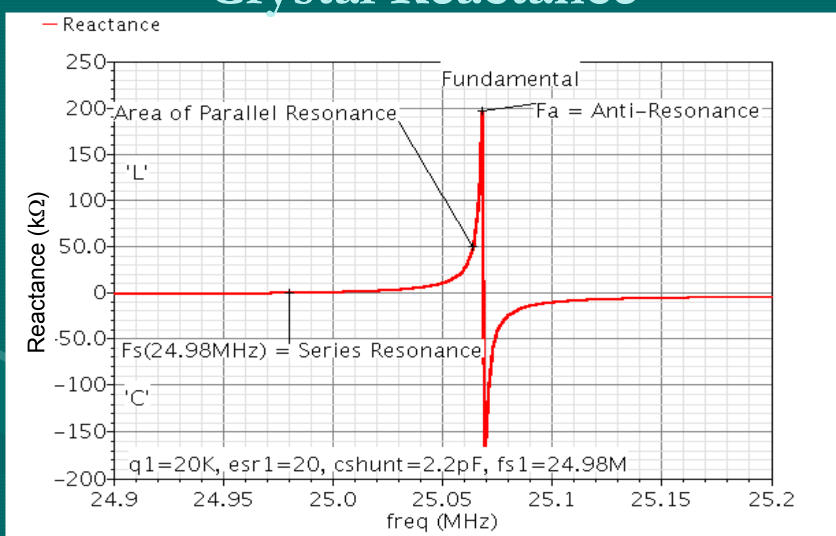
Crystal Impedance



Crystal Reactance



Crystal Reactance



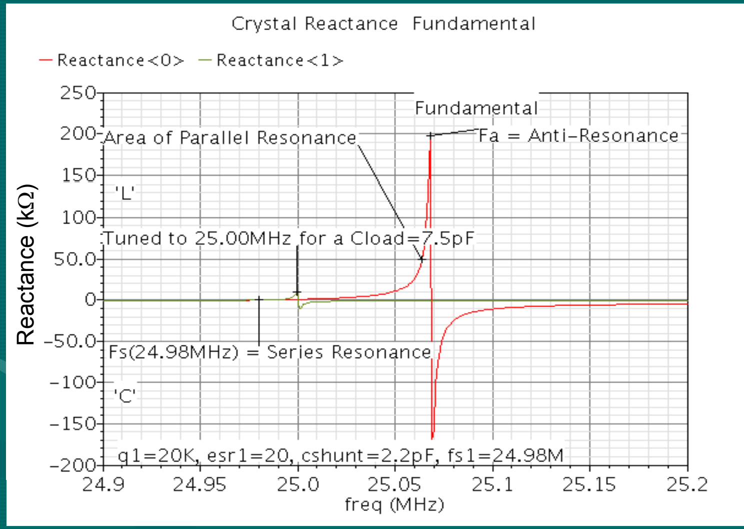
Crystal Tuning

- Crystals are "Tuned" to a particular frequency tolerance for a specified Cload.
  - Can be "Series" tuned or "Parallel" Tuned
  - Since a Gate oscillator works in the "Parallel Resonance" region, you normally want "Parallel Tuned" crystals

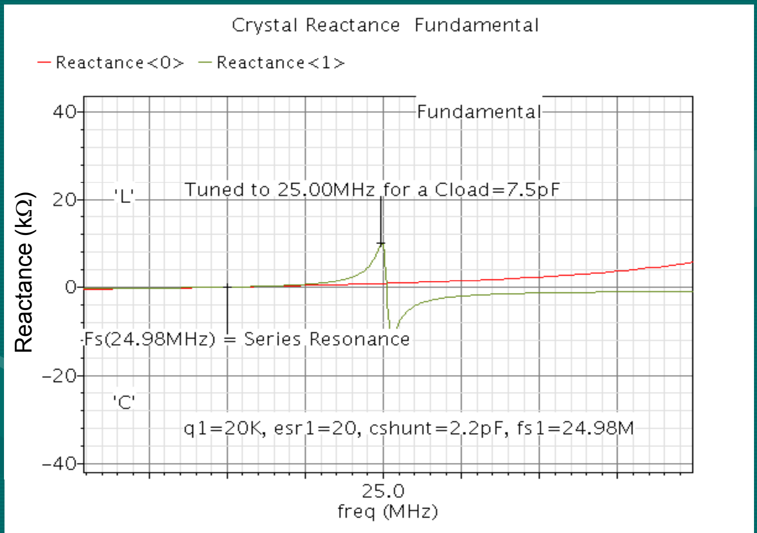
Crystal C_{LOAD}

- C_{LOAD} specification:
  - Represents tuning fixture capacitance plus added parallel capacitance across crystal.
  - Larger C_{LOAD} provides better immunity (less frequency pulling) due to your board and package parasitic capacitances
  - Smaller C_{LOAD} provides:
    - Lower power dissipation inside crystal
    - Better ability to tweak frequency with trimmer cap.
    - More tuning range with a tuning varactor.

Reactance Plot with C_{LOAD}



Reactance Plot with C_{LOAD}



Crystal Equations

$$F_L = F_S\left[\frac{C1}{2(C0 + C_{LOAD})} + 1\right]$$

FL = Parallel Load Resonant Frequency (MHz)

FS = Series Resonant Frequency (MHz)

C1 = Motional Capacitance (pF)

C0 = Shunt Capacitance (pF) (i.e. cshunt)

C_{LOAD} = Load Capacitance (pF)

C_{LOAD} in Oscillator Circuit

$$C_{LOAD} = C_{PAR} + \frac{C_{LOAD1}\, C_{LOAD2}}{C_{LOAD1} + C_{LOAD2}}$$

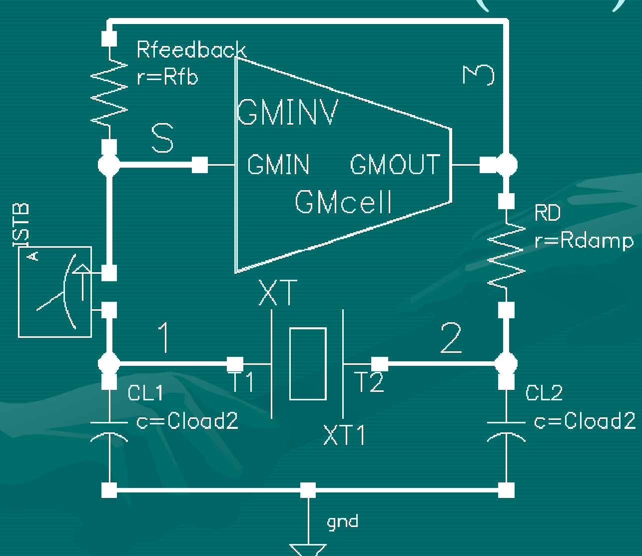
C_{PAR} is the effective capacitance due to your PWB and IC package. You can also separate your parasitic capacitance into between the two paths and from each path to ground.

For $C_{LOAD1} = C_{LOAD2}$, $C_{LOAD2} \approx 2\, C_{LOAD}$

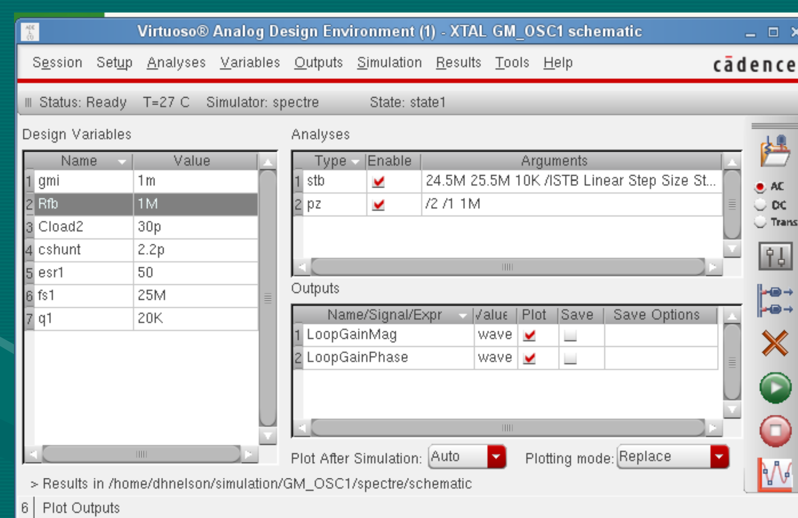
Crystal ESR

- ESR = Effective Series Resistance
  – Can be different at different “Drive Levels”
  – Can change if crystal is over driven
  – Often 1/5th the Max. specified
  – For very low drive levels, the ESR can be much higher → Start up margin required
- Crystal RLC Model is a MODEL,
  – there are no such components hidden inside the package.

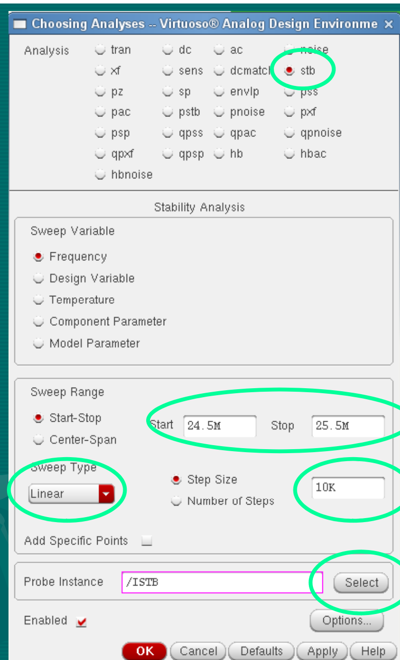
GM Cell Oscillator (Ideal)



ADE Window for GM Cell Oscillator



Setting up stability analysis

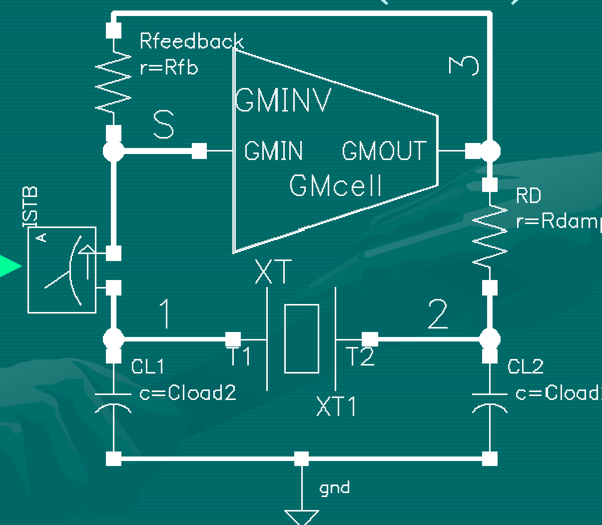


Narrow Range

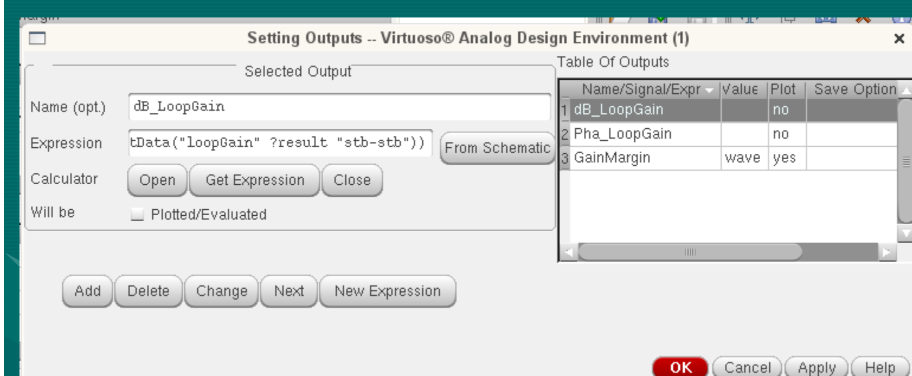
Lots of Points

GM Cell Oscillator (Ideal)

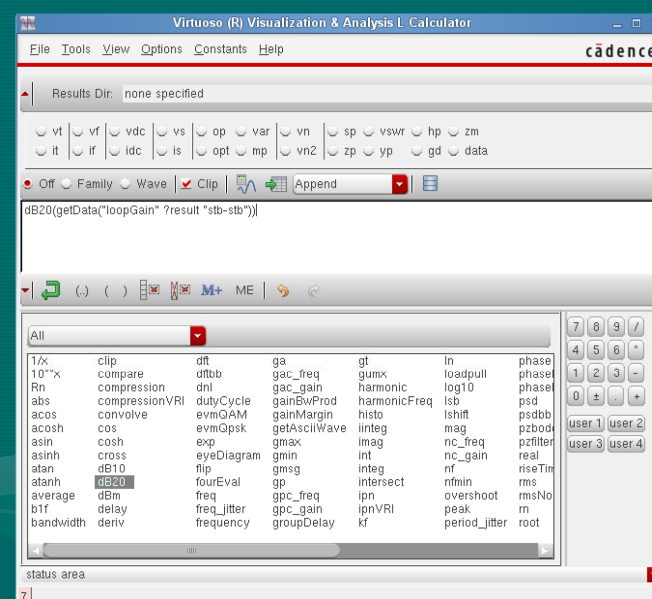
Select Desired iprobe



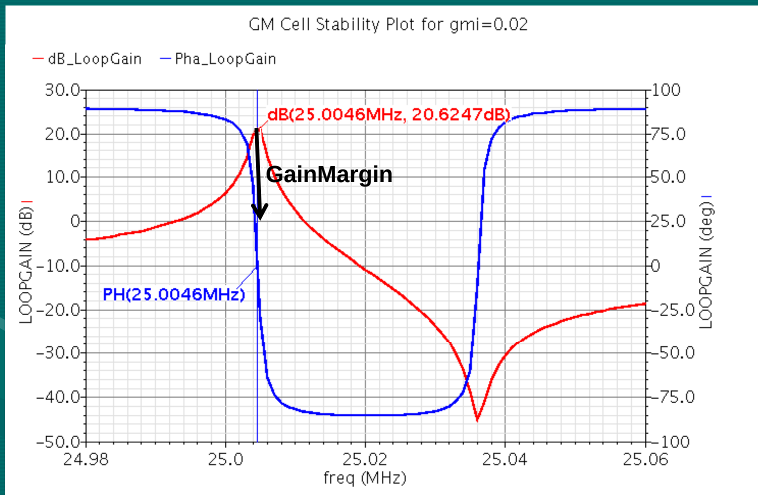
GM Cell loopGain Output Set Up



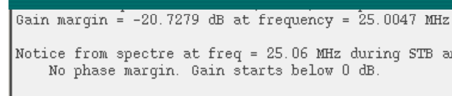
Using Calculator set up dB and phase of loopGain

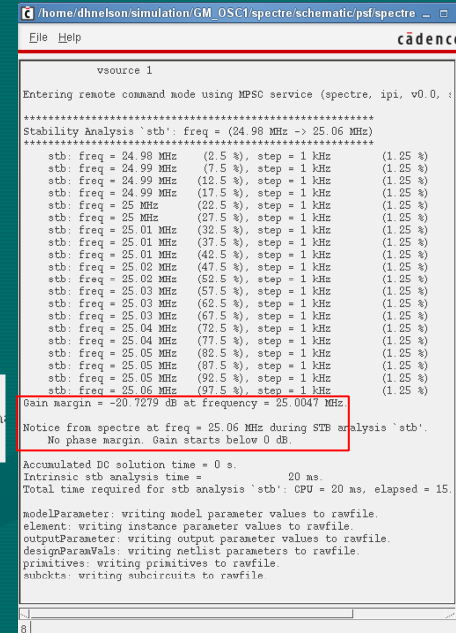


GM Cell LoopGain Plot

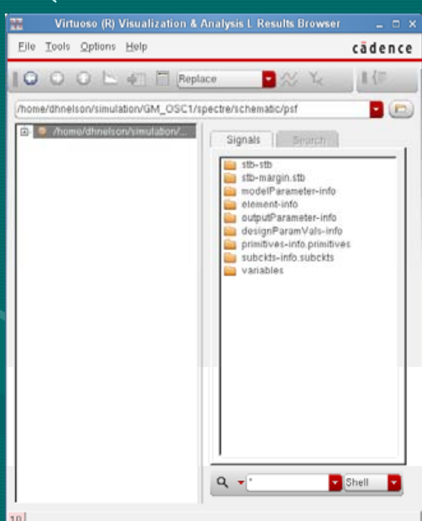


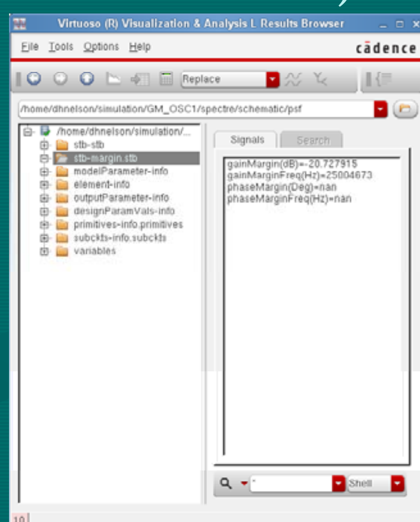
Getting dB and phase of loopGain

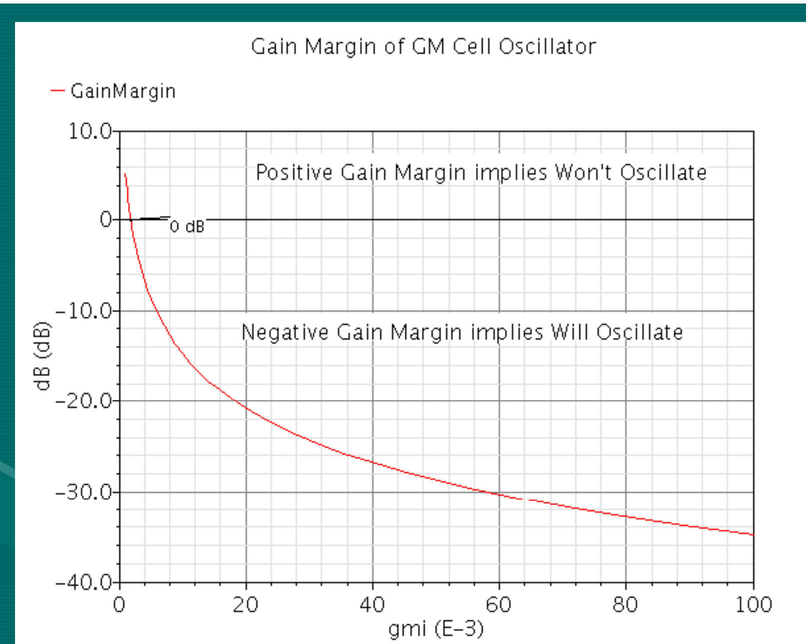


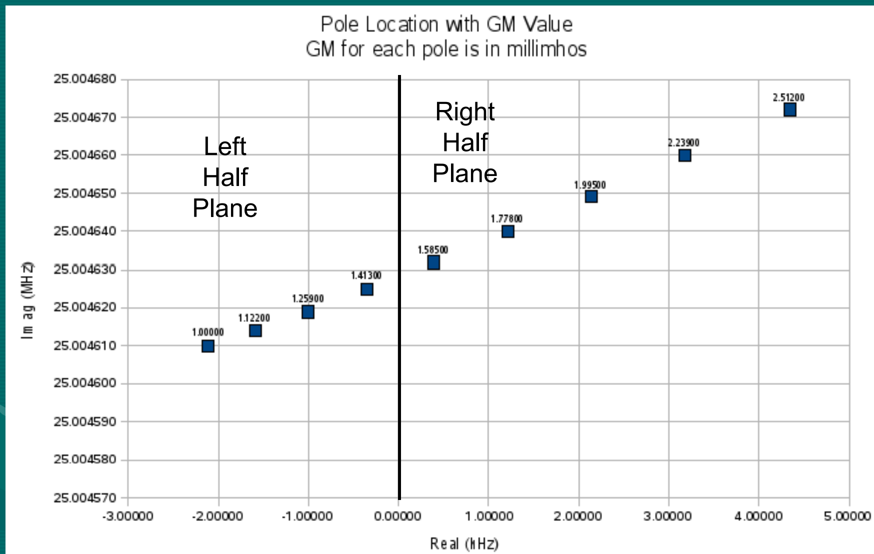


Getting dB and phase of loopGain (In ADE Window: Tools→Results Browser)



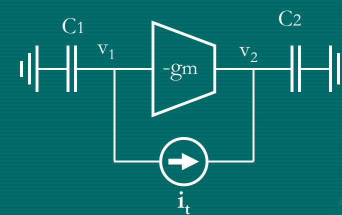






Only +j region shown, -j region is reflection about real axis at j0

Negative Resistance Test Bench



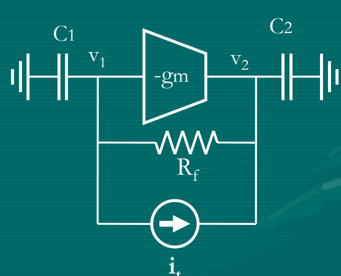
$s\,C1\,v_1 + i_t = 0 \quad \rightarrow \quad v_1 = -\frac{i_t}{s\,C1}$

$-gm\,v_1 + i_t - s\,C2\,v_2 = 0$

$\left(\frac{gm}{s\,C1} + 1\right) i_t = s\,C2\,v_2 \quad \rightarrow \quad v_2 = \frac{\left(1 + \frac{gm}{s\,C1}\right)}{s\,C2}\, i_t$

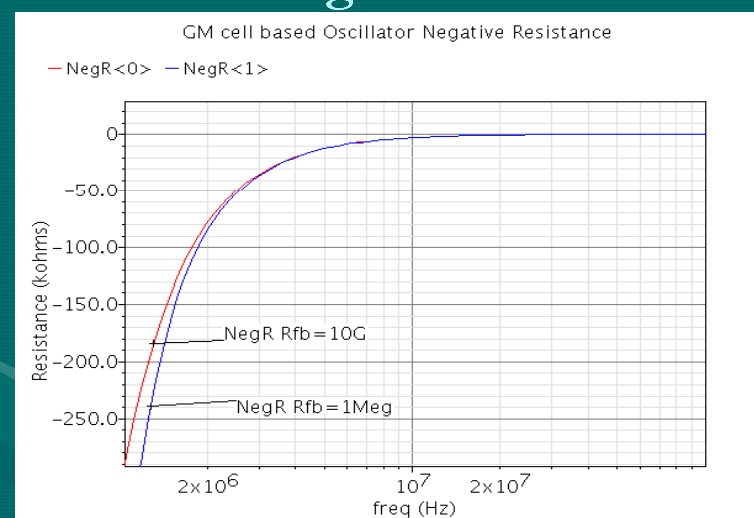
$$Zin = \frac{v_2 - v_1}{i_t} = \frac{s\,(C1 + C2) + gm}{s^2\,C1\,C2} = -\frac{gm + j\,\omega\,(C1 + C2)}{\omega^2\,C1\,C2}$$

Negative Resistance Test Bench with feedback resistor added

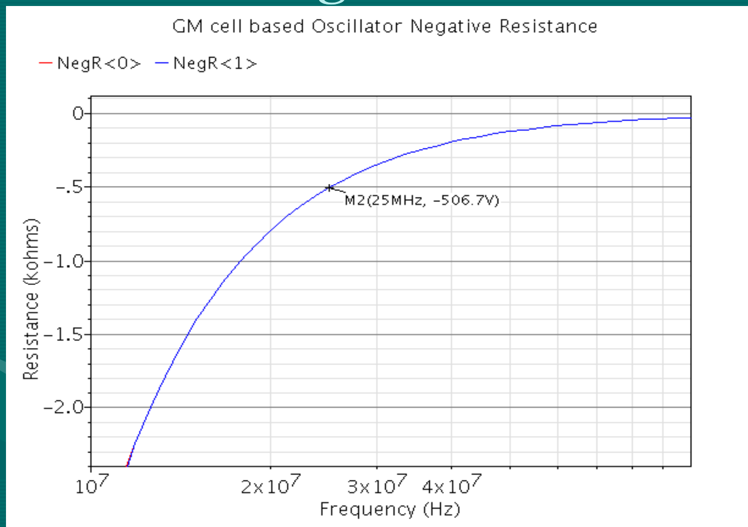


$$Zin = \frac{v_2 - v_1}{i_t} = \frac{s\,(C1 + C2) + gm}{s^2\,C1\,C2 + s\,(C1 + C2)/(C2\,R_f) + gm/R_f}$$

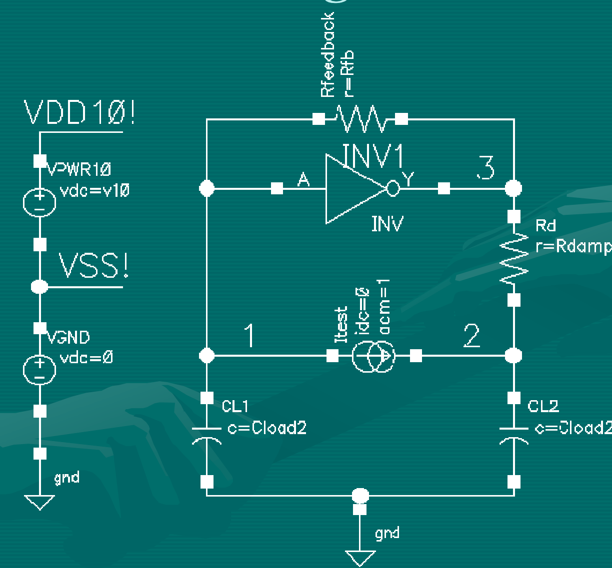
GM Cell Negative Resistance



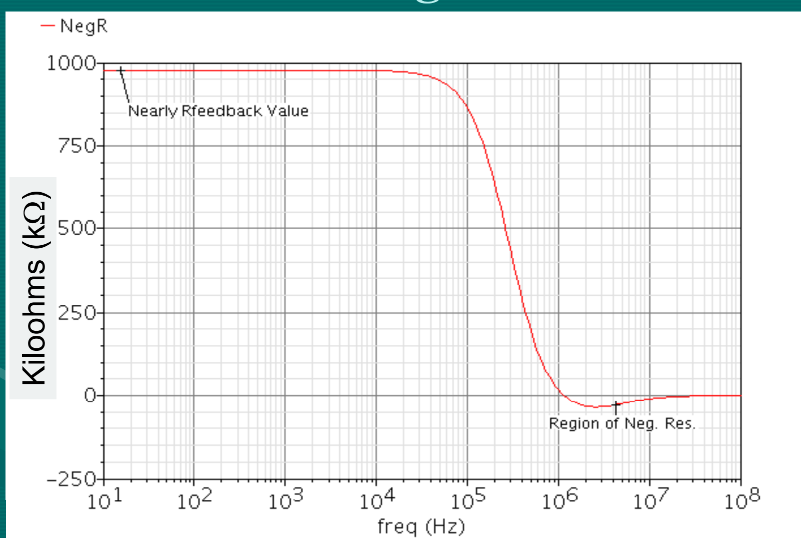
GM Cell Negative Resistance



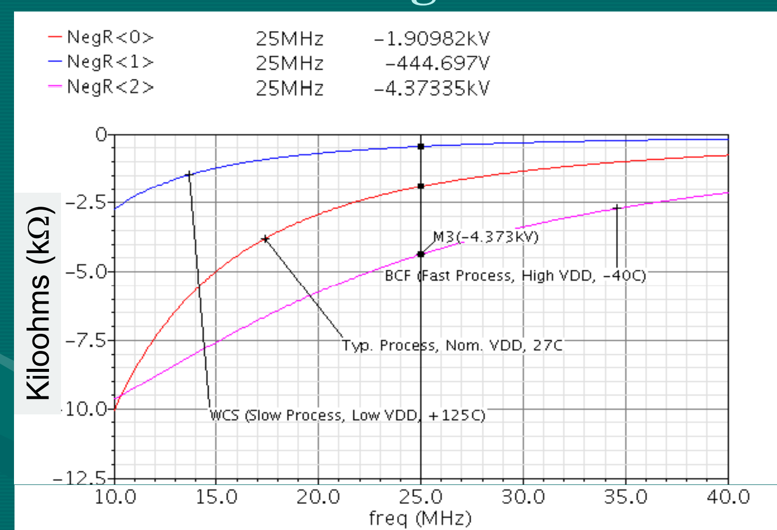
Gate Oscillator Negative Resistance



Gate Oscillator Negative Resistance



Gate Oscillator Negative Resistance



Gate Oscillator Negative Resistance

Rules of Thumb:

- Desirable: The absolute value of the negative resistance should be 10X the maximum ESR.
- Essential: The absolute value of the negative resistance must be 5X the maximum ESR.
  - Applies to your worst PVT corner

Gate Oscillator Negative Resistance

Why????

- Potential for low amplitude oscillation
  - No “digital” output from cell
  - An “inverter” will always be near max. current
  - Insufficient drive level
  - Poor duty cycle if there is a “digital” output
- Potential for not oscillating at all

Negative Resistance versus Stability Analysis

Negative Resistance

- Covers a broad range of frequencies
- Can infer start up/oscillation from
  - Max. C_{LOAD}
  - Max. ESR

Stability Analysis

- Gives margin for specific crystal models
- Must run all PVT for each crystal model
  - Lots more simulations

Strategy: Do a significant amount of your design work using Negative Resistance first, run Stability and Transient simulations after your design is stable.

Transient Simulations needed for

- Determining or verifying your output duty cycle to core specification
- Average Power draw from the supplies
- Signal Amplitude at terminals
- Crystal Drive level

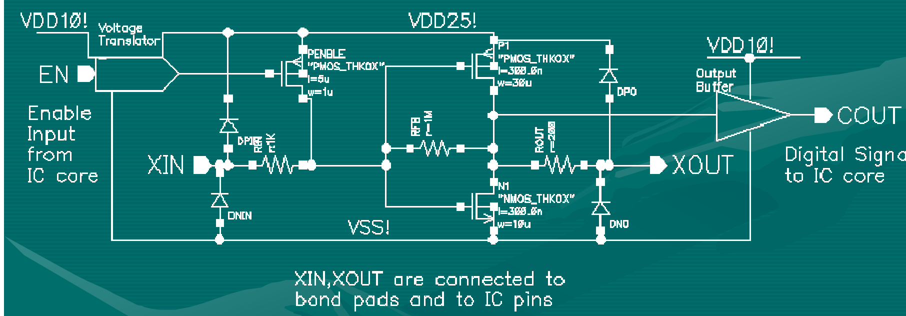
I usually use a reduced Q (400 to 1000) to lessen simulation time required. The lowered Q provides accurate information for the above parameters.

Crystal Oscillator Cell General Requirements

Although the primary function is to provide a digital output signal based on a crystal based oscillator, two other functions are highly desirable:

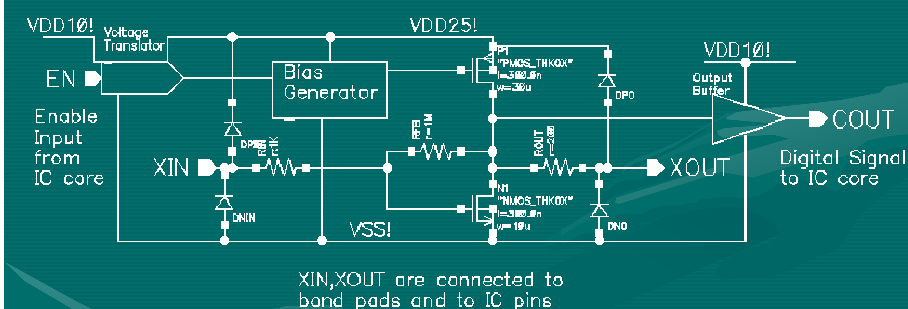
- Power Down to a near zero power drain condition
- The ability to drive a signal into the IC core using an ATE source instead of a crystal

Gate Oscillator Internals 1) Basic CMOS Inverter



Advantage: Transconductance is sum of P1 and N1
Drawback: Transconductance and Power vary widely over PVT

Gate Oscillator Internals 2) NMOS Inverter



Advantage: Transconductance and Power more controlled over PVT
Drawback: Must design low power Bias Generator that reduces PVT sensitivity.

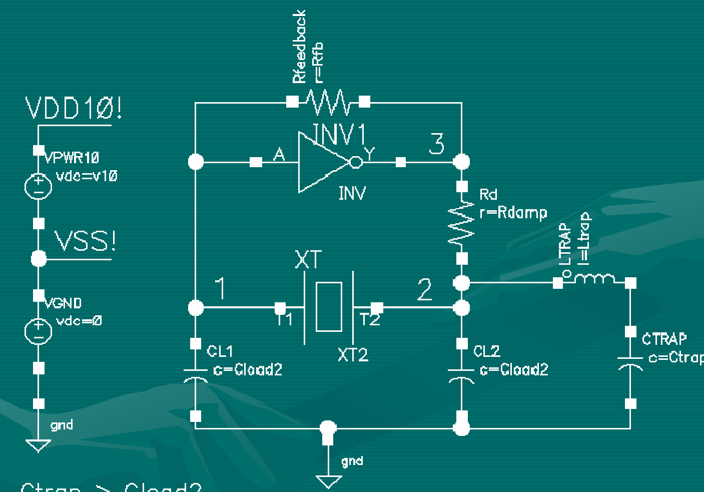
Many Other Options

- In published literature, GM cell based approaches have been used.
- Amplitude limiting or a form of AGC can be added to control amplitude of oscillation and drive level
  - AGC dynamics are tricky due to high Q of crystal
- Getting a low power design requires a more effective way to get large transconductance than the two circuits shown in the previous slides.

Special Situations
Overtone Oscillators

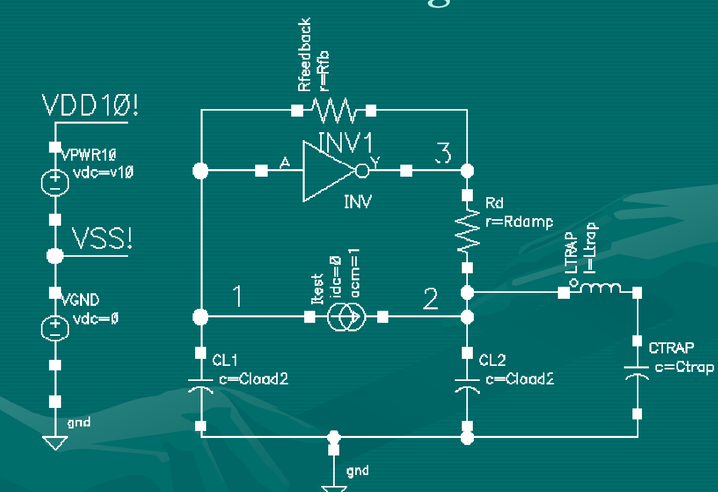
- Require a "trap" to prevent oscillating at the fundamental.
  - An extra inductor is needed outside IC
  - Helps by improving negative resistance at the higher frequency

Overtone Oscillator



Ctrap > Cload2
Ltrap = 0.028*(Cload2+Ctrap)/(Fosc*Fosc*Cload2*Ctrap)
Ctrap = 0.028*Cload2/(Fosc*Fosc*Cload2*Ltrap − 0.028)

Overtone Oscillator Negative Resistance



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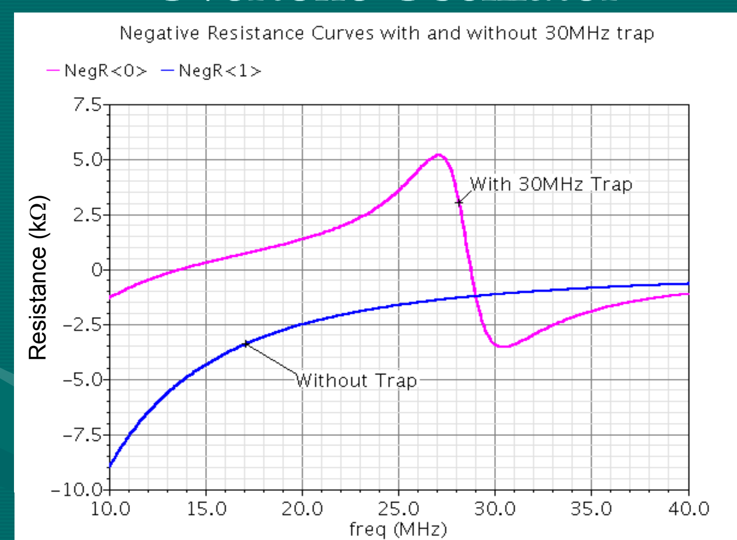
Overtone Oscillator



Special Situations "32kHz" Oscillators

- Sub 100kHz oscillators
  - Need a much larger effective feedback resistor
  - Perhaps open loop biasing
  - Tend to be much larger cells physically than MHz range designs
    - Transistor Area is small
    - Resistors take the most area
    - Capacitors the next most.
    - Low Power→Low Current→Large value bias resistors.

The Oscillator that wouldn't stop

- The external crystal and two load capacitors are where the high current resonance is.
  - When the oscillator bias is turned of, XOUT dc drops to VSS level, but the oscillation (ringing) signal goes below VSS
  - NTUB resistors were used for ESD protection
  - The two NTUB resistors (output,input) created a lateral NPN transistor.

The Oscillator that wouldn't stop (continued)

- Think of the lateral NPN as having its Emitter at XOUT, its collector at XIN, and its base at VSS:
  - Pulling the XOUT below ground turns on the transistor
  - The pull-up PMOS on XIN is not strong enough to dominate, so XIN voltage is pulled to a near normal value, putting the Inverter in an active gain situation, sustaining the oscillation.

The Oscillator that wouldn't stop (continued)

- Using an external resistor R_{DAMP} in the XOUT path limited the emitter current for the parasitic lateral NPN transistor.
  - Now the oscillator stopped as intended.
  - Layout of cell was modified to separate and guard ring NTUB resistors for future designs in that technology.
  - My preference is to use wide poly resistors instead of NWELL/NTUB resistors if possible for the ESD resistors.

The Oscillator that ran at 240MHz

- The PWB design was very concerned about skew of his digital bus signals
  - Gave those signals top routing priority
  - Resulted in crystal being placed about 3” from IC
- The inductance of the paths created an LC tank that oscillated instead of the intended crystal oscillation
  - Fixed by cutting path and bridging cut with a resistor to kill the Q of the unwanted tank

The Oscillator that wouldn’t start

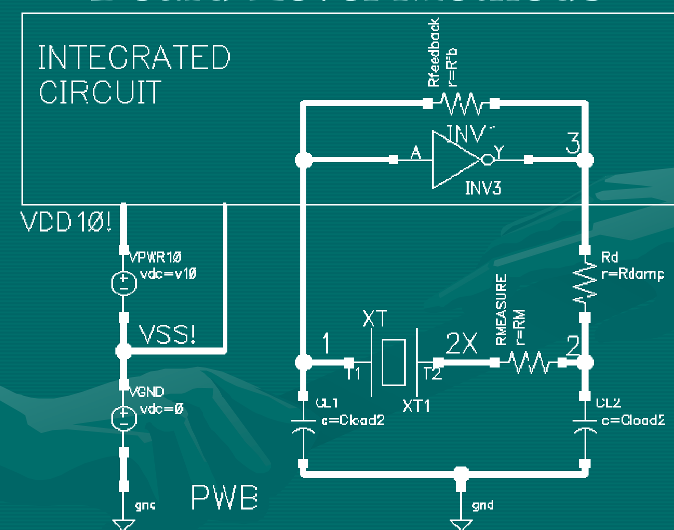
- Initially, looking at the crystal signals, appeared to be just low level noise
- Further investigation revealed about a 900MHz oscillation.
- Layout was much better than previous case, but vias in the PWB paths to the crystal added capacitance and inductance
- A resistor to kill the Q of the parasitic inductance solved the problem

Moral: Always provide space for R_{DAMP} on PWB.

My Post-layout simulation doesn’t show any negative resistance

- Output buffer had several inverter stages
- At one point, there was a minimal cross over of the output of the third inversion stage to the XIN signal as I recall
  - In this design, the output buffer picked from the XIN to improve duty cycle
  - The inverters were scaled exactly as the one for the core oscillator
  - Caused a Miller multiplication of the capacitance, perhaps a factor ~1000
  - Shielded cross over to eliminate

Board Level Methods



Measuring Drive Level

Using a small resistor (RMEASURE) ~1Ω or a current probe in that path measure the ac current (rms) I_M

- The internal current through the ESR resistor should be $(1+{}^{Cshunt}/_{Cload})$ larger.
- Drive Level = $ESR\,(1+{}^{Cshunt}/_{Cload})^2\, I_M^2$

Cload is ~${}^{Cload2}/_2$

Determining Design Margin

- Increase RMEASURE until the oscillator won't start up any more.
  - If the value is >>Max. ESR for your crystals, you have adequate margin.

Notes:

1. Don't use a wirewound potentiometer with lots of inductance
2. Be sure you don't add lots of inductance.
   - Perhap use a surface mount resistor 2X Max. ESR

Board Level Considerations

1. Always layout your PWB to make provision for Rdamp.
2. The two capacitors to ground and the crystal are the primary resonant circuit
   - Keep very close together
   - Keep ground contact for capacitors together if possible
3. Keep the paths from package to crystal short (<1'' if possible with minimum of vias.

Conclusion

- Designing a robust crystal oscillator requires care and attention to details.
- Board Level components and layout are critical to successful design
- I write OCEAN scripts to:
  - Run through the Negative Resistance Curves and extract tables for Data Sheets
  - Run stability analysis over corners and crystal models
  - Run transient simulations as batch jobs
    - Sub-divided by process corner to get parallel effort