Back Contact Thin Film Photovoltaics & My PV System: 9 kW and a Rooftop

Daniel Josell
Metallurgy Division
Material Measurement Laboratory
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Outline:

Introduction to solar panels and devices

Back contact silicon devices

Back contact thin film devices

My PV system
Light hits the photovoltaic device

Each photon that enters with energy greater than the bandgap creates an electron-hole pair.

Carriers are separated by a junction between p- and n-type material and move to +/- electrodes.

Those that don’t recombine on the way or at the interfaces supply current.

Geometries are optimized to maximize absorption of light and minimize carrier recombination.
Thin film devices

The bandgap is maximum energy extractable from a photon

Direct bandgap absorbers such as a-Si, CdTe, CIS or CIGS

Otherwise similar 1D geometry:

Planar contact/p-type/n-type/contact

Thin film technologies based on thin film CdTe can now be produced for less than $1/watt, well below crystalline Si costs. The present cost leader produced at $0.73/watt; production panel efficiency exceeding 12% and record panel 14.7%
Devices based on nanostructuring – CdTe/CdS

Use 3D architecture to achieve lateral carrier separation

Sub-micrometer dimensions for inorganic devices

- 500 nm pitch, 600+ nm tall CdS pillars/CdTe matrix 6% efficient device

Front and back electrode geometry typical of planar thin film and Si technologies

- Gold/copper top electrode reflects 50% of the incoming light

“Hero” Photovoltaic Devices

Numbers in the lab differ from commercial module efficiencies

- Do indicate the potential efficiencies of panel-scale technologies
- Don’t indicate difficulty of achieving performance
- Don’t indicate cost
Some silicon photovoltaics use a dual back contact geometry.

Record setting efficiencies in 1989 over 22% at 1 sun and 28% under 150 sun.


(Dual) back contact geometry

No light blocked by front contact metal lines or transparent conducting oxide

Place dopants and contacts through successive patterning steps

Successive aligned patterning steps

More difficult for dimensions of thin film and nanostructured devices
Start with patterned electrodes

- Utilize the interdigitated “comb” structures of microelectronics as electrodes and deposit semiconductor on them to define device dimensions and geometry.
Devices based on CdS/CdTe system

Electrodeposit CdS on one electrode
Electrodeposit CdTe on both electrodes
Pros:

• Industrially relevant materials system
• Eliminate detrimental UV absorption in “window” layer (i.e., CdS behind the CdTe)
• Eliminate top conducting oxide and metallization that block incoming light
• Create surface topography that could enhance light absorption
• Material and process generic after first electrodeposition step
• Electrodeposition yields extremely high material utilization

Cons:

• Electrode patterning – length scale dictated by recombination length (carrier lifetime)
• Electrodes present during all processing
CdS/CdTe Modeling

Modeling dual back-contact geometry: CdS behind CdTe

100 nm CdS under 2 μm CdTe in the 2 μm pitch 3D devices: different electrode heights vs planar

These early modeling results ignore recombination at interfaces/surfaces

External Quantum Efficiency: EQE – fraction of photons that actually generate current (as function of wavelength)

Taller electrodes are beneficial as they reduce carrier diffusion length
Modeling device performance

External quantum efficiency and device performance are predicted to be dominated by the carrier lifetime

3D surface topography also influences performance
Device performance improves with annealing

Also required for CdS/CdTe planar devices (often in the presence of CdCl$_2$)

Device efficiency of 0.9 % consistent with dimensions, microstructure, non-ideal contacts

Resistivity is an issue in these devices
CdTe grain size increases and CdS/CdTe junction improves with annealing

- Performance improves

Electrodeposited CdTe reacts with the Pt electrodes during annealing after CdCl₂ solution dip

- Voids form at the interface prior to optimum annealing for the semiconductor and device fails

Electrodeposited CdTe does not react with Ru electrodes during annealing after CdCl₂ solution dip

- Adhesion not ideal
Performance of devices annealed at 350 °C for 20 min exhibits trends consistent with transport limitation expected for low temperature anneal.

- $J_{sc}$ trends with the width of the gap between electrodes – consistent with simulation
- $V_{oc}$ only weakly trends with the gap

Performance limited by annealing conditions and contact to CdS

**Experiment**

- 450 nm tall electrodes
- 20 min, 350 °C air anneal, with CdCl$_2$
CdS/CdTe Evaluation

Modeling suggests origin of observed EQE behavior for these materials/devices

- High density of carriers generated near the surface for shorter wavelengths results in increased recombination due to poor quality of material (short lifetime)
- Low lamp intensity possible origin up uptick at shortest wavelengths (i.e., artifact)
CdSe/CdTe Devices

Back contact geometry gives flexibility

- N-type material substitution without risk of blocking incoming light
- Might improve contact, junction, overall performance

Replace CdS with CdSe

- Lower bandgap ~1.7 eV is unacceptable for CdTe absorber with front contact/window layer
- Very thin (50 nm) iridium contacts - nonreactive
Improved EQE for ~0.6 and ~0.9 µm thick CdTe
Decrease at shorter wavelengths not due to absorption in (nonexistent) window layer

Improved AM1.5 short circuit current and fill factor
No voiding at the semiconductor/iridium electrode interfaces
Large work function iridium not ideal for n-type CdSe contact...
Performance depends on thickness of CdSe
  Too thin – pinholes lead to shunting, reducing $V_{oc}$ and $J_{sc}$

Performance depends on electrode gap
  Too wide, recombination occurs before charges can be collected, reducing $J_{sc}$

AM1.5 : Eff. 2.0%; $V_{oc}$ 510 mV; $J_{sc}$ 8 mA/cm$^2$; fill factor 48%
EQE: maximum 29%

Smallest pitch 2 µm
Higher quality CdTe – pulsed laser deposited (M. Sahiner, Seton Hall Univ.)

Short circuit current 60% higher at 13.5 mA/cm² and EQE exceeding 41%

- $V_{oc}$ needs to be improved
- Resistivity is less of an issue with higher quality CdTe – reduced dependence on pitch

The CdSe does not prevent incoming light from reaching the CdTe absorber

- CdSe in front of the CdTe would absorb at ~730 nm; but it is behind.

Device area 0.16 cm²
Summary:

- Back contact geometry solar cells – eliminating layers that block light and add to processing complexity
- CdS/CdTe devices – traditional materials in back contact geometry
  - AM1.5: $J_{sc} = 4 \text{ mA/cm}^2$, $V_{oc} = 520 \text{ mV}$, $ff = 39 \%$, Eff. = 0.9 \%; Max EQE = 21\%
- CdSe/CdTe devices – taking advantage of the geometry to substitute materials
  - AM1.5: $J_{sc} = 8 \text{ mA/cm}^2$, $V_{oc} = 510 \text{ mV}$, $ff = 48 \%$, Eff. = 2.0 \%; Max EQE = 30\%
- CdSe/CdTe (PLD) devices – the role of material quality in device performance
  - AM1.5: $J_{sc} = 13 \text{ mA/cm}^2$, $V_{oc} = 400 \text{ mV}$, $ff = 42 \%$, Eff. = 2.2 \%; Max EQE = 41\%
- These are early devices
- Back contact devices based on other materials and processes by other researchers

Ongoing Efforts

- Smaller dimensions
- Differentiated electrodes
- Surface passivation
- Other materials


42 panels with 17.1% panel (19.3 % wafer) conversion efficiency and microinverters
“Nameplate capacity” 9.02 kW DC
Peak capacity ~ 8 kW AC
Nominal Generation ~ 11 MWh/yr

Panels were highest available efficiency when installed
Hip-roof: East/West panels are nonideal, mainly in winter as solar path sinks toward south
Tree coverage on west face
Our electric bill is:
$7 /mo (fee) for two-thirds of the year
This reflects net metering carryover
Substantially reduced in winter months.
Amortization of total install cost

Payback:

2010:
- 30% Federal income tax credit
- ~$7k MD grant

2012:
- Mo.Co. $5k property tax credit

Each Year:
- Eleven Solar Renewable Energy Credits (SRECs)
- Electric bill energy savings
- Five years of ~$100 state income tax credit

Premium panels added > $1/watt – but high watt system lowered roof costs by $1/watt
Thinking of installing your own?

Pros:

- Energy savings are always there but their value depends on the nature of your heating/cooling, utilization, etc.
- Panels are *much* cheaper than when I installed my system
- They are guaranteed to provide 80% of nameplate value for 25 years (!)

Cons:

- Does not address balance of system costs
- County and state programs are no longer available
- Future of federal credit is uncertain
- SREC value has always been an unknown – recent state legislation aimed at stabilizing/raising it for a few years

I am as happy to discuss PV installation and installers as I am to discuss my research.
Thank you for your attention!