Power Distribution Network Design for High-Speed Printed Circuit Boards

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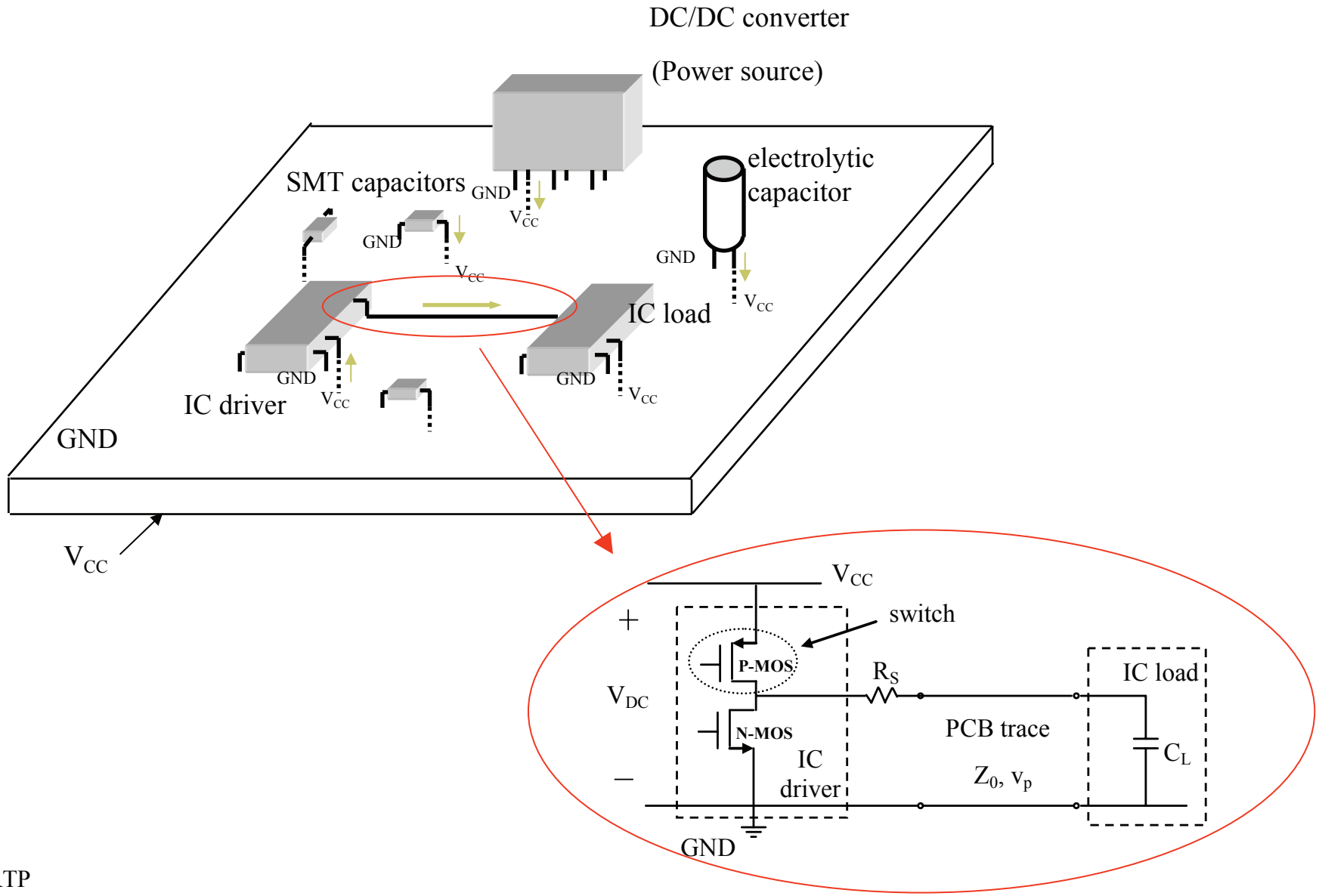
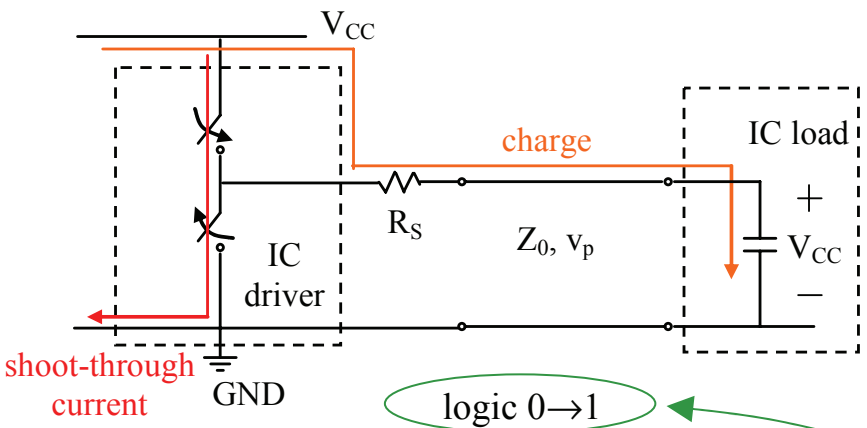
Outline

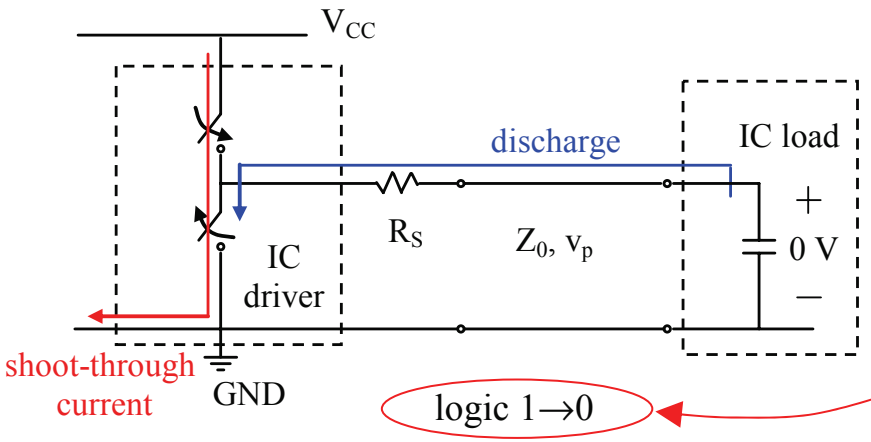
- Overview of PDN design in multi-layer PCBs
- Interconnect Inductance
- Individual Capacitor Values
- Capacitor Location
- Power/Ground Plane Pair
- Summary

PDN in a Multi-Layer PCB

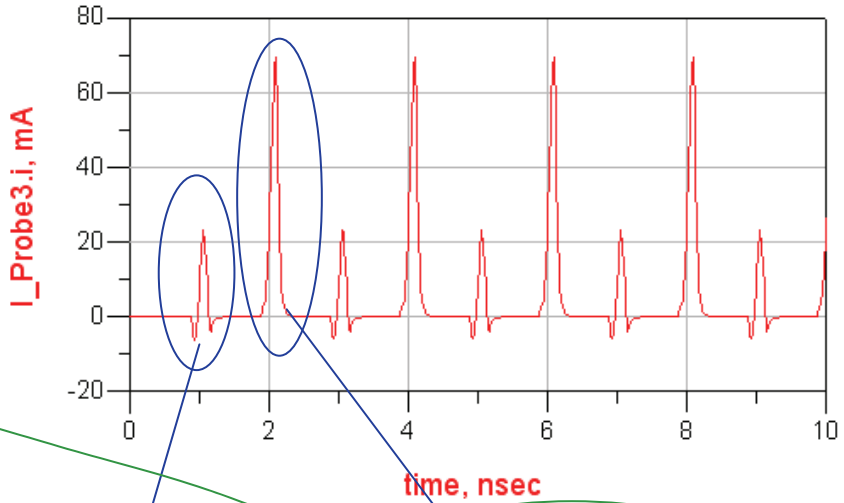


Device Switching





Current drawn from power

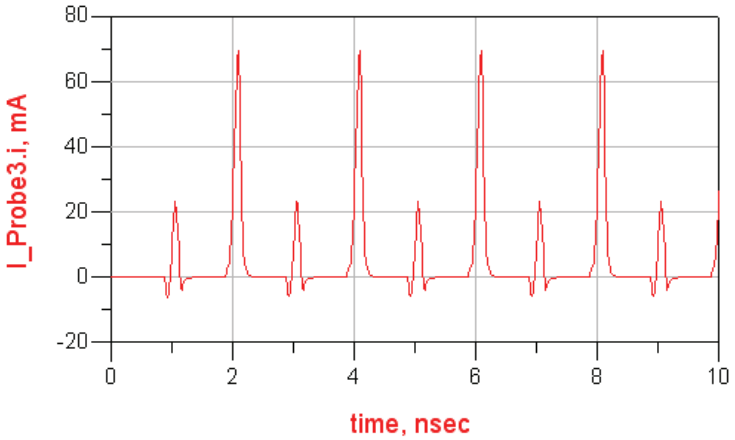


Shoot-through current only

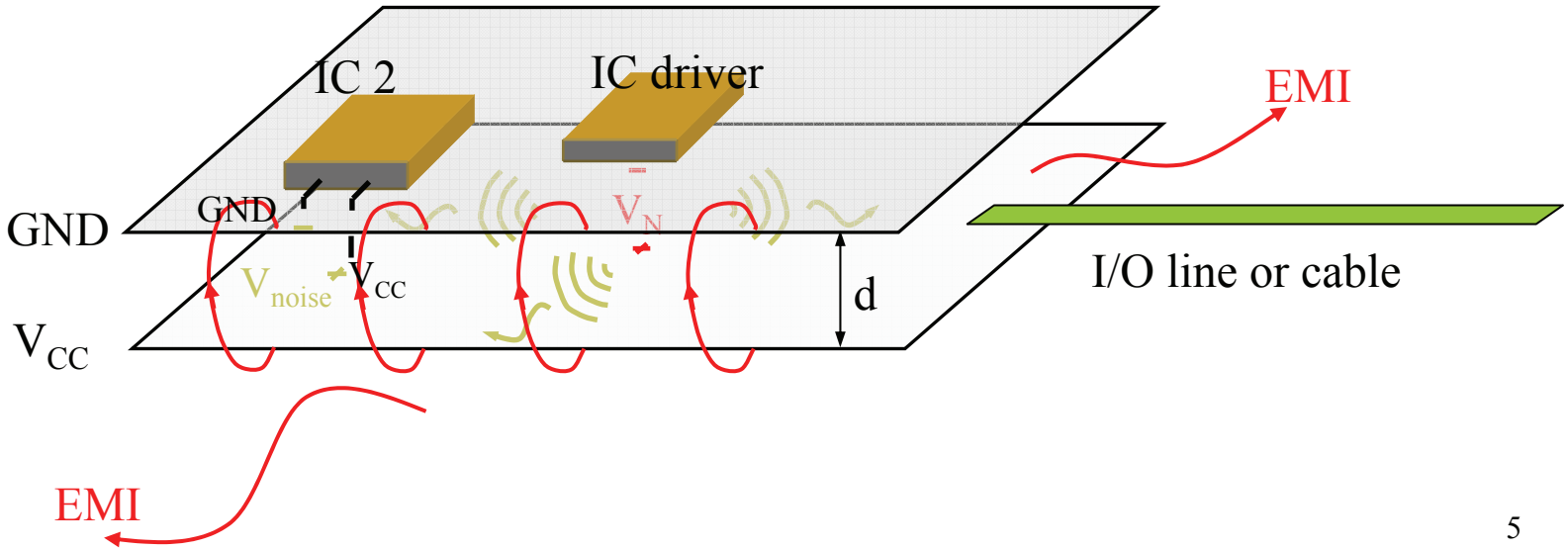
Shoot-through + load charging current

J. L Knighten, B. Archambeault, J. Fan, et. al., "PDN Design Strategies: IV. Sources of PDN Noise," *IEEE EMC Society Newsletter*, Winter 2007, Issue No. 212, pp. 66-76.

Current Supply and Power Bus Noise

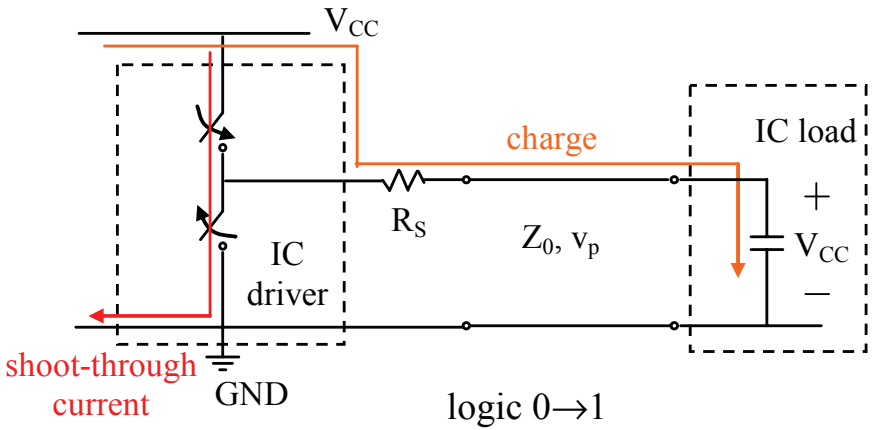


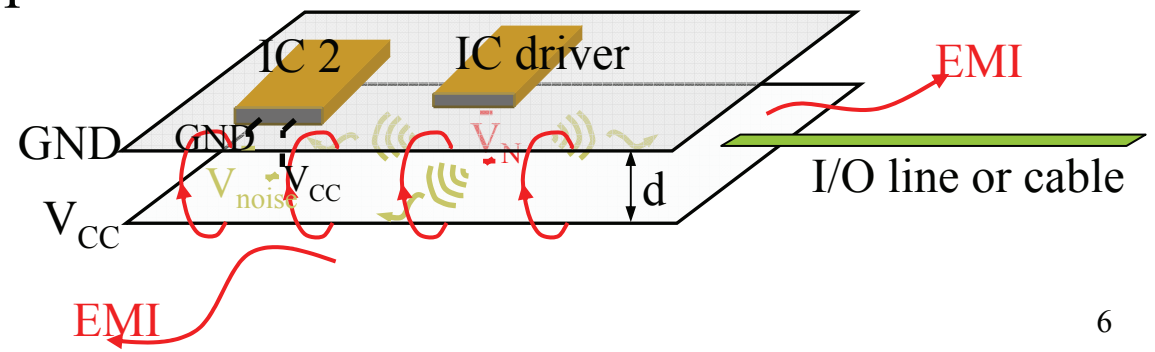
I am Mr. Charge!



PDN Design Objectives

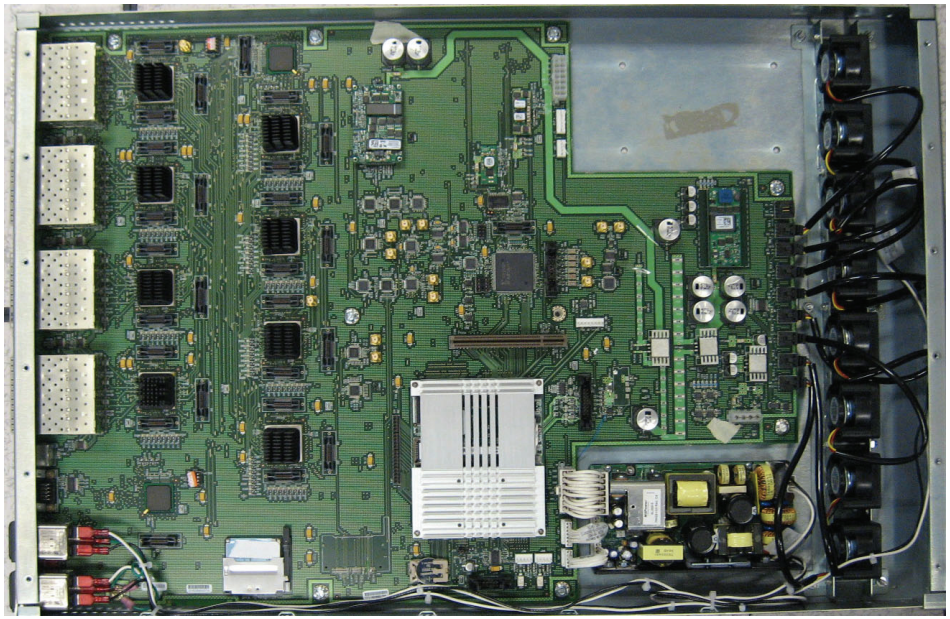
1. Ensure charge supply for logic transitions
   - Enough capacitance to store charge
   - Enough charge readily available for short transitions
2. Minimize noise voltage distribution on the V_{CC}/GND plane pair
   - Low power bus impedance over frequency
   - Noise decoupling
   - Noise isolation



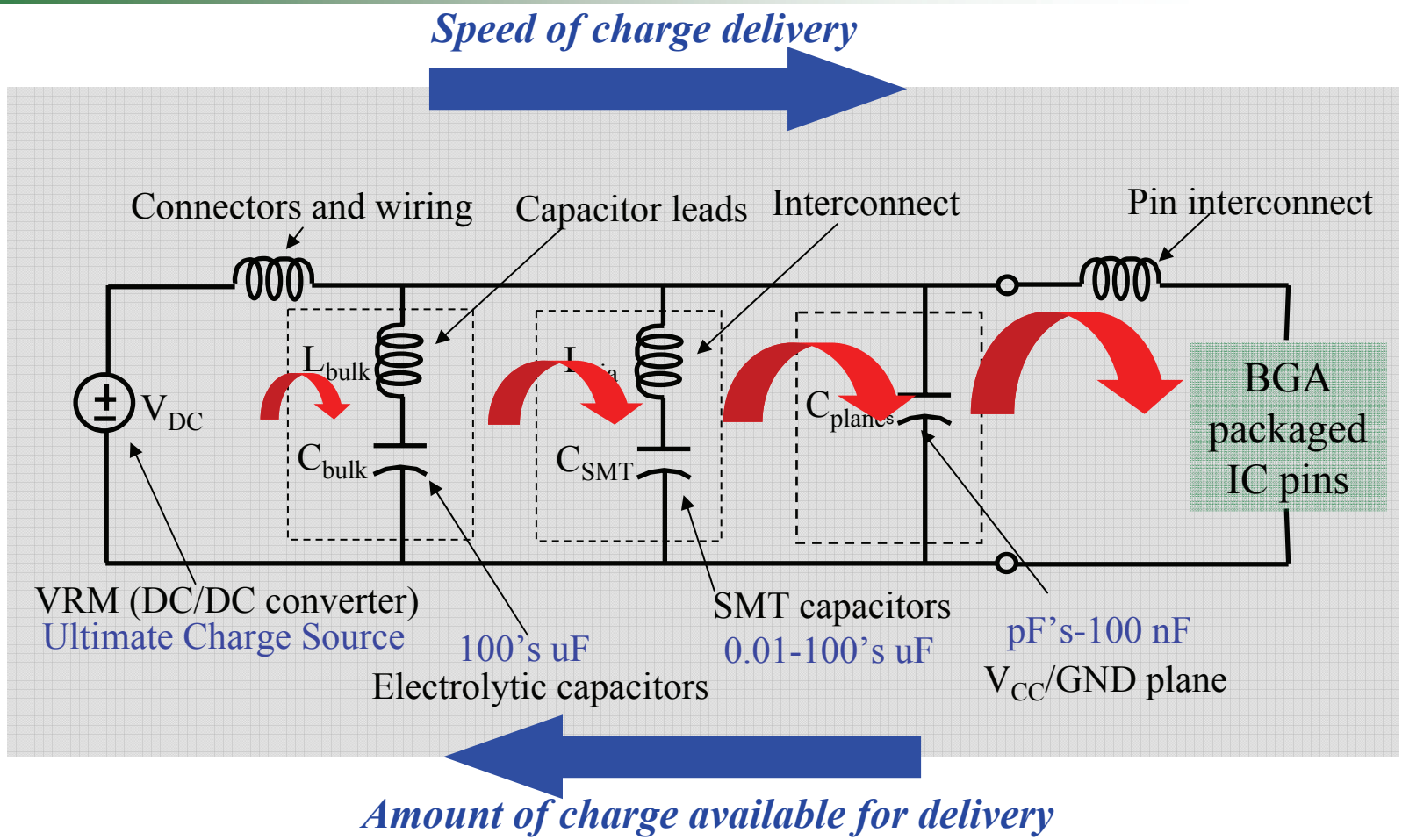


PDN Design Issues in PCB

- Capacitor interconnects;
- Individual capacitor values and packaging forms;
- Number of capacitors needed;
- Capacitor placement;
- PCB stack-up;
- Power/ground plane pair geometry;
- Segmentation and isolation

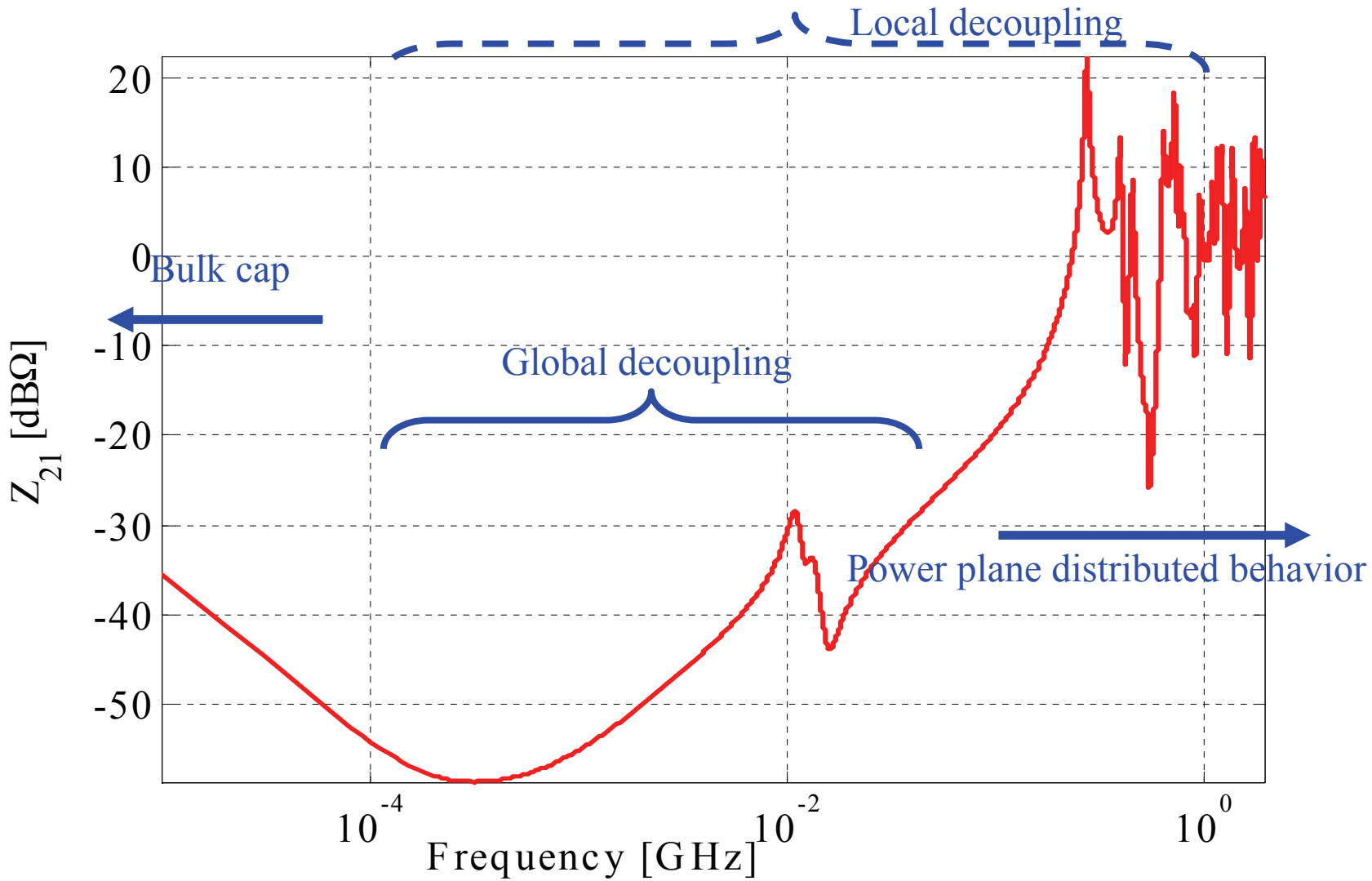


PDN Charging/Discharging Hierarchy



- The planes can be regarded as a *C* only @ low frequencies

PDN Impedance Profile



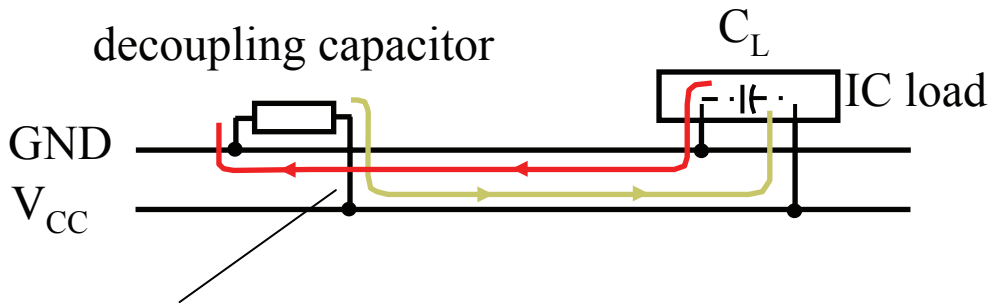
Outline

Interconnect Inductance

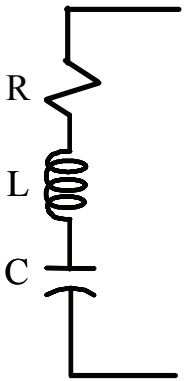
- shall be minimized in any situation

Effect of Inductance

Inductance – impedes the flow of current (charge) to the load that will charge it to achieve a logic 1

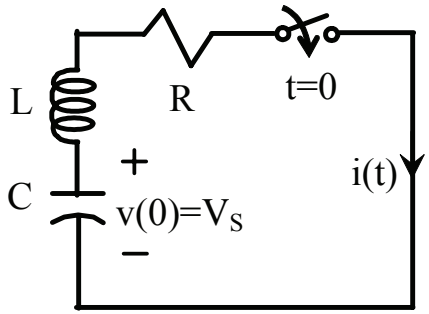


Inductance associated with the capacitor: package parasitics, bonding pads, board traces, and vias



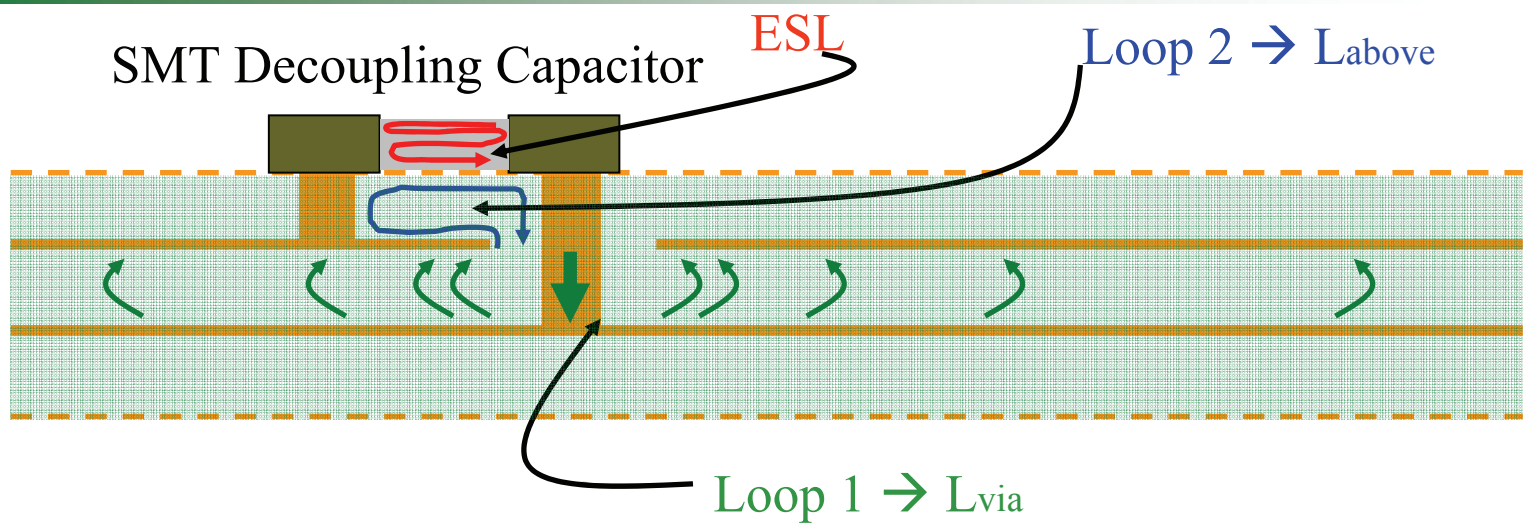
$$Z = R + j\omega L + \frac{1}{j\omega C}$$

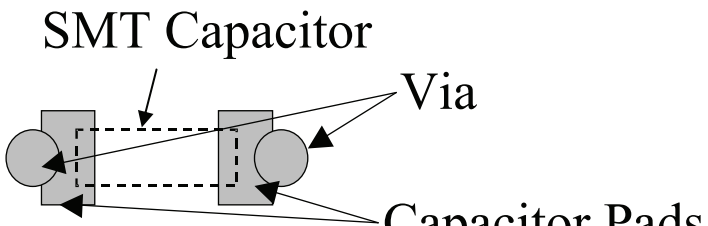
$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$



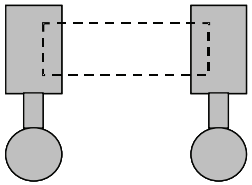
$$i(t \geq 0) = V_S\sqrt{\frac{C}{L}}\sin\left(\frac{t}{\sqrt{LC}}\right)$$

Minimizing Interconnect Inductance

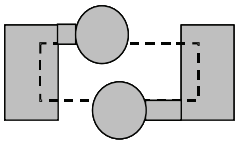




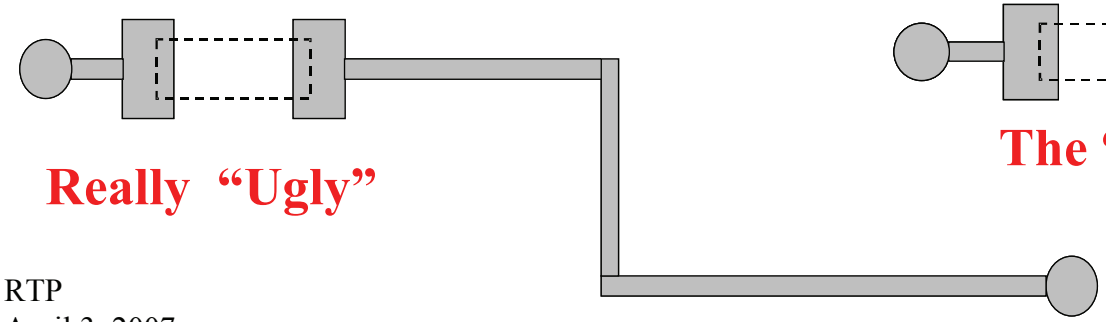
The "Good"



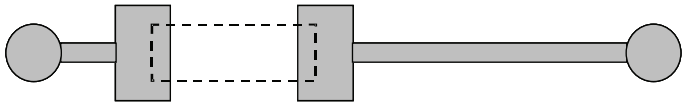
The "Better"



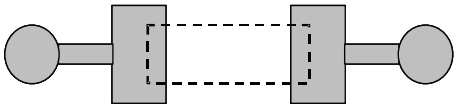
The "Best"



Really "Ugly"



The "Ugly"



The "Bad"

Outline

Individual Capacitor Values

- multiple values or maximum value? May not matter

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

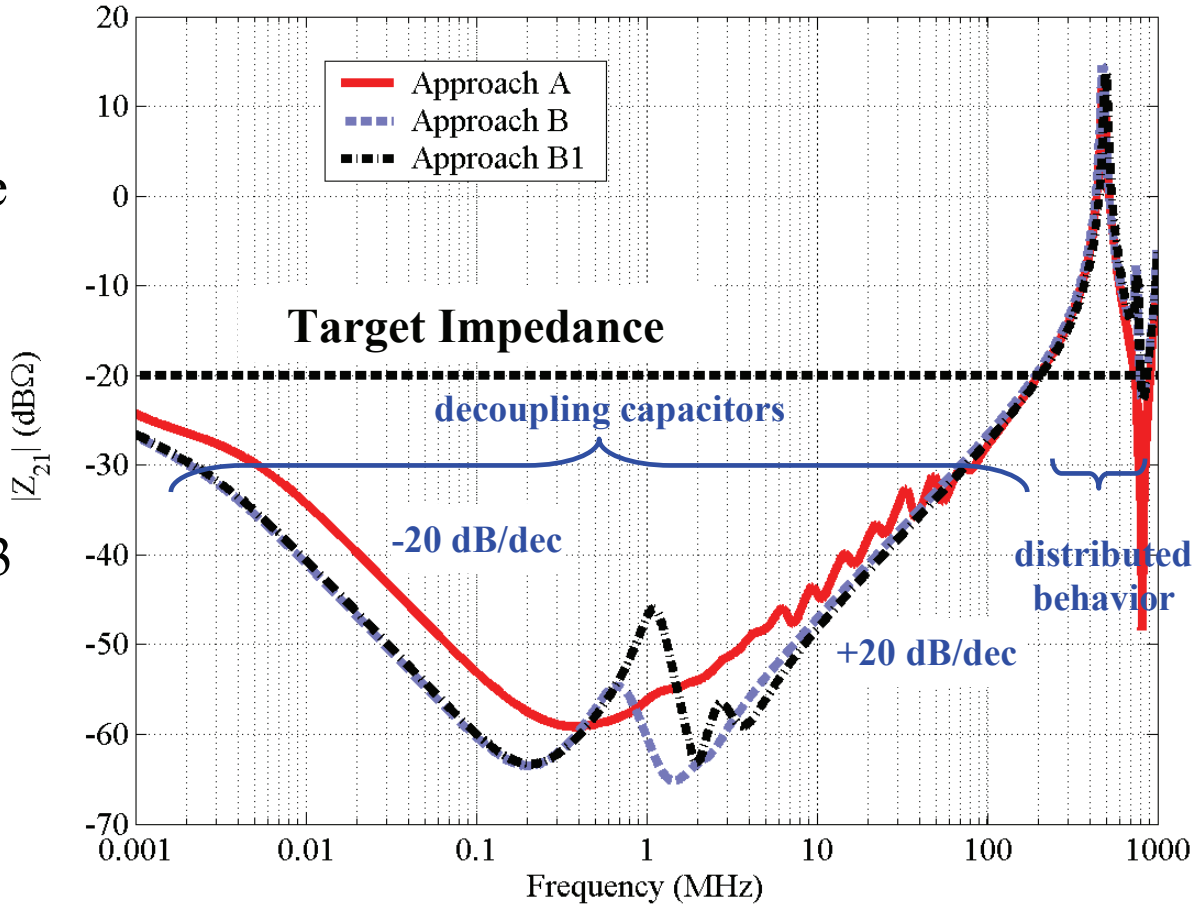
Two Common SMT Decoupling Strategies

- Use an array of capacitor values:
  - This may be the best known approach and is very popular in the signal integrity design community (SI-LIST).
  - Rationale: to maintain a flat impedance profile below a target impedance over a wide frequency range
  - Typically a logarithmically spaced (10, 22, 47, 100, 220, 470nF, etc.) array of 3 values per decade.

- Use the largest capacitor value in the package size
  - This is less well-known, but a popular approach in the EMI design community
  - Rationale: to keep impedance as low as possible, less emphasis on a target impedance and a flat profile

Different Approaches : Comparison

- Approach A : values of decoupling capacitors logarithmically spaced, i.e. 3 values per decade : 10, 22, 47, 100, etc.
- Approach B : largest values of decoupling available in two package sizes, i.e., 0603 and 0402
- Approach B1 : largest values of decoupling available in one package size, i.e., 0402.



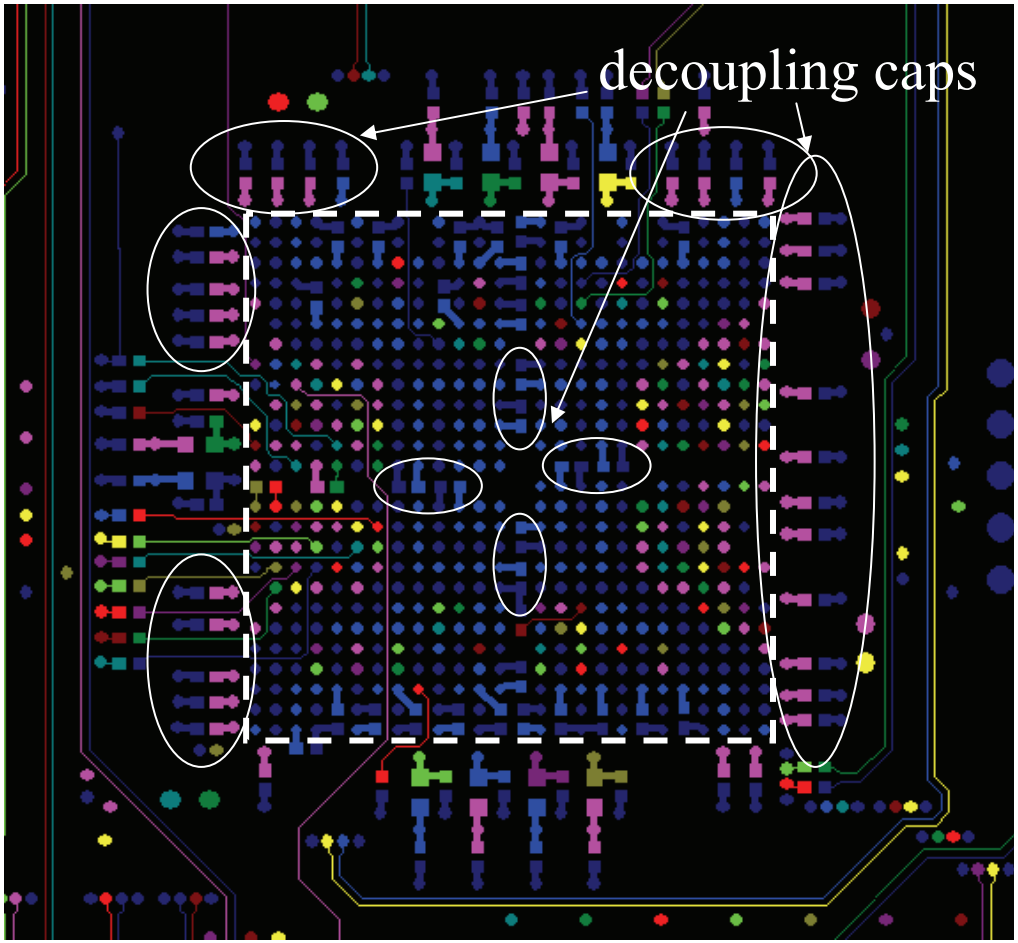
<u>Both</u> approaches can meet the design specs relative to the target impedance

Outline

Capacitor Location

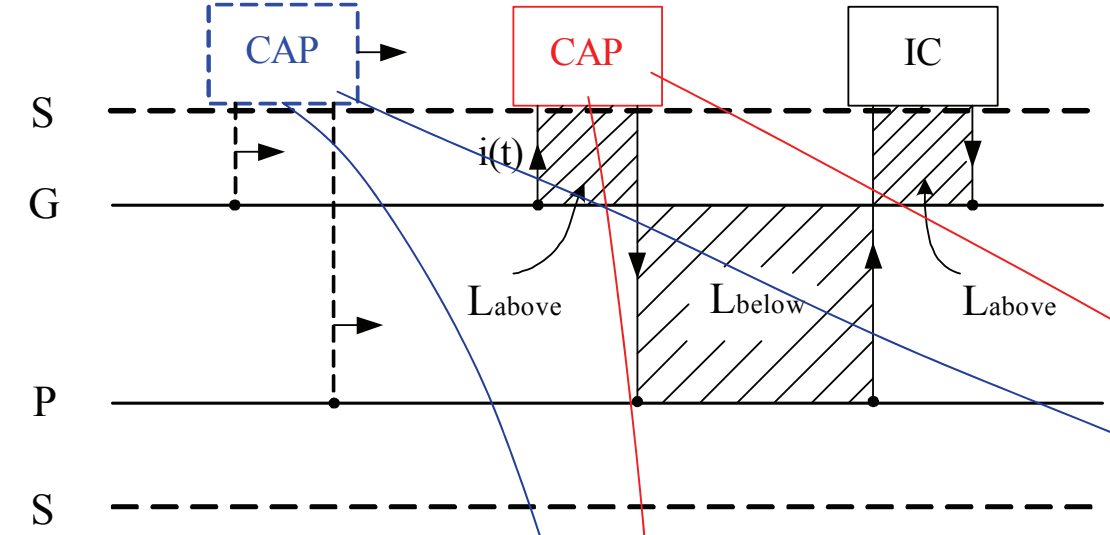
- could be important due to PCB geometry

Background



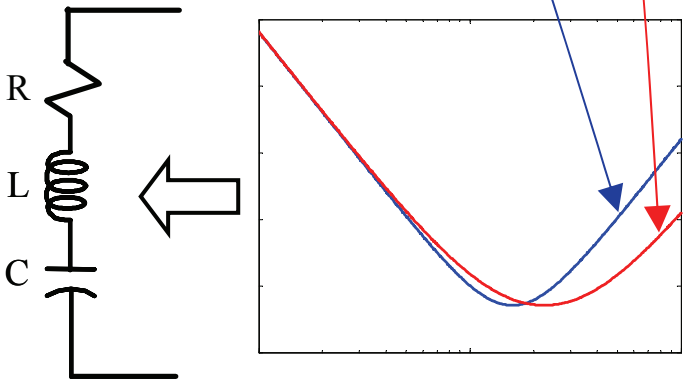
- Does capacitor location matter?
- How close is close?
- What if capacitors can't be placed close enough to the IC pwr/gnd pins?
- Is it worth sacrificing routing or using costly new technology in order to get capacitors closer?
- Need a way to facilitate engineering judgment

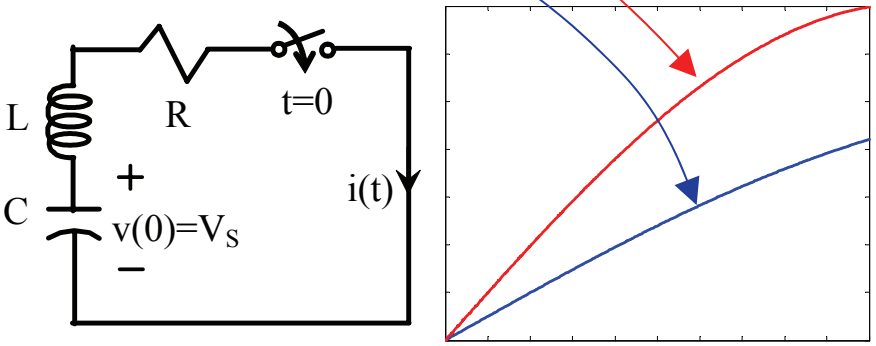
Location Affects Interconnect Inductance



Interconnect inductance is reduced when the cap is moved closer to the IC

⇒ The capacitor becomes more effective



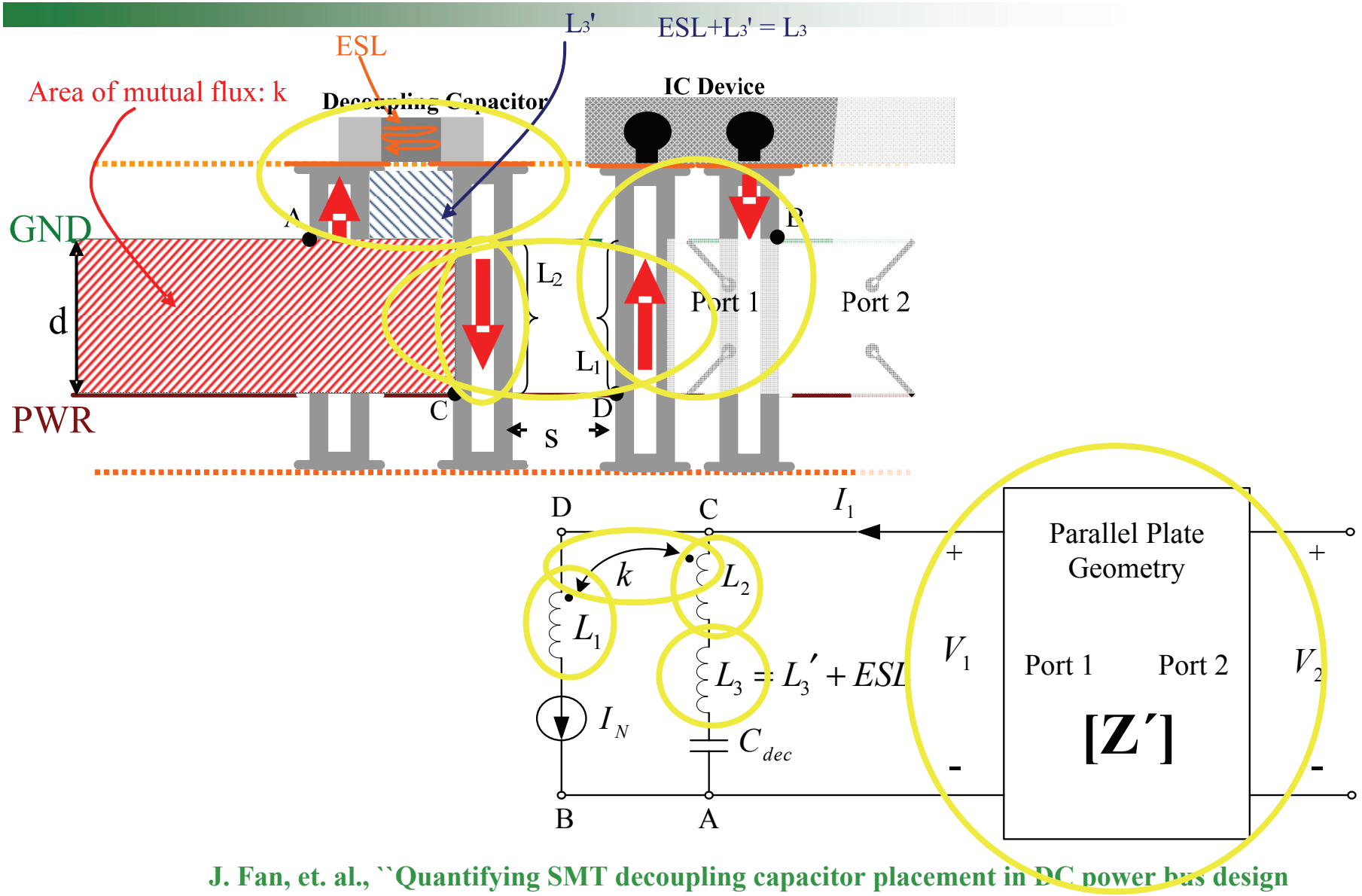


$$Z = R + j\omega L + \frac{1}{j\omega C}$$

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

$$i(t \geq 0) = V_S\sqrt{\frac{C}{L}}\sin(\frac{t}{\sqrt{LC}})$$

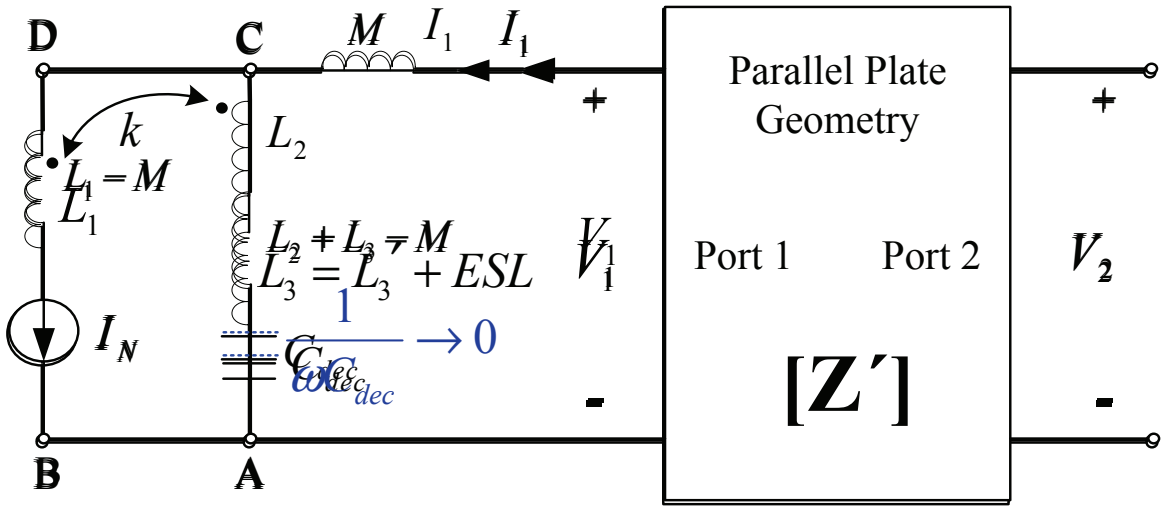
Equivalent Circuit Model



J. Fan, et. al., ``Quantifying SMT decoupling capacitor placement in DC power bus design for multi-layer PCBs,'' *IEEE Transactions on Electromagnetic Compatibility*, Vol. 43, No. 4, pp. 588-599, November 2001.

Local Decoupling Effect – Frequency-Domain

Equivalent circuit at high frequencies



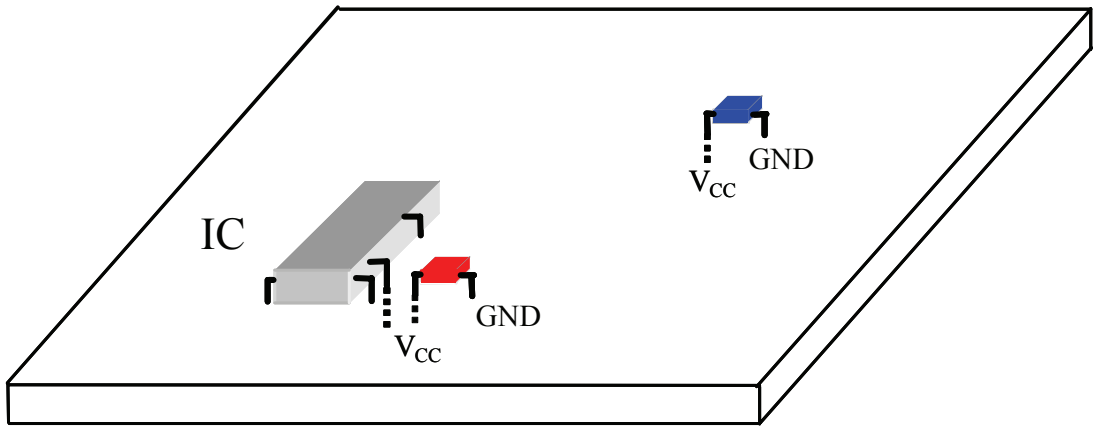
$$Z_{21} = \frac{V_2}{I_N}$$

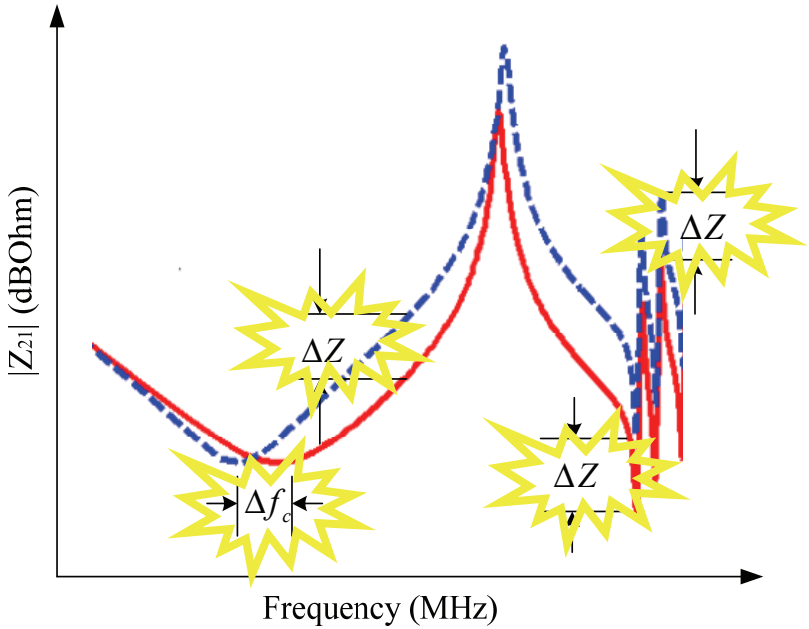
$$Z'_{21} = \frac{V_2}{I_1}$$

$$Z'_{11} = \frac{V_1}{I_1}$$

$$\frac{Z_{21}}{Z'_{21}} = \frac{I_1}{I_N} = \frac{j\omega(L_2 + L_3 - M)}{j\omega(L_2 + L_3) + Z'_{11}} \approx \frac{(1-k) + \frac{L_3}{L_2}}{1 + \frac{L_3}{L_2}}$$

Local Decoupling Effect – Frequency-Domain

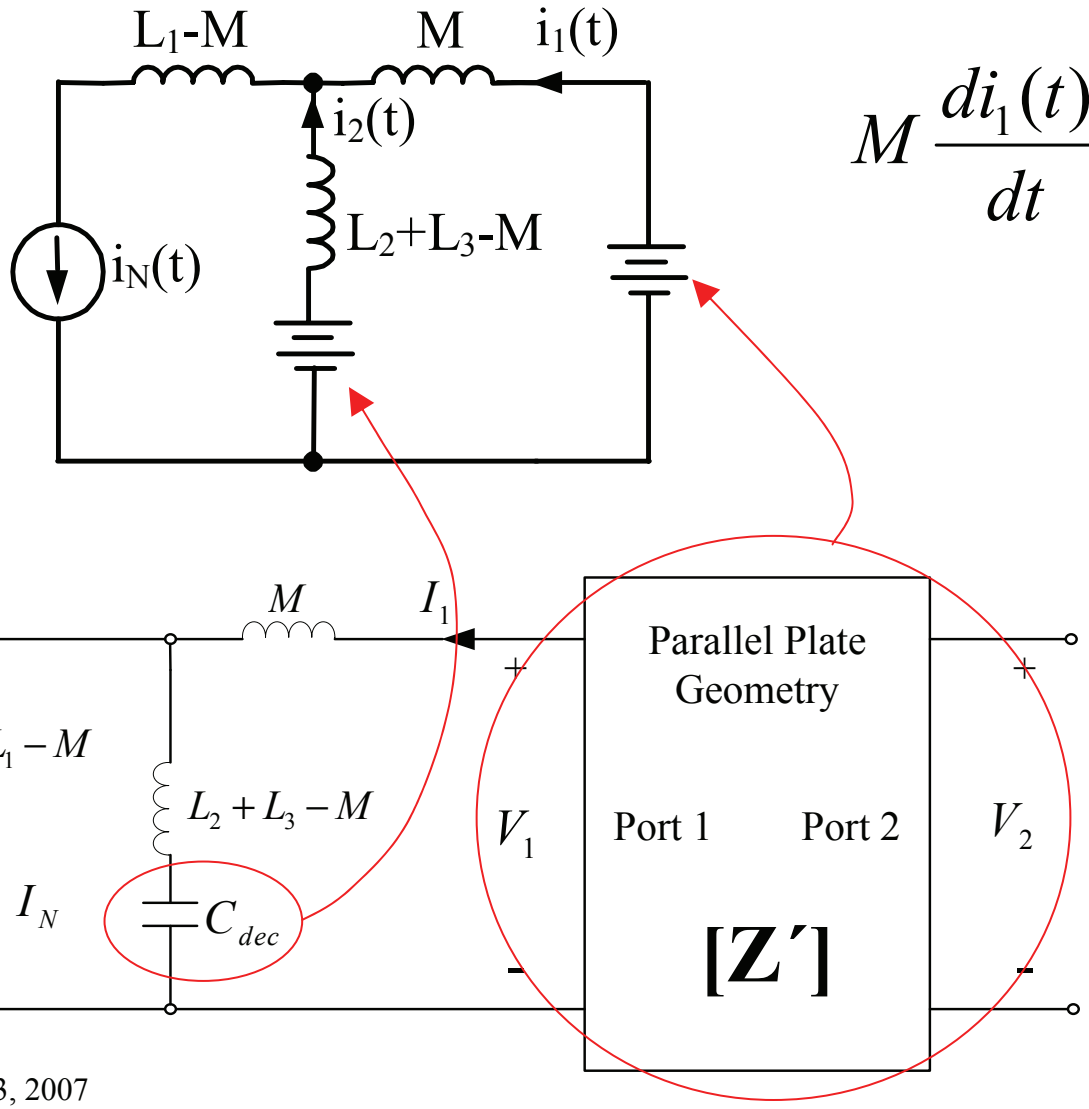




- **Increasing series resonant frequency of decoupling capacitor**
- **Reducing impedance uniformly in a frequency-independent manner (approximately) for frequencies higher than the series resonant frequency**

Local Decoupling Effect – Time-Domain

Equivalent circuit at early time (t≈0)

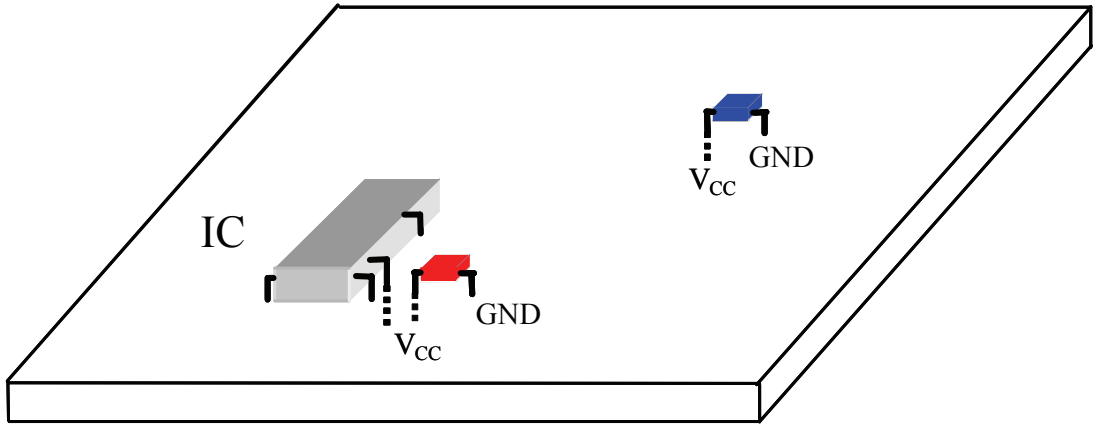


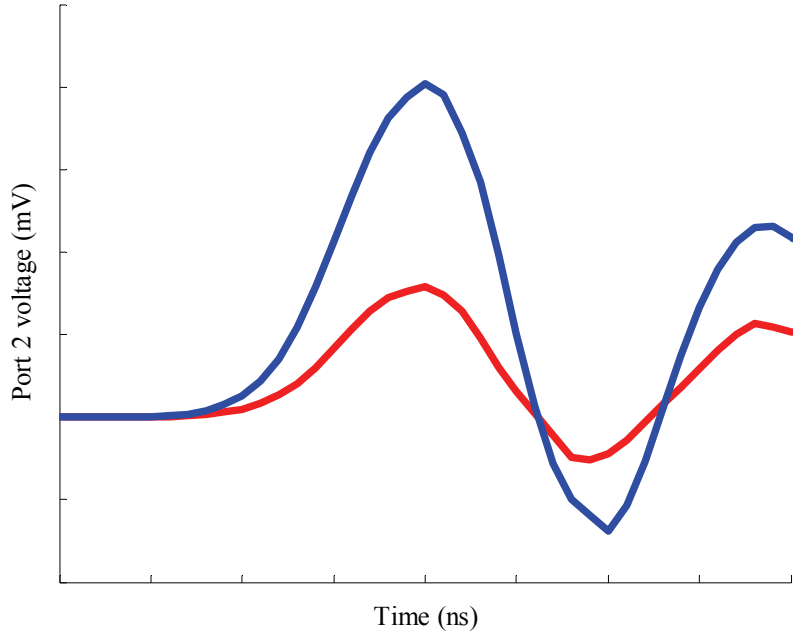
$$M\frac{di_1(t)}{dt} \approx (L_2 + L_3 - M)\frac{di_2(t)}{dt}$$

$$i_1(t) = \frac{L_2 + L_3 - M}{L_2 + L_3} i_N(t)$$

$$\approx \frac{(1-k) + \dfrac{L_3}{L_2}}{1 + \dfrac{L_3}{L_2}} i_N(t)$$

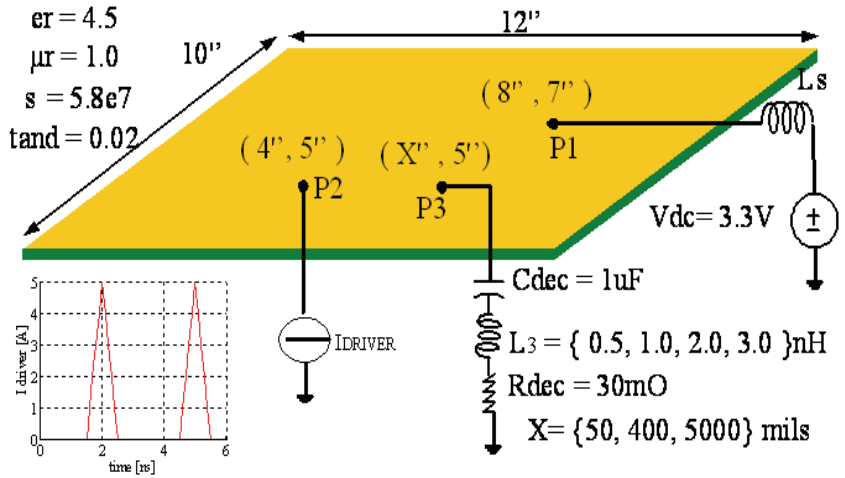
Local Decoupling Effect – Time Domain

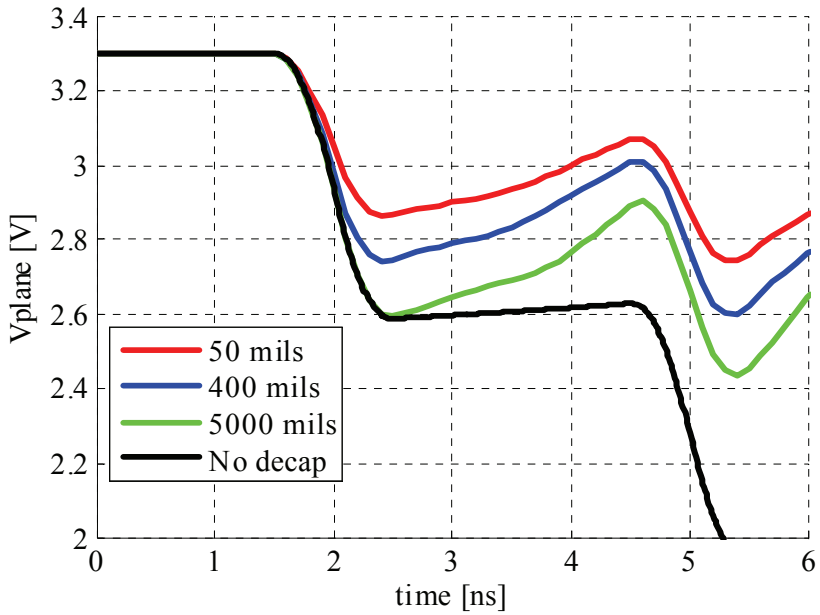




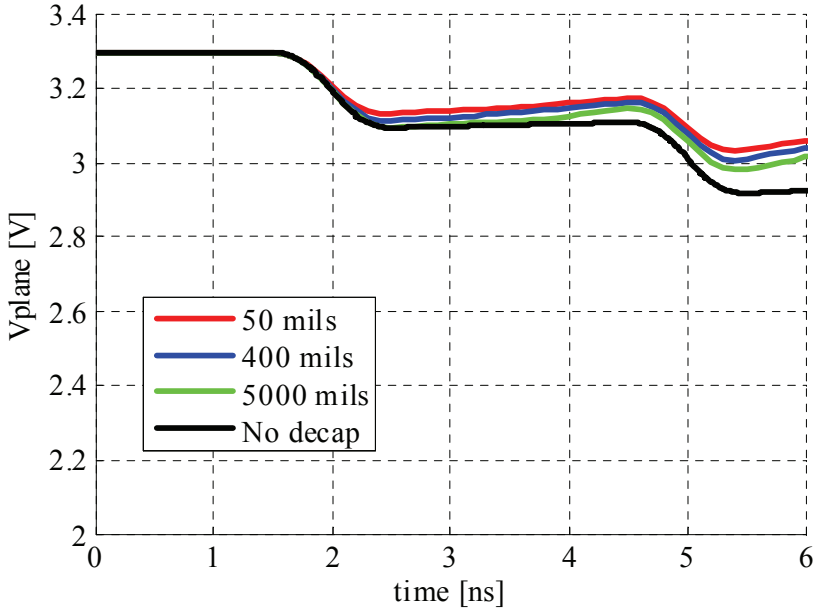
Reducing initial noise voltage generated in the power bus due to logic transitions.

Local Decoupling Effect – Charge Delivery





35 mil thick



10 mil thick

Estimating Local Decoupling Effect

$$\Delta|Z_{21}|(dB) \approx 20\log_{10}\left[\frac{(1-k)+\frac{L_3}{L_2}}{1+\frac{L_3}{L_2}}\right]$$

Closed-form expressions derived from the radial transmission-line theory :

$$L_2 = \frac{\mu_0 d}{2\pi}\left[\ln\left(\frac{R_{equiv}}{r}\right) - 0.75\right] H$$

accounting for fringing effect

$$k \approx \frac{\ln\left(\frac{R_{equiv}}{s+r}\right) - 0.75}{\ln\left(\frac{R_{equiv}}{r}\right) - 0.75}$$

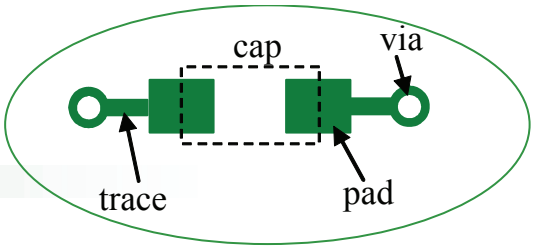
- **d – PWR/GND plane pair spacing**
- **r – via radius**
- **R_{equiv} – equivalent radius of power bus**
- **s – spacing between two vias**

For a rectangular power bus, $R_{equiv} \approx \frac{a+b}{4}$

assumption: vias are located close to the center of the planes

J. Fan, et. al., "Estimating the noise mitigation effect of local decoupling in printed circuit boards," *IEEE Transactions on Advanced Packaging*, Vol. 25, No. 2, pp. 154-165, May 2002.

Estimating Local Decoupling Effect



$$L_3' = L_{via} + L_{trace} \quad \text{where } L_{via} = 2\left(L_{ps} - M_{ps}\right) \text{ and } L_{trace} = L_t - M_t$$

$$M_{ps} = \frac{\mu_0}{2\pi} h_s \left\{ \ln\left[\frac{h_s}{l} + \sqrt{1+\left(\frac{h_s}{l}\right)^2} \right] + \frac{l}{h_s} - \sqrt{1+\left(\frac{l}{h_s}\right)^2} \right\}$$

$$L_{ps} = \frac{\mu_0}{2\pi} h_s \left\{ \ln\left[\frac{h_s}{r} + \sqrt{1+\left(\frac{h_s}{r}\right)^2} \right] + \frac{r}{h_s} - \sqrt{1+\left(\frac{r}{h_s}\right)^2} \right\}$$

$$L_t = \frac{2\times 10^{-7}}{3w^2} \left[\begin{array}{l} 3w^2 l \ln\left(\frac{l+\sqrt{w^2+l^2}}{w} \right) + 3l^2 w \ln\left(\frac{w+\sqrt{w^2+l^2}}{l} \right) \\ -\left(w^2+l^2\right)^{3/2} + l^3 + w^3 \end{array} \right]$$

Validated with CEMPIE

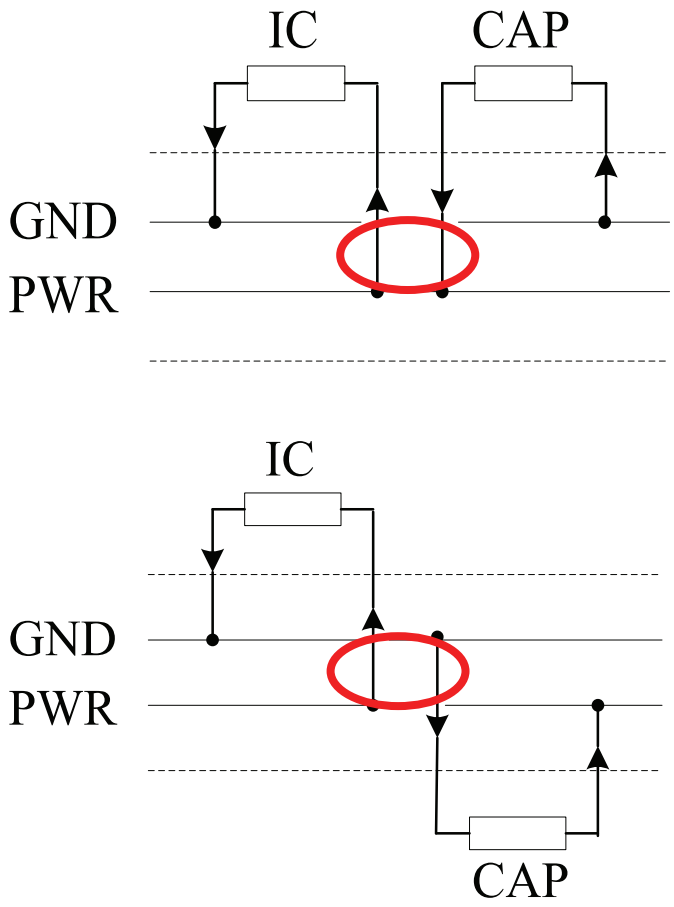
$$M_t = \frac{10^{-7}}{w^2} \left[\begin{array}{l} -\frac{2}{3}\left(w^2-2p^2+l^2\right)\sqrt{w^2+p^2+l^2} \\ +l\left(w^2-p^2\right)\ln\left(\frac{l+\sqrt{w^2+p^2+l^2}}{-l+\sqrt{w^2+p^2+l^2}} \right) \\ +\frac{2}{3}\left(w^2-2p^2\right)\sqrt{w^2+p^2} \\ +l^2 w \ln\left(\frac{w+\sqrt{w^2+p^2+l^2}}{-w+\sqrt{w^2+p^2+l^2}} \right) \\ -4wpl\cdot\tan^{-1}\left(\frac{wl}{p\sqrt{w^2+p^2+l^2}} \right) \\ +\frac{2}{3}\left(l^2-2p^2\right)\sqrt{l^2+p^2} \\ +p^2 l \ln\left(\frac{l+\sqrt{l^2+p^2}}{-l+\sqrt{l^2+p^2}} \right) + \frac{4p^3}{3} \end{array} \right]$$

l: separation between two via;
h_s: height of the capacitor from the nearest power or ground plane ;
w: width of the trace connecting two vias, or width of the capacitor package if no trace ;
r: radius of the via ; and $p = 2h_s$.

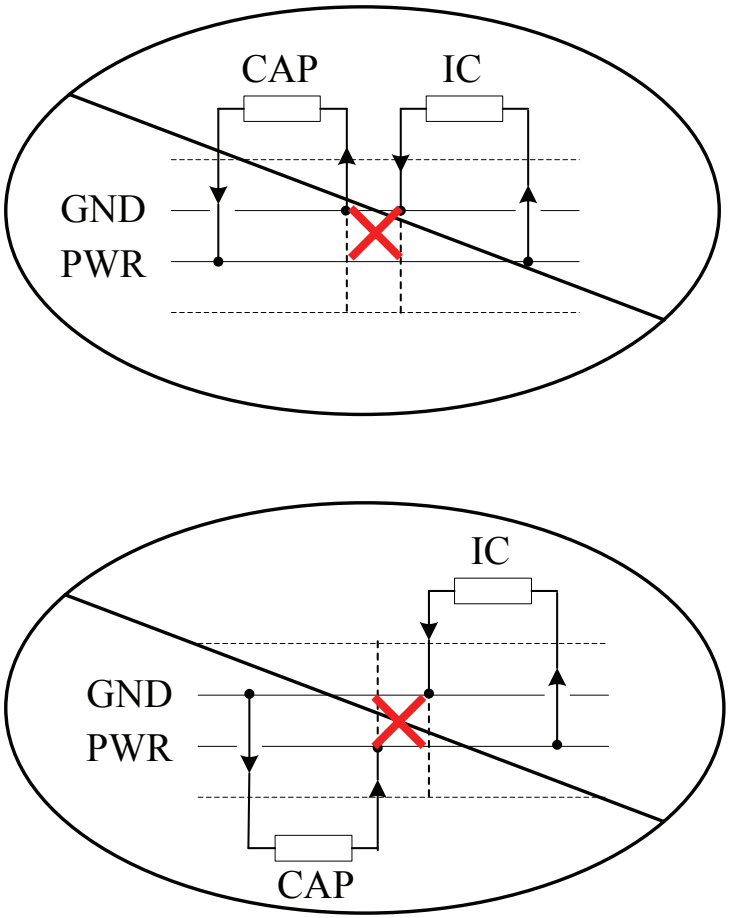
C. Wang, et. al., "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductances," *IEEE Transactions on Advanced Packaging*, Vol. 29, No. 2, pp. 320-334, May 2006.

Design Implications

Dos



Don'ts



J. L Knighten, B. Archambeault, J. Fan, et. al., "PDN Design Strategies: II. Ceramic SMT Decoupling Capacitors – Does Location Matter?," *IEEE EMC Society Newsletter*, Issue No. 207, Winter 2006, pp. 56-67.

Design Implications

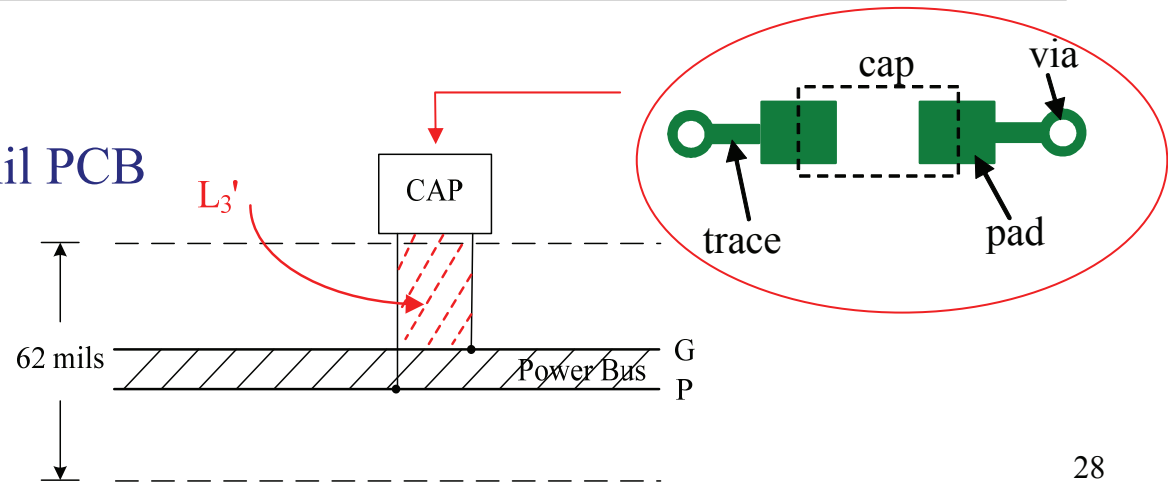
The ratio of L_3/L_2

- A good indicator of the ability of a power bus to support local decoupling
- The lower, the better
- Can be greatly increased by even very short trace length from via to pad

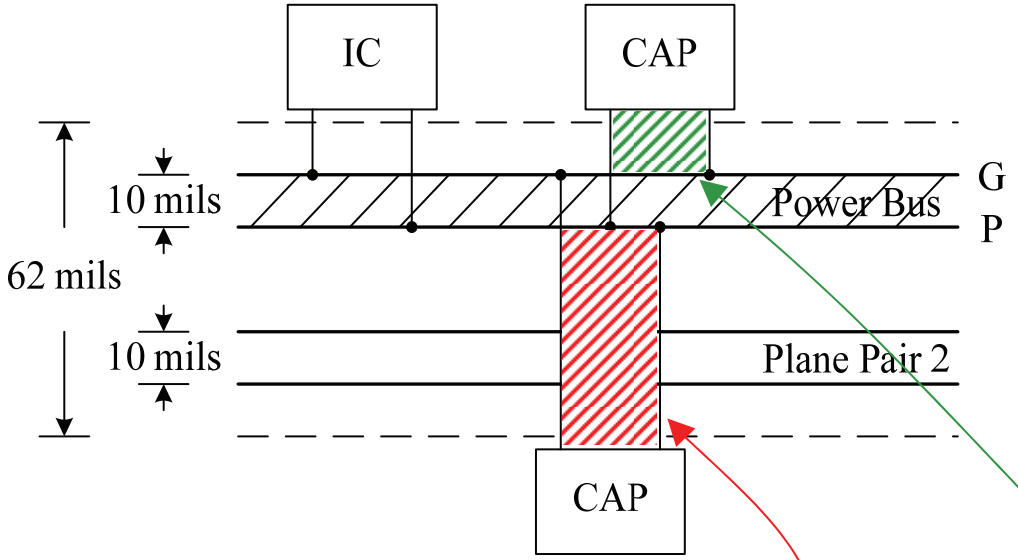
PWR/GND pair thickness	L_3' (nH)	L_3/L_2 with no trace	L_3/L_2 w/extra 100 mil trace length	L_3/L_2 w/extra 200 mil trace length	L_3/L_2 w/extra 300 mil trace length
10 mils	1.66	6.75	9.13	11.50	13.88
35 mils	0.92	1.29	1.98	2.67	3.36

Tabulated values for

- Centered power bus in a 62-mil PCB stack-up
- 10 mil via diameter
- 0603 SMT capacitor package



Design Implications



The placement of de-cap (obverse or reverse), can be highly dependent on the position of power bus in PCB stack-up.

Always LEAST above-plane inductance!

SMT de-cap Placement	L_3' (nH)	L_3/L_2
Obverse	0.45	2.96875
Reverse	2.56	9.5625

Outline

Power/Ground Plane Pair

- thin is always better

Impedance of the Power/Ground Plane Pair

Based on the cavity method:

Low frequency capacitive term

Location

Port Dimensions

$$Z_{ij}(\omega) = \frac{1}{j\omega C_{plane}} + j\omega\mu d\left[\sum_{m=0}^{M}\sum_{n=0}^{N}\frac{\varepsilon_n^2\varepsilon_m^2}{\left(k_{nm}^2 - k^2\right)ab}_{m=n\neq 0} f\left(x_i, x_j, y_i, y_j\right) p\left(L_{xi}, L_{xj}, L_{yi}, L_{yj}\right) + j\omega L_{ij}^{HM}\right]$$

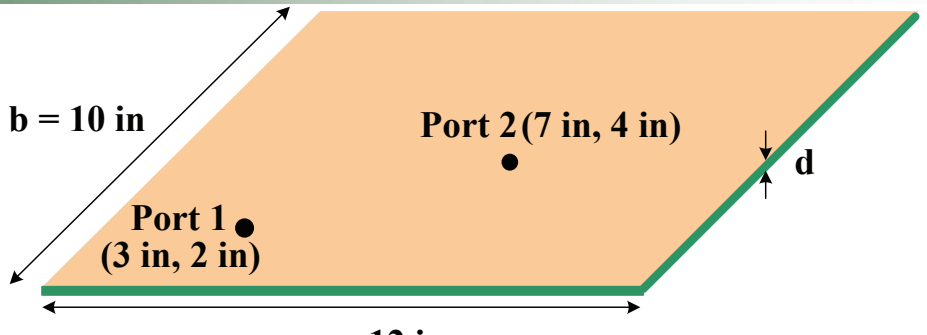
Resonant frequency contributions

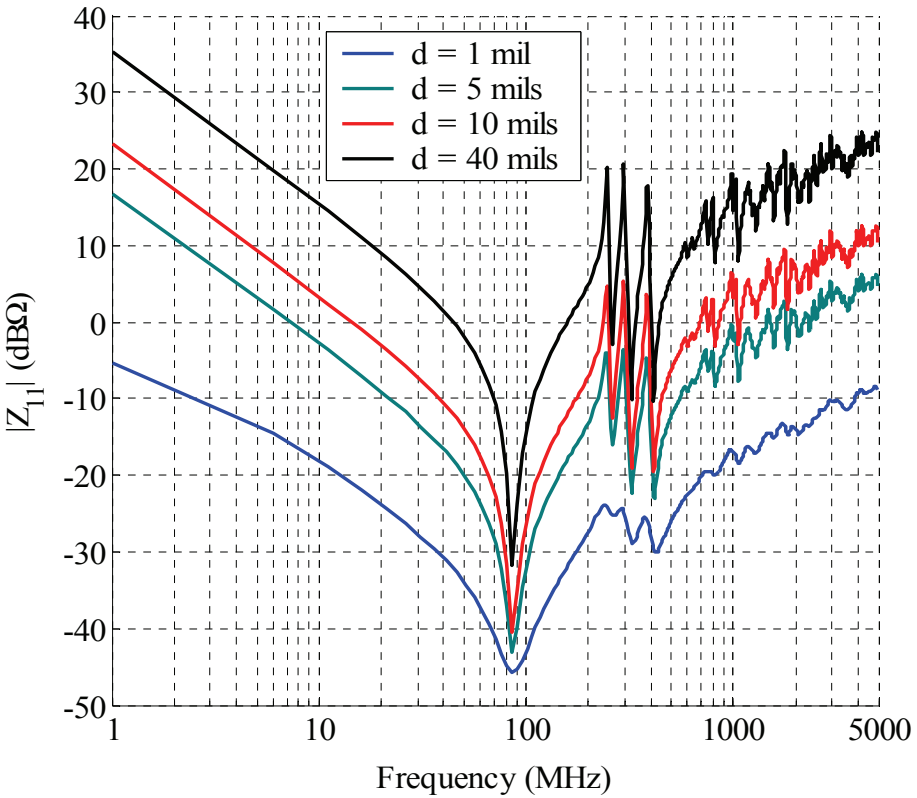
Higher order mode L exists only when i = j

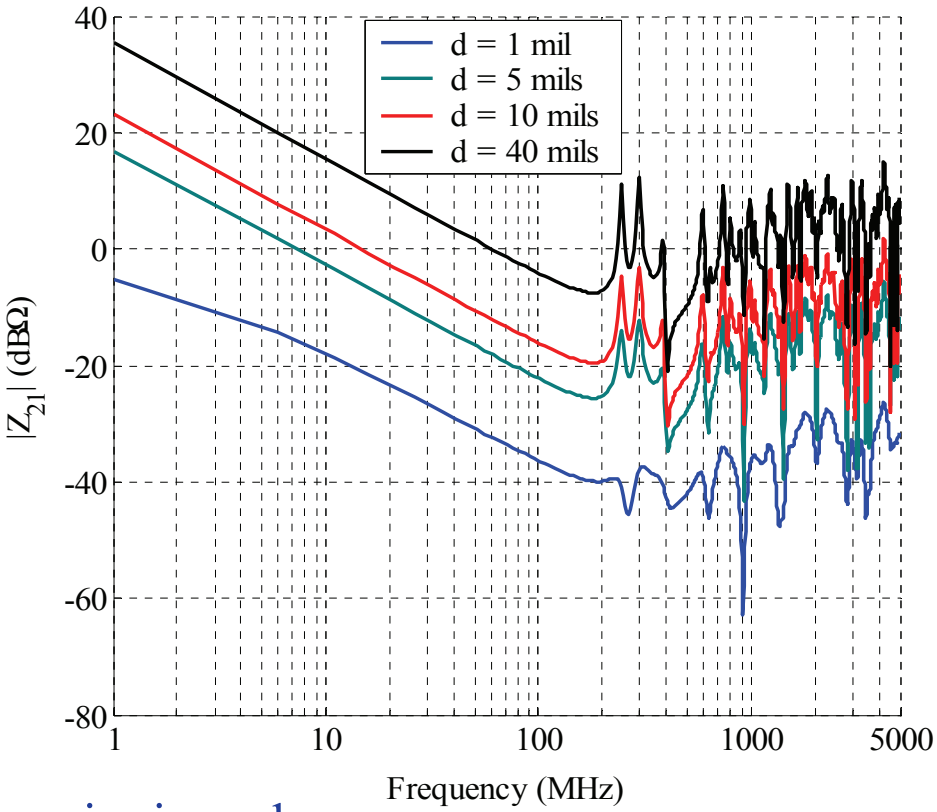
$$Z_{ij}(\omega) \propto d$$

C. Wang, et. al., "An efficient approach for power delivery network design with closed-form expressions for parasitic interconnect inductances," *IEEE Transactions on Advanced Packaging*, Vol. 29, No. 2, pp. 320-334, May 2006.

Power Bus Thickness Effects on Decoupling



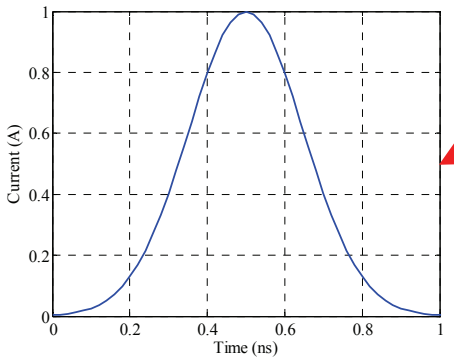


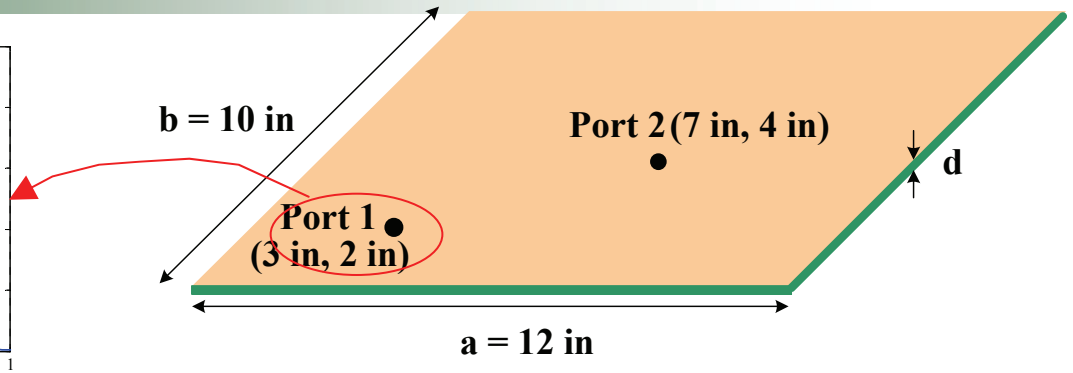


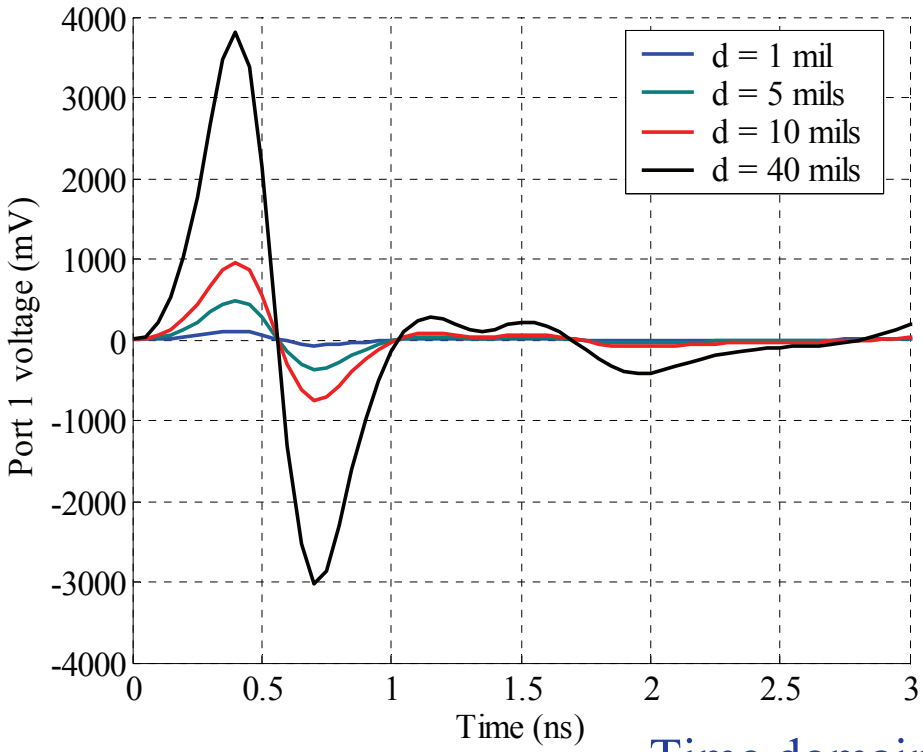
Frequency domain: impedance

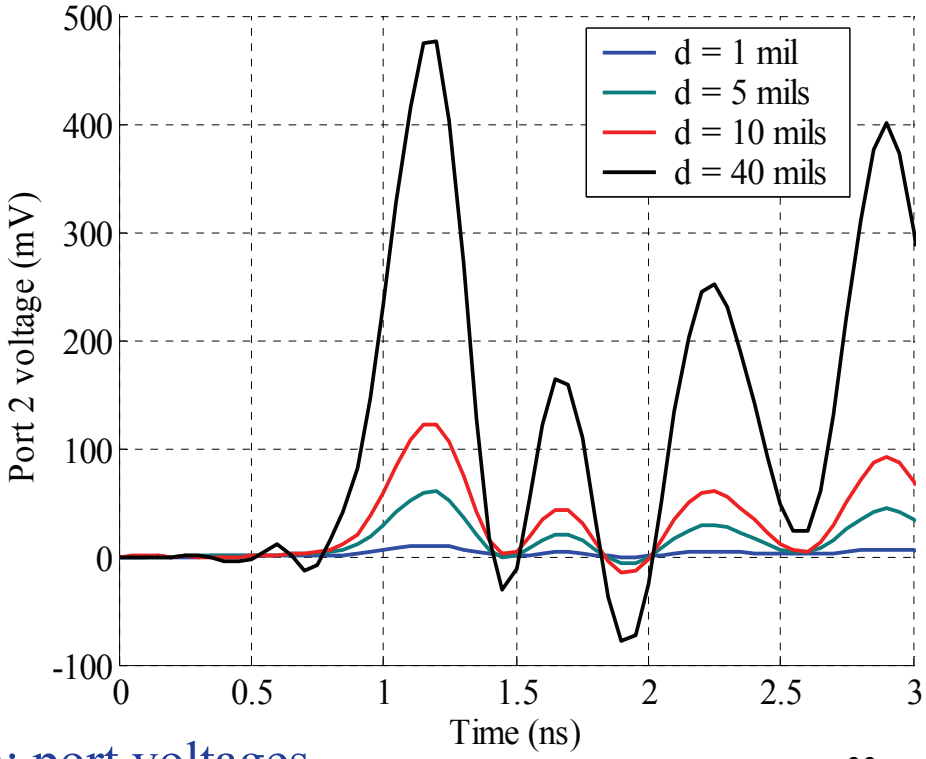
Power Bus Thickness Effects on Decoupling

port 1 current



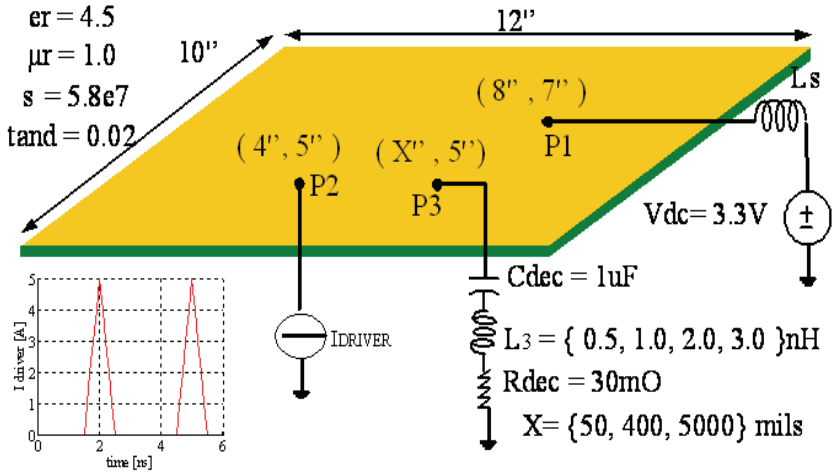


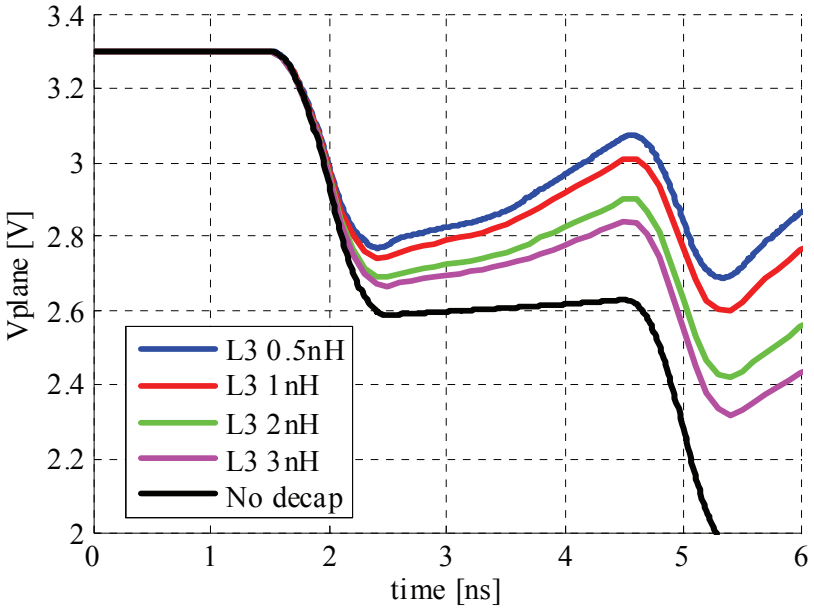




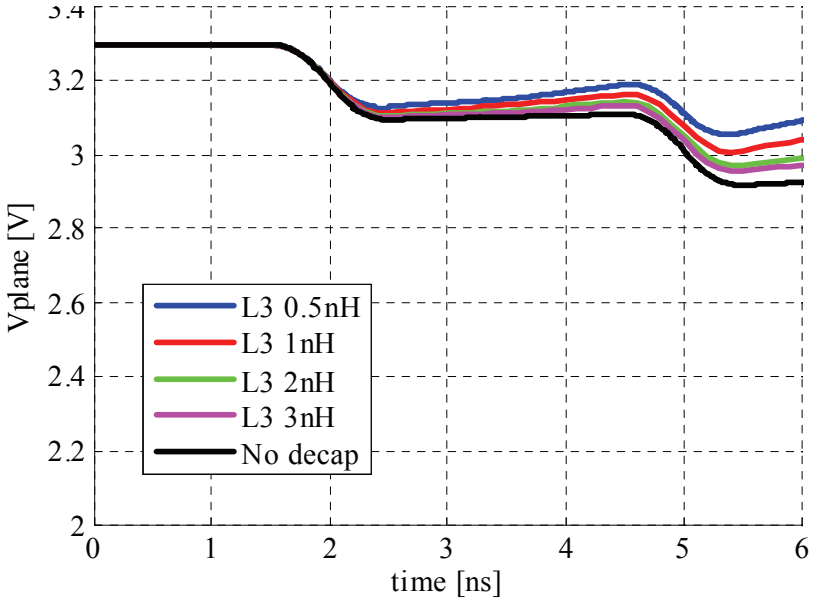
Time domain: port voltages

Power Bus Thickness Effects on Decoupling





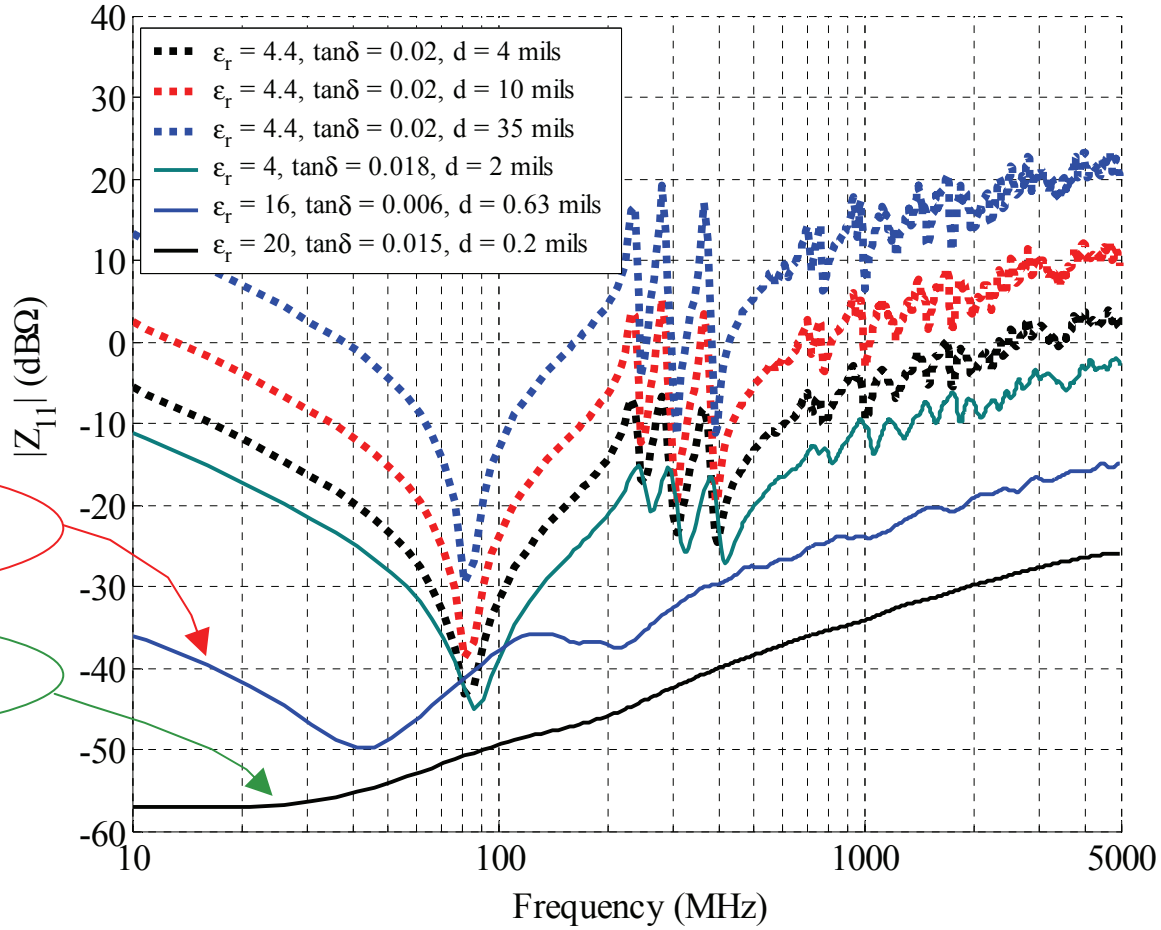
35 mil thick



10 mil thick

Effect of Typical Laminates on Decoupling

Dk	Loss Tangent	Thick-ness, d	Comment
4.4	0.02	4, 10, 35 mils	better quality fiberglass/ epoxy resin material
4	0.02	2 mils	patented thin FR4 core, widely used.
16	0.006	16 microns (0.63 mils)	ultra-thin material commercially available
20	0.015	0.2 mils	ultra-thin material from [7, 8].



Embedded capacitance (thin laminate) has superior electrical performance

Summary

- **Interconnect inductance shall be minimized in any situation:** inductance limits the effectiveness of decoupling
- **Individual capacitor values may not matter:** using an array of capacitor values or the largest value in a package size meets design specifications
- **Capacitor location could be important due to PCB geometry**: thin power bus structures (< 10 mils) usually result in a larger L_3/L_2 value; thus capacitor location is relatively unimportant. Thick power bus structures usually result in a smaller (L_3/L_2) value, and capacitor placement can be an important design factor
- **Thin power/ground plane pair is always better:** low impedance and high charge availability