Relationship Between Signal Integrity and EMC

Presented by

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What is Signal Integrity (SI)?

Signal Integrity ensures that:

- Signal quality is maintained from a driver to a receiver
- Interference between two or more signals doesn't degrade the signal
- The signals don't damage any devices
- Power distribution network (PDN) integrity is maintained
- Timing margins are achieved

Differences between SI and EMI (Emissions)

EMI	SI
Frequency domain	Time domain
Voltage/current spectrum for conducted emissions. Current spectrum and radiated field spectrum for radiated emissions	Voltage waveform
More attention is given to the clock and I/O signals	All high-speed signals are analyzed
Common mode noise is of prime interest	Common mode noise is not that important
Noise levels of concern are in μA and μV	Noise levels of concern are in mA and mV
Simulation is not popular. Design is based on rule of thumbs, empirical formulas	Analysis based on simulations is quite common

Differences between SI and EMI (Emissions)

EMI	SI
Filters are used on clocks and I/Os	Can have negative impact on SI performance
Clock/high-speed circuitry placement with respect to the I/O circuitry	May not be as important
Clock traces are routed away from the edge of the board	No such requirement
I/O connectors should not be placed on the opposite sides of the board	No such requirement
Ground flooding on signal layers	No such requirement
No clock/high-speed traces between the I/O connector and the I/O circuitry	No such requirement

Differences between SI and EMI (Emissions)

EMI	SI
No clock traces on the surface layers	No such requirement
Ground via fence around the edge of the board	No such requirement
Decoupling caps need to be spread on the board	No such requirement
Heatsink grounding	No such requirement
PCB mounting holes to ground	No such requirement
Avoid having clocks with overlapping clock harmonics. Use of spread spectrum clocks.	No such requirement

Why is Signal Integrity (SI) Needed?

Technology Drivers

- Lower driver voltages
- Increased circuit density
- Faster edge rates
- Higher data rates and clock frequencies
- Longer signal paths

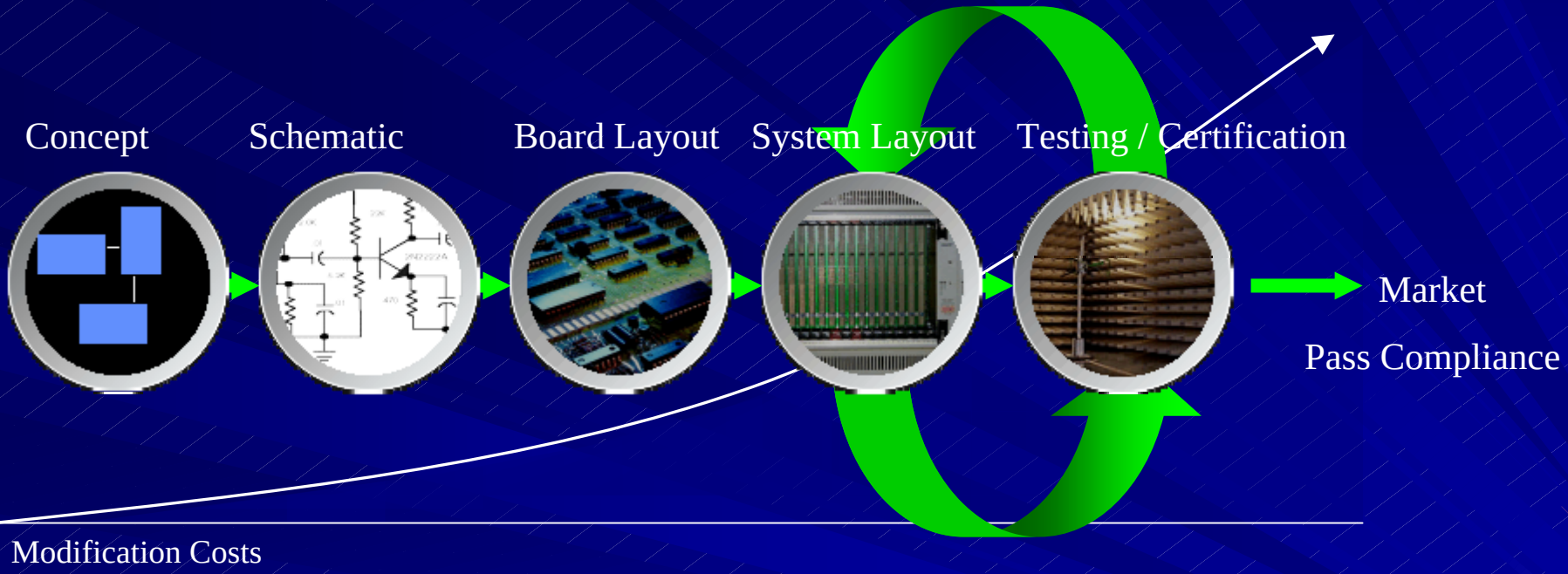
Interconnects affect signal quality!

Benefits of SI

- Shorter and more predictable design cycle time
- Reduced time for prototype testing and redesign
- Reduced EMI
- Shorter time to market

As a general rule of thumb, SI analysis is required for signals with rise/fall time of less than 1 ns or with frequency 100 MHz or higher.

Electronic System Design



Signal Quality

Signal quality is affected by any impedance discontinuity that exists in the interconnect between the driver and the receiver.

Examples of Impedance Discontinuities:

- A change in the trace-width
- Changing reference planes
- A gap in the reference plane
- Connectors
- A branch, tee or stub
- Vias
- Components connected on a trace

Signal Quality

Signal quality is affected by any losses that exist in the interconnect between the driver and the receiver.

Examples of Losses introduced in the interconnects:

- Skin effect loss
- Dielectric loss

Lumped vs Distributed

L = T x v

L = Length of the rising edge (inches)
T = 10-90% rise time, ps
V = Velocity, in/ps

Interconnect size < L / 6	Lumped
Interconnect size > L / 6	Distributed (transmission line)

Need for Simulations in SI Analysis

- Reduces the risk of failure
- Enables the SI engineer to evaluate what-if scenarios early on in the design cycle
- Provides information to justify design changes and verify effectiveness
- Reduces time to market

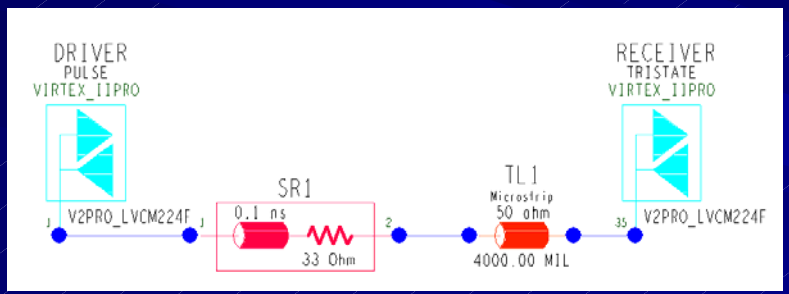
Device Modeling - IBIS

- IBIS – I/O Buffer Information Specification
- A vendor-independent format for driver/receiver modeling
- Like a black box model of a device. Internal working of the device circuitry is hidden. Useful for SPICE-like simulators.
- Has V-I and V-t curves. Package parasitics can be included.
- Simulation time is smaller as compared with the transistor based SPICE models.

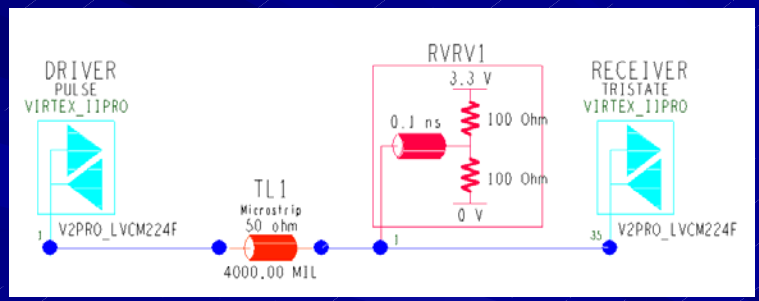
Termination Schemes

Impedance discontinuities lead to reflections. Different termination schemes are employed to reduce long-line reflections and short-line ringing.

Some examples of most commonly used termination schemes:

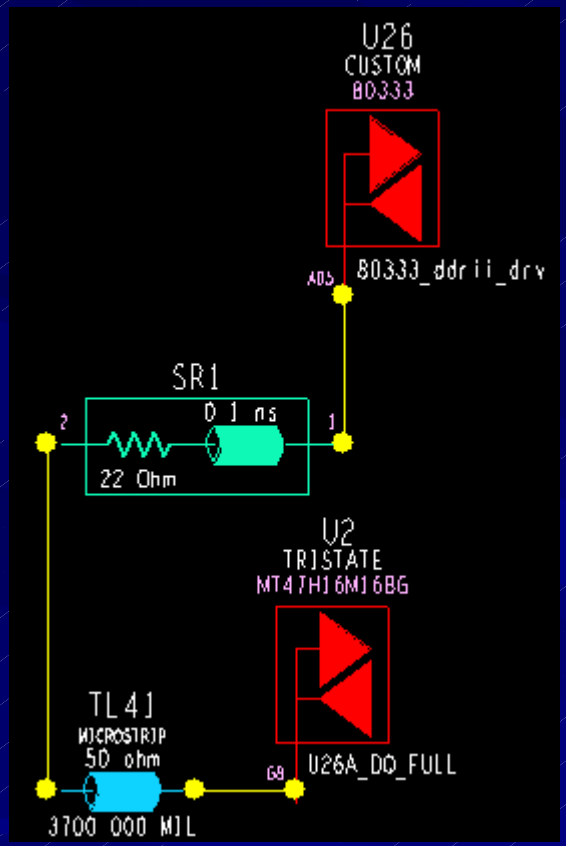


Series Termination



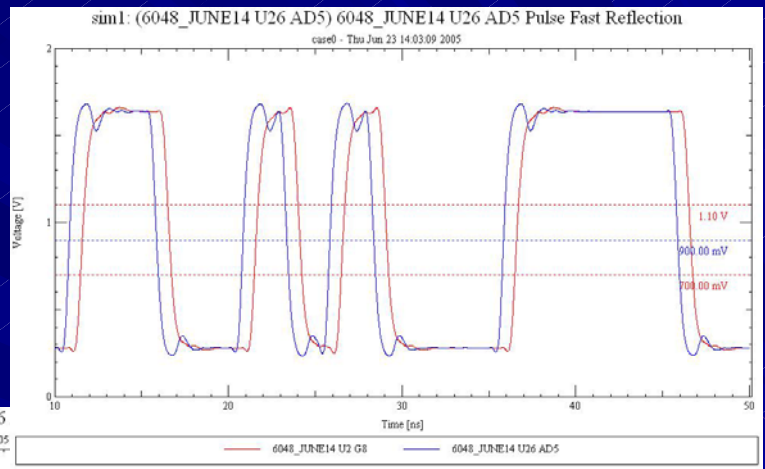
End Termination

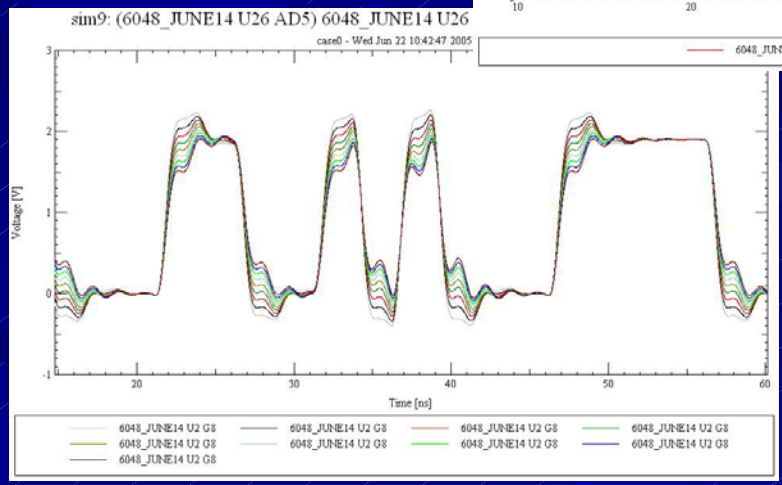
Reflection Simulation



Solution Space Analysis

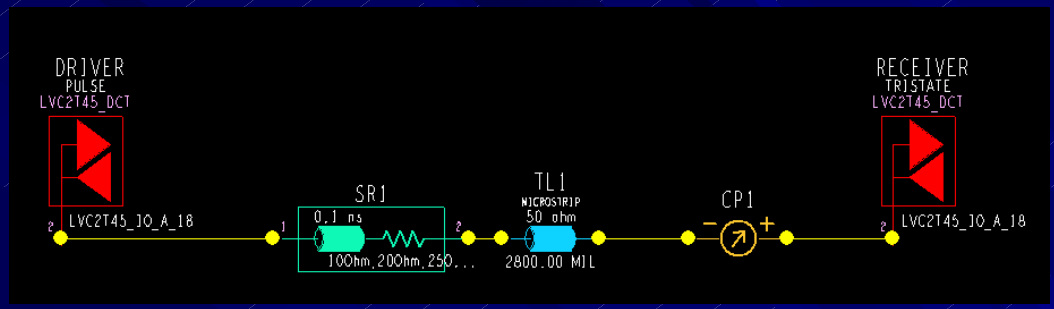
Component speed, trace impedance, terminator value, trace length

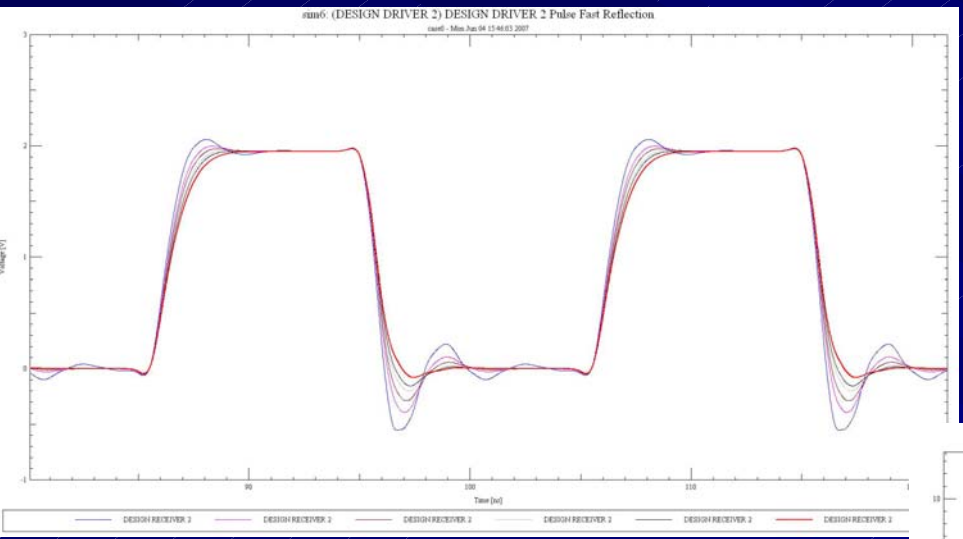




EMI Impact

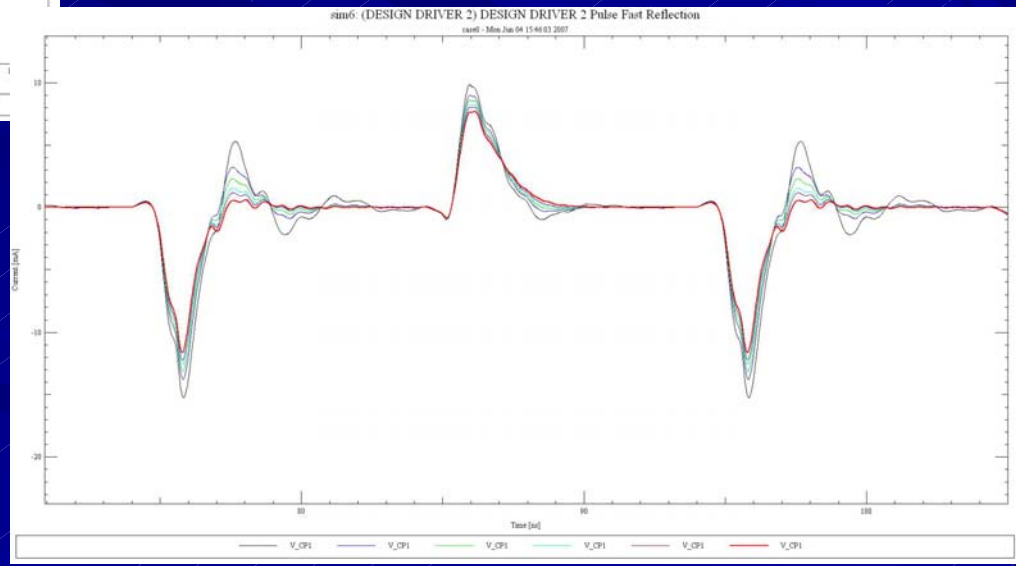
- SI analysis focuses on a voltage waveform.
- From an EMI perspective the current waveform is more critical.
- Some of the intentional current flowing over the interconnects gets converted into a common mode current on a PCB.
- A reduction in the intentional current also leads to a reduction in the common mode current.
- A termination scheme can be selected which can minimize the level of intentional current over an interconnect while at the same time providing an acceptable voltage waveform at the receiver.
- For example, a series termination is better than an end termination. Also, the series termination resistor value can be optimized for lower intentional current and acceptable voltage waveform.



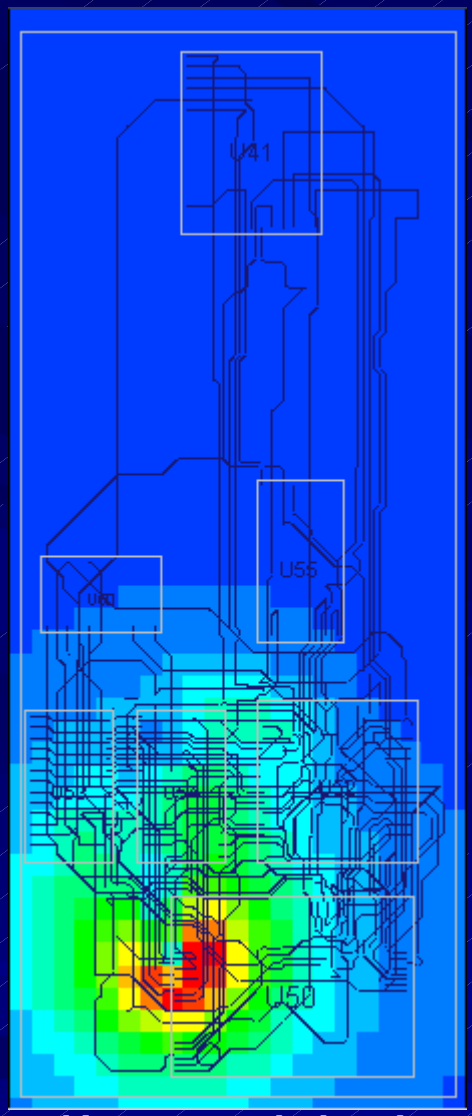


Voltage waveform

Current waveform

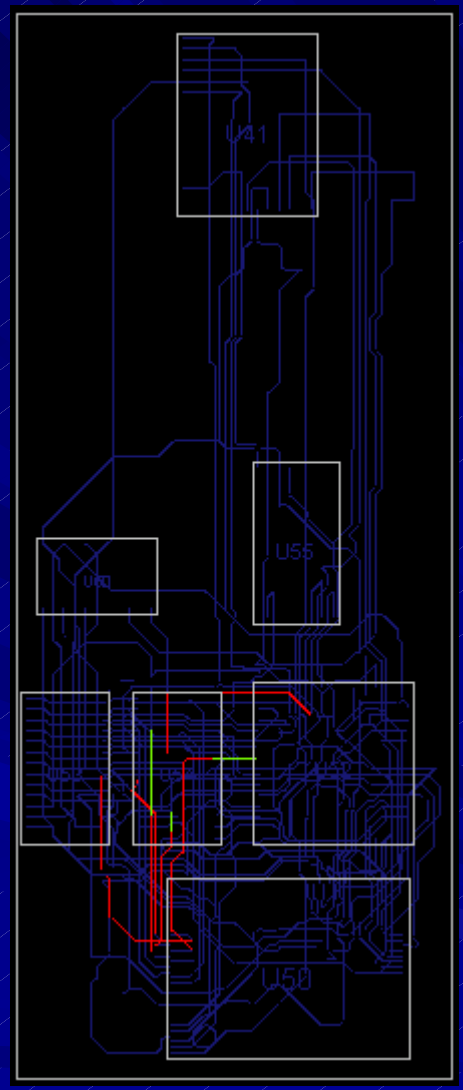


Radiation from Noise Currents



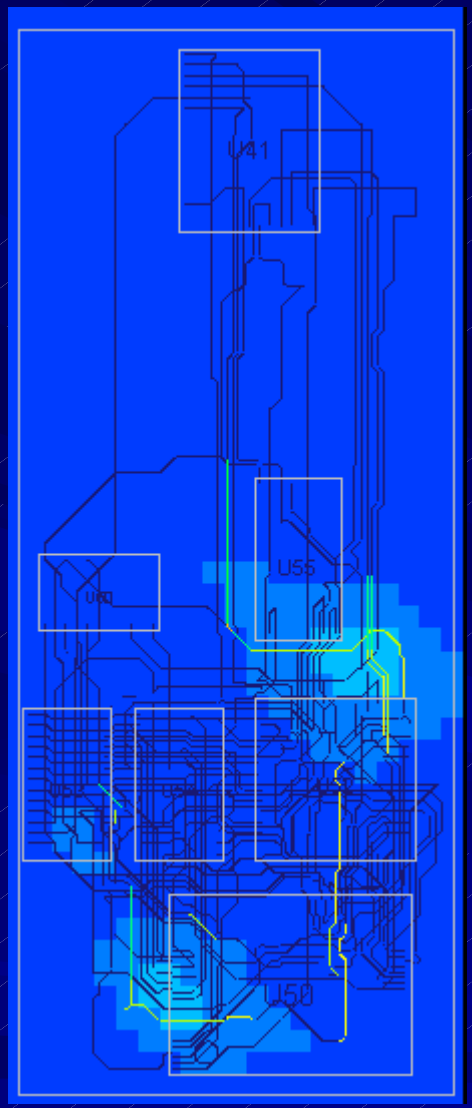
Problem area on the board
(Near-field magnetic field scan)

Before
fixing
the problem



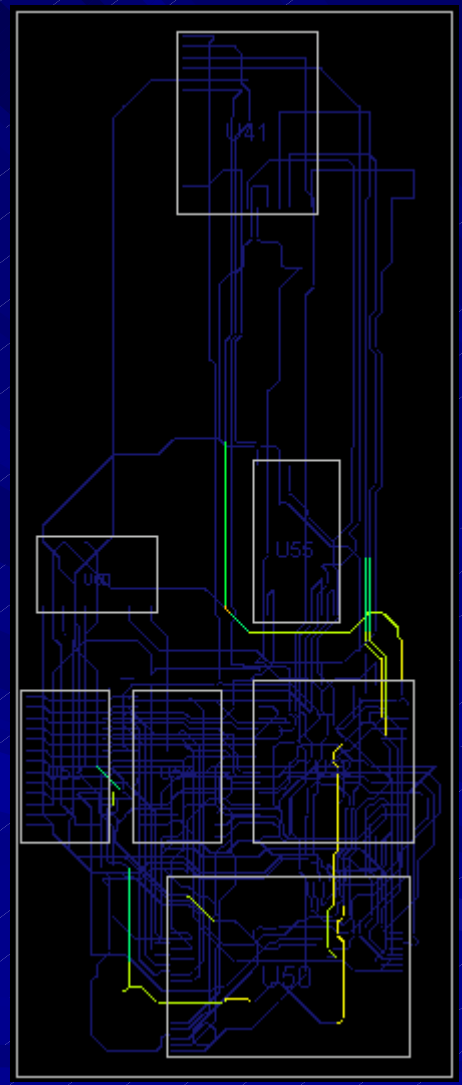
Problem nets on the board
(Level of noise current)

Radiation from Noise Currents



Problem area on the board
(Near-field magnetic field scan)

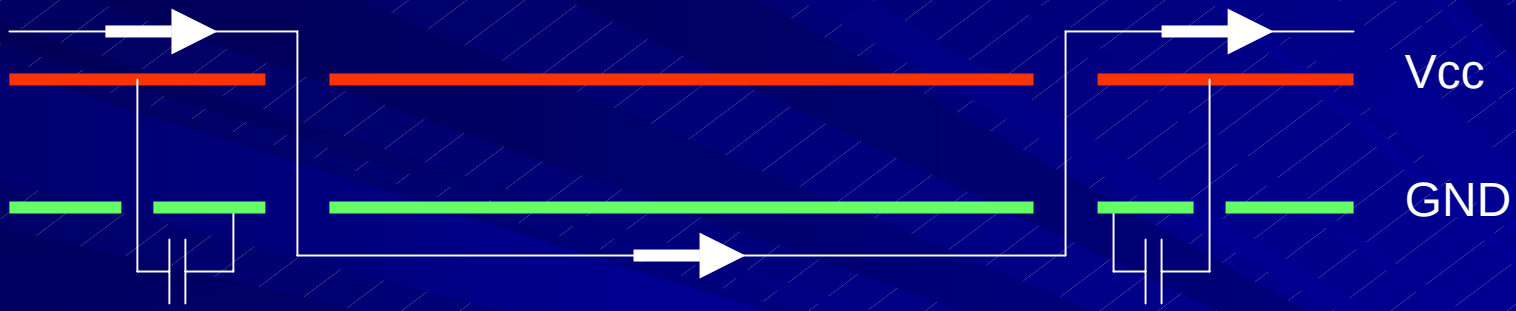
After fixing the problem (added termination resistors on problem nets)



Problem nets on the board
(Level of noise current)

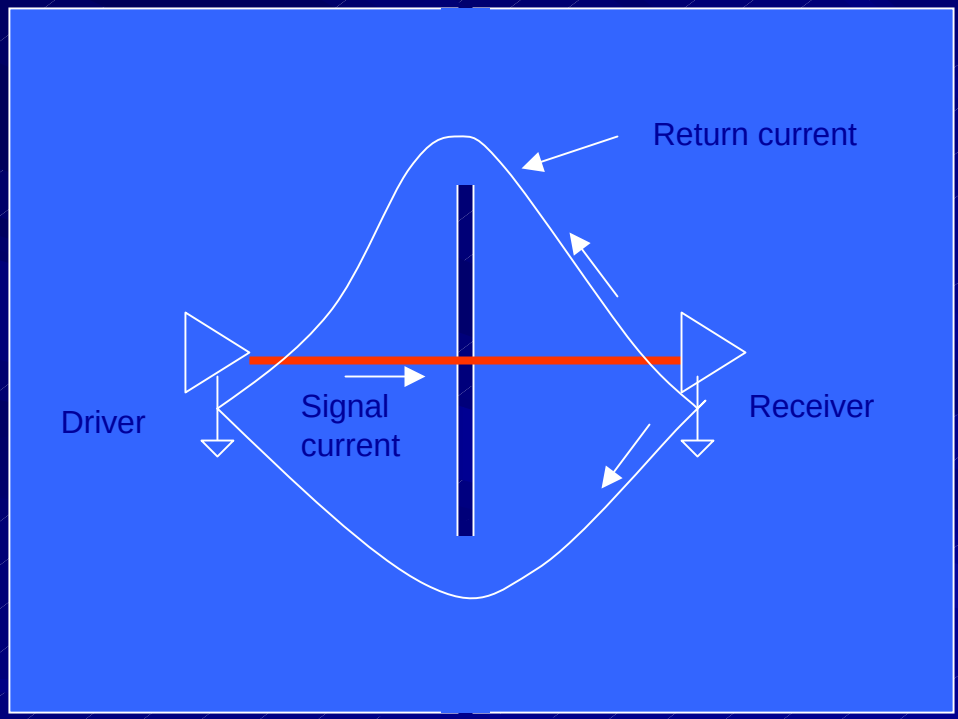
Changing Reference Planes

Impacts both SI and EMI



A Gap in the Reference Plane

Impacts both SI and EMI

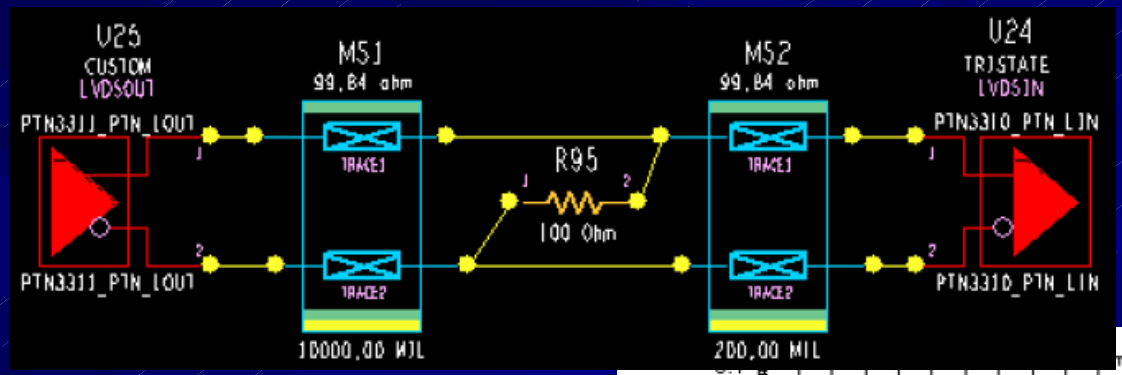


Slots in the reference plane add inductance to the traces.

Reflection Simulation

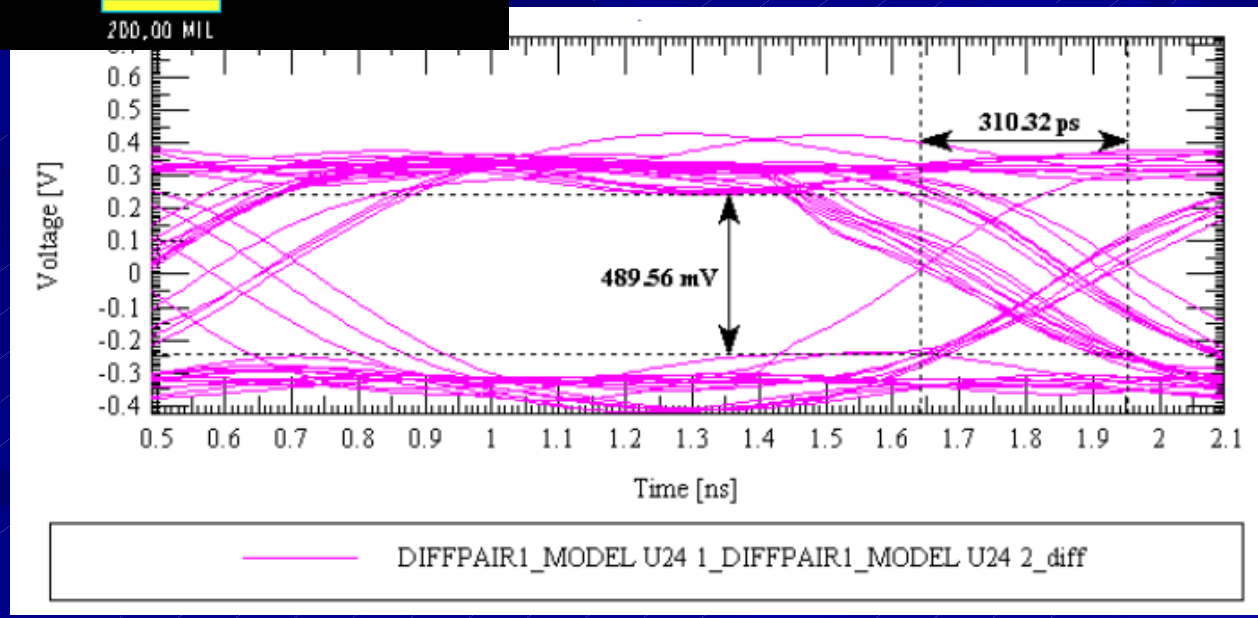
Solution Space Analysis

Component speed, trace impedance, terminator value, trace length

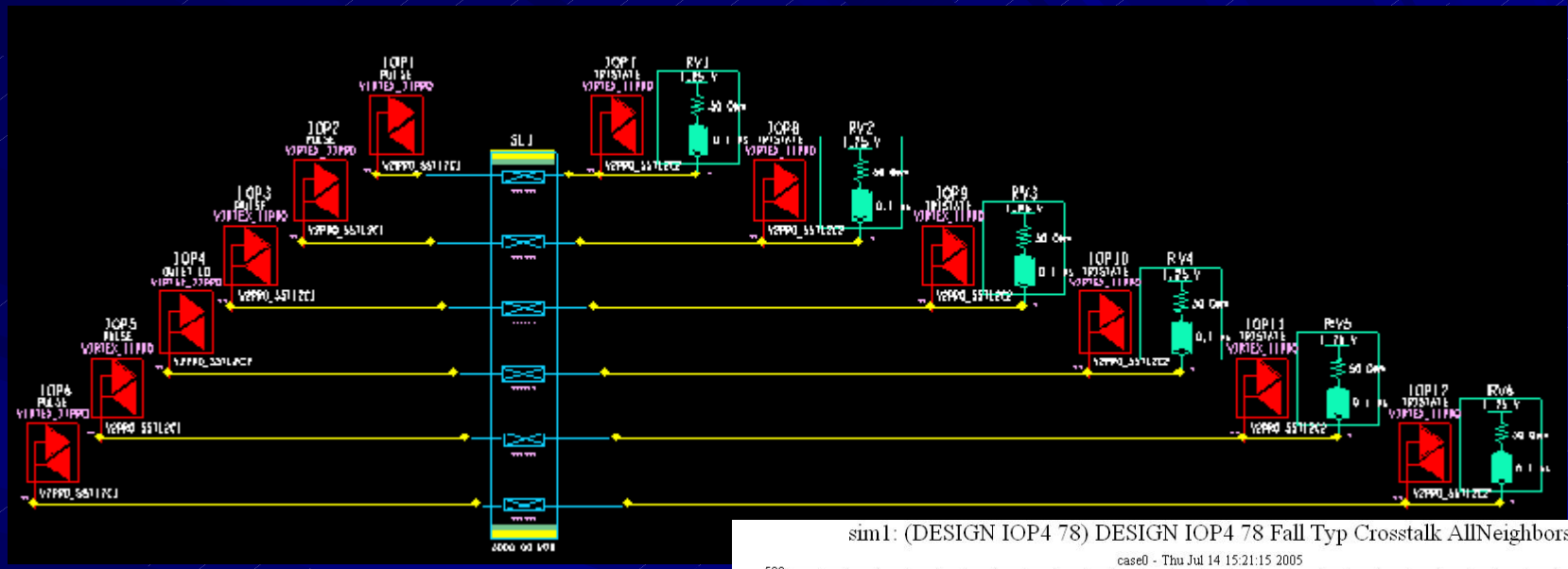


1. Differential Signaling improves noise immunity.
2. Solves the ground bounce problem.
3. Need to reduce skew within the differential pair. Any skew within the differential pair leads to common mode noise.

Eye Diagrams

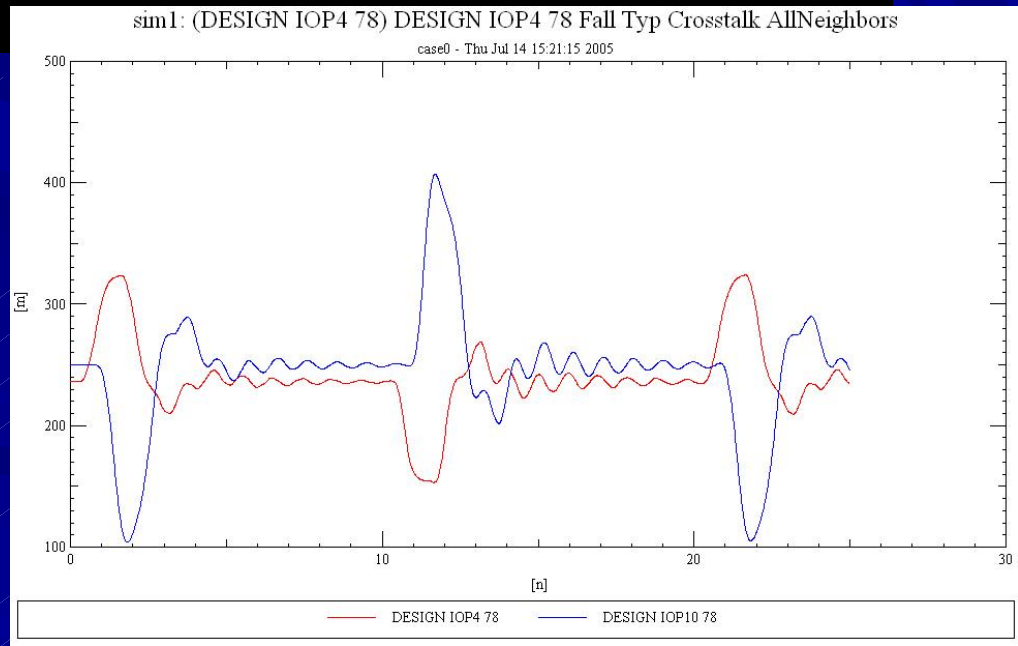


Crosstalk Simulation



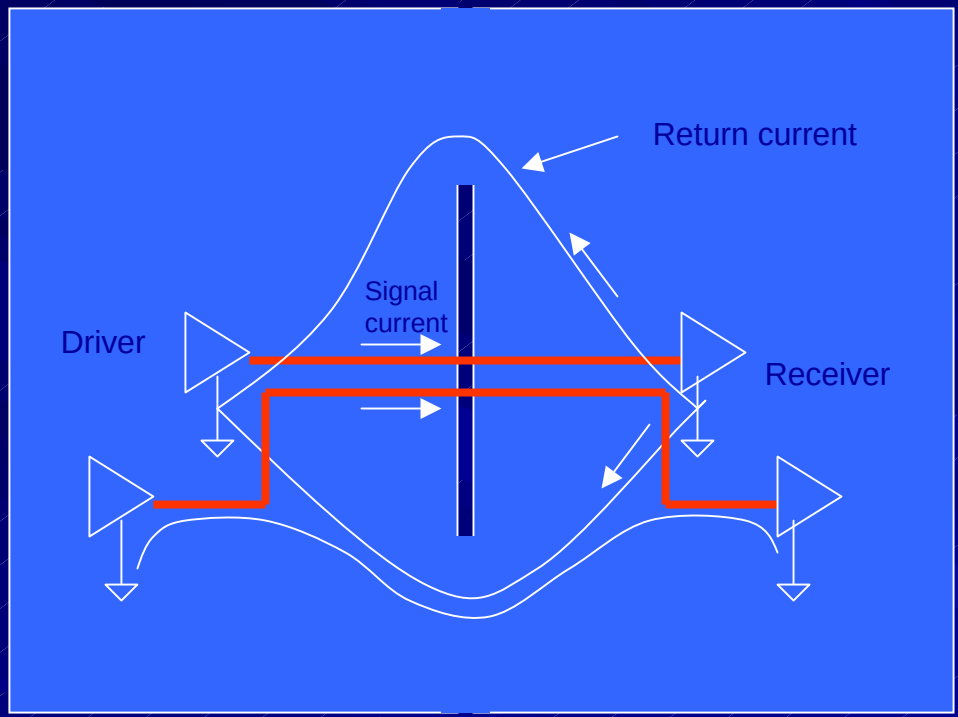
Solution Space Analysis
Trace width and separation

Impacts both SI and EMI



A Gap in the Reference Plane

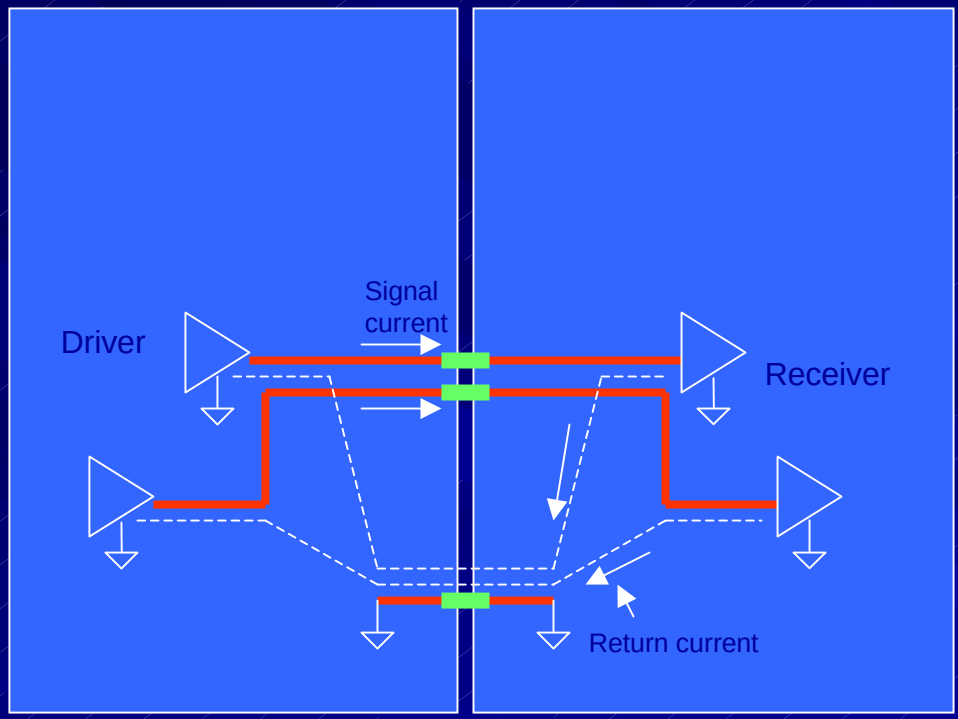
Impacts both SI and EMI



Increased crosstalk due to shared current return path. Overlapping current loops result in mutual inductance causing crosstalk.

Crosstalk in Connectors

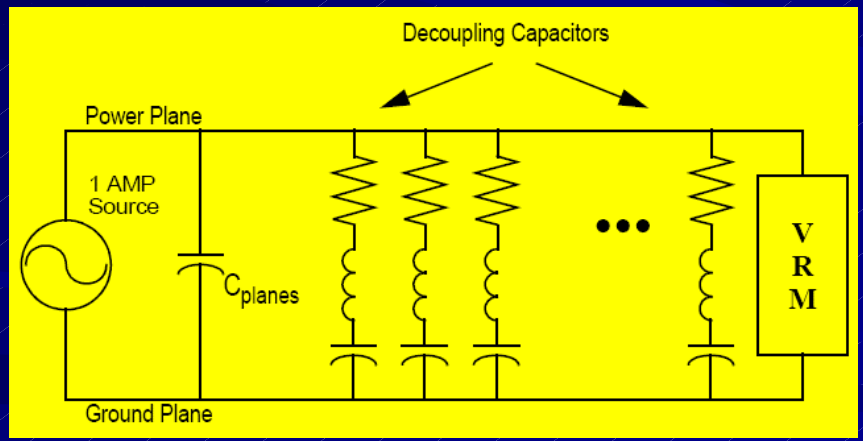
Impacts both SI and EMI

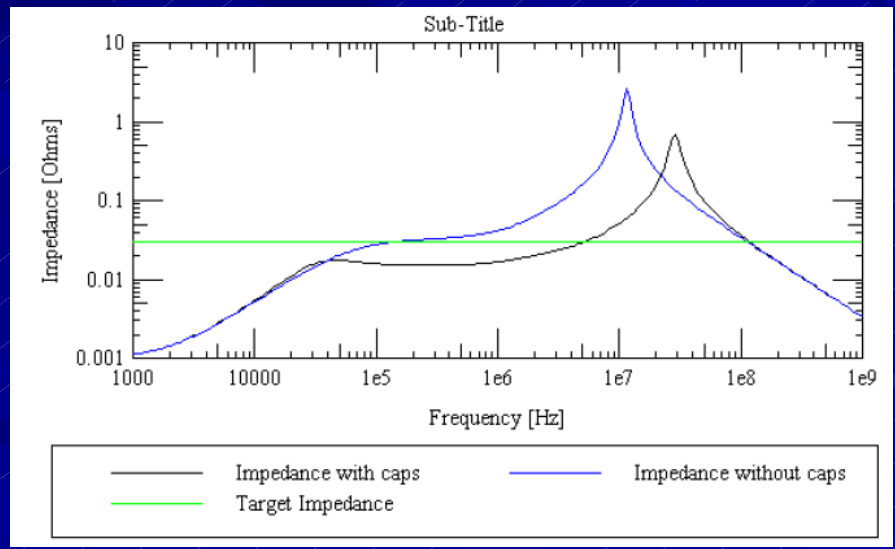


Increased crosstalk due to shared current return path. Overlapping current loops result in mutual inductance causing crosstalk.

Power Integrity Simulation

- Minimize PCB power distribution noise
- Fulfill charge requirements of high-speed devices during switching
- Low target impedance for power/ground over the frequency range of interest

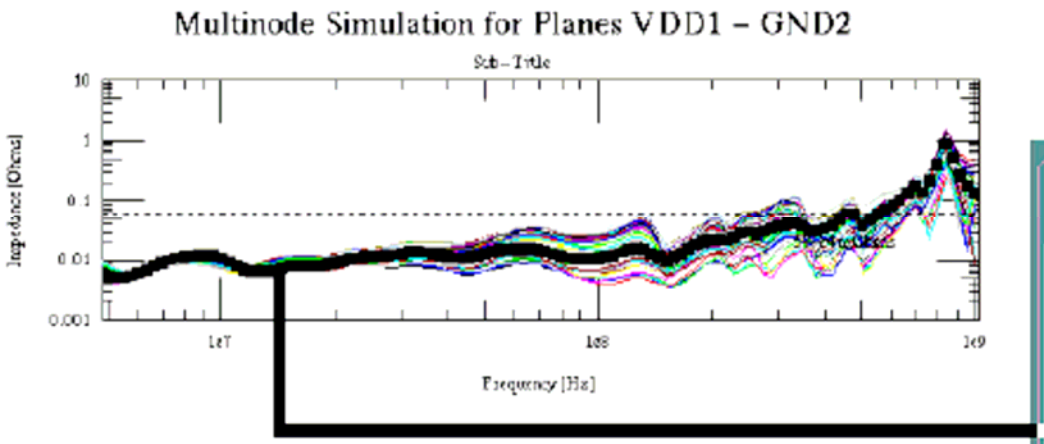


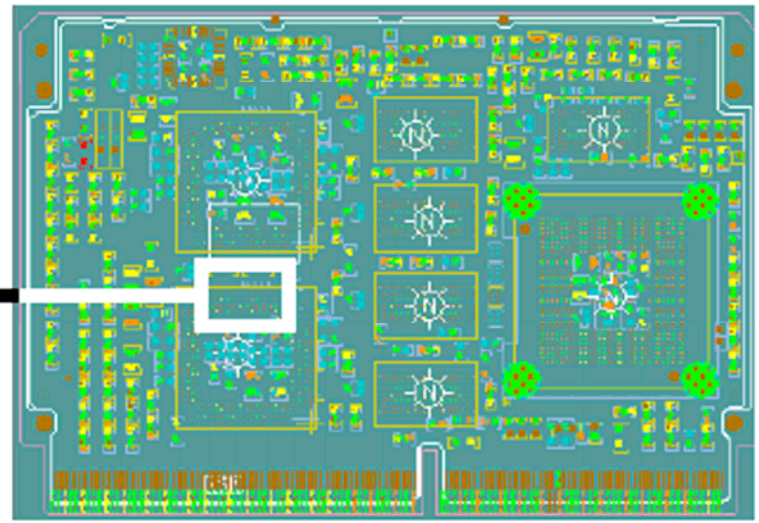


Impacts both SI and EMI

Power Integrity Simulation

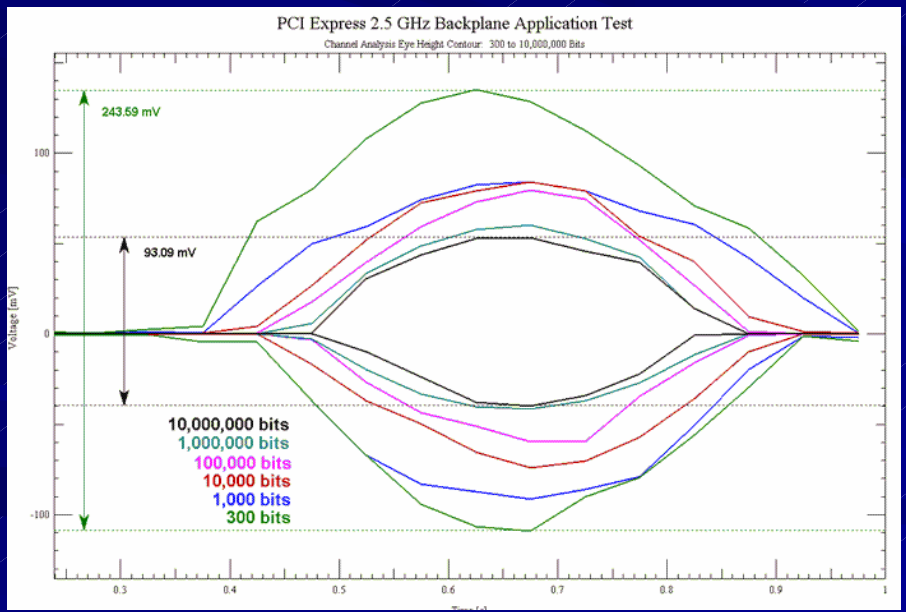
- Selection of bulk and high-frequency decoupling capacitors
- Pre-layout analysis
- PCB resonances and placement of decoupling capacitors
- Post-layout analysis
- Big “V” approach (used in EMI community) vs Capacitor Array approach (more popular in the SI community)

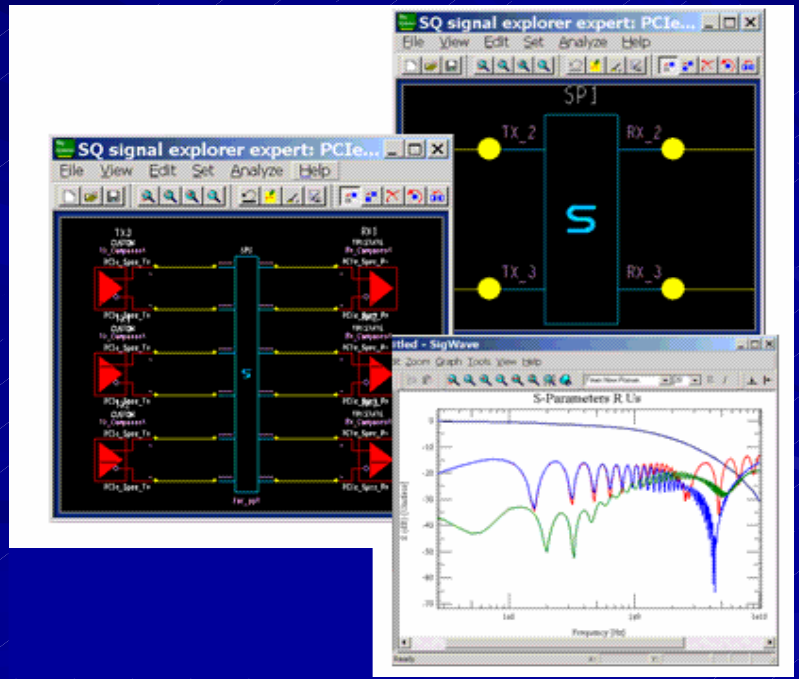




Backplane SI Design

- S-parameter analysis to determine “Insertion Loss” and “Return Loss”
- Skin effect loss, dielectric loss
- Discontinuities like vias, connectors
- Channel Analysis - Tx chip to Rx chip link simulation to verify architecture, determine constraints and optimize design
- Pre- and post-layout simulation
- Backplanes can be characterized up to several GHz

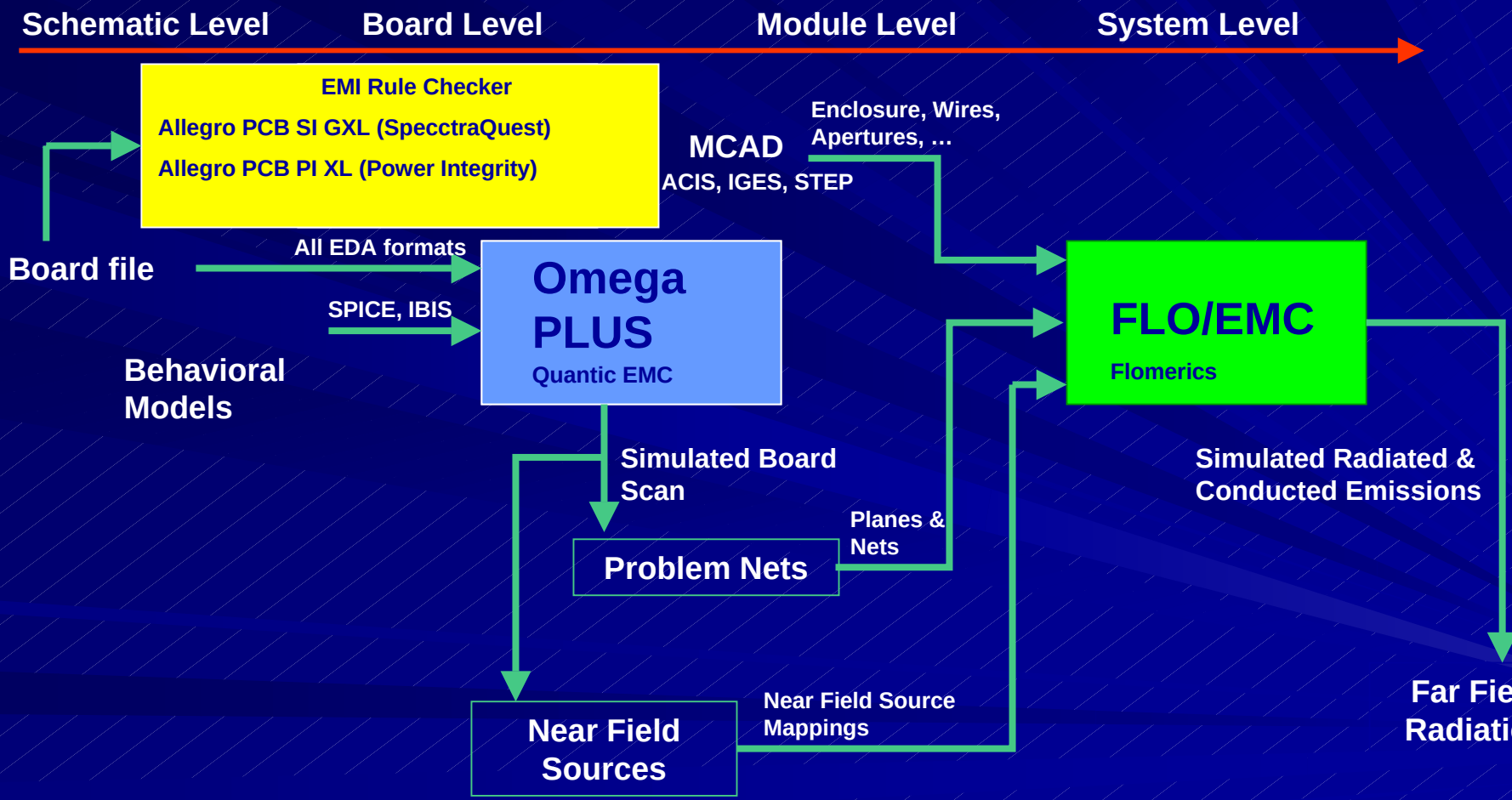




A Typical PCB SI/EMI Design Process

- Schematic and BOM review
- PCB stackup and layer assignment
- Pre-route topology extraction and design
- Solution Space Analysis
  - Statistical design - component, manufacturing and design variances simulated. Design margins applied. Final topology template and design constraints extracted.
- Constraint driven placement
- Constraint driven routing
- Critical net routing review – return current path review
- Post-route analysis and verification
- An EMI rule checker can be used at various review stages

Example of an Integrated EMC/SI Simulation Based Design Process



SI and EMI Measurements

EMI Emissions Measurements

- Are done in frequency domain using an EMI receiver or a spectrum analyzer

SI Measurements

- Mostly done in time domain using:
  Oscilloscope
  TDR (Time Domain Reflectometer)
- Network analyzer is used to measure S-parameters in frequency domain

Summary

- SI is critical to modern day high-speed digital board design
- There are some common design objectives between SI and EMI
- There are some differences between the two areas and, therefore, a good SI design doesn't necessarily mean a good EMI design and a good EMI design can't ensure a good SI design
- EMI design can be improved using simulation techniques used in SI analysis
- The SI and EMI engineers need to work closely in evaluating the possible trade-offs in the design related to EMI/SI.

Some Good SI Books

- “High-speed Digital Design: A Handbook of Black Magic”, by Howard Johnson and Martin Graham.
- “High Speed Signal Propagation: Advanced Black Magic”, by Howard Johnson.
- “High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices” by Stephen Hall, Garrett Hall and James McCall.
- “Signal Integrity – Simplified”, by Eric Bogatin