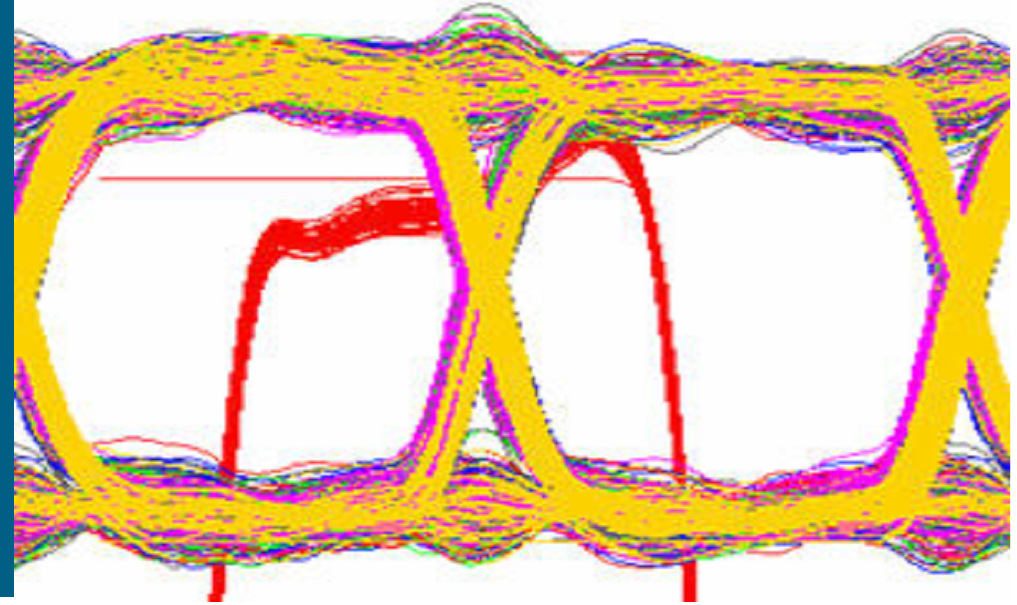




# PCB level SI tools and strategy



**Stephen Scarce**  
**High Speed Design Team Manager**  
**Cisco Systems Inc, RTP NC**

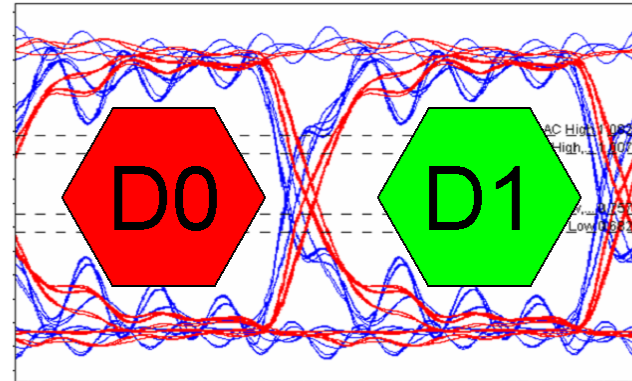
**Q1 FY 2008**

# PCB level SI tools and strategy

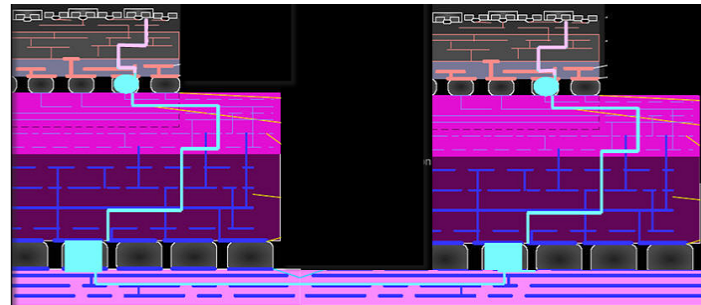
- Definition of HSD
- Static Timing Analysis for DDR
- Pre-route simulations (Scan the design space)
- Routing Rules development for CAD
- Full post route simulations
- Summary

# What Is *High Speed Design*?

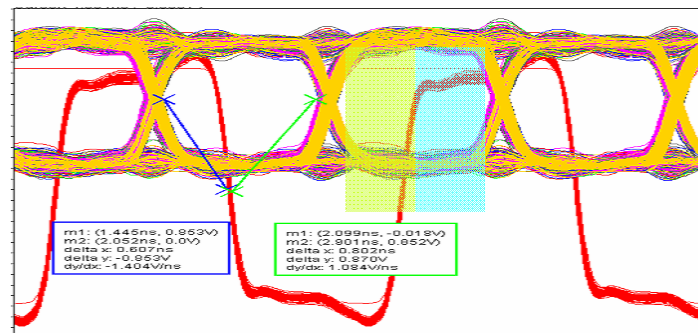
Getting the right data



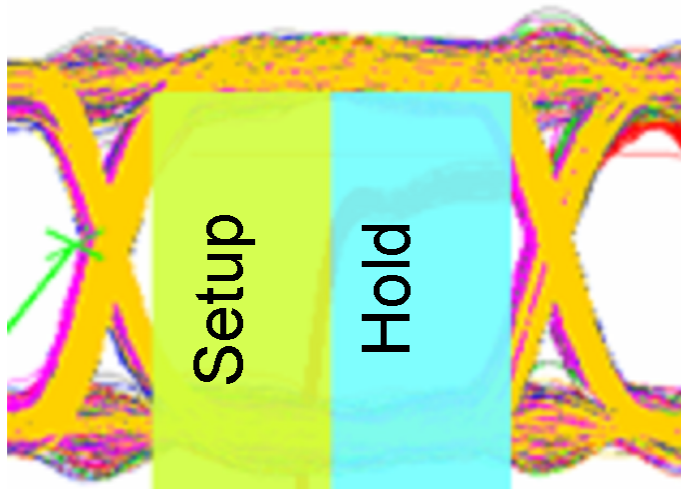
To the right place



At the right time



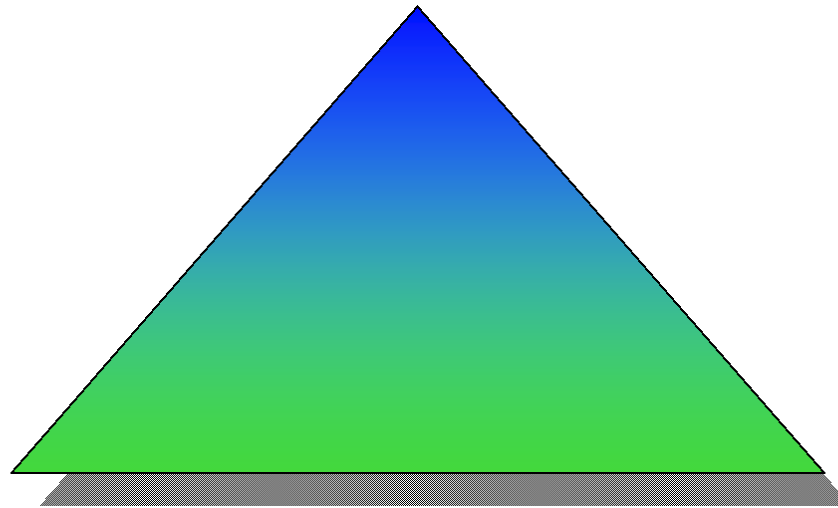
# High Speed Design is the study of analog effects on Timing



- Component timing (process)
- Voltage
- Temperature
- Package & PCB routing lengths
- PCB manufacturing variations ( $Z_0$ , loss)
- Reflection/Overshoot
- ISI
- SSN/SSO
- Crosstalk...

# High Speed Design

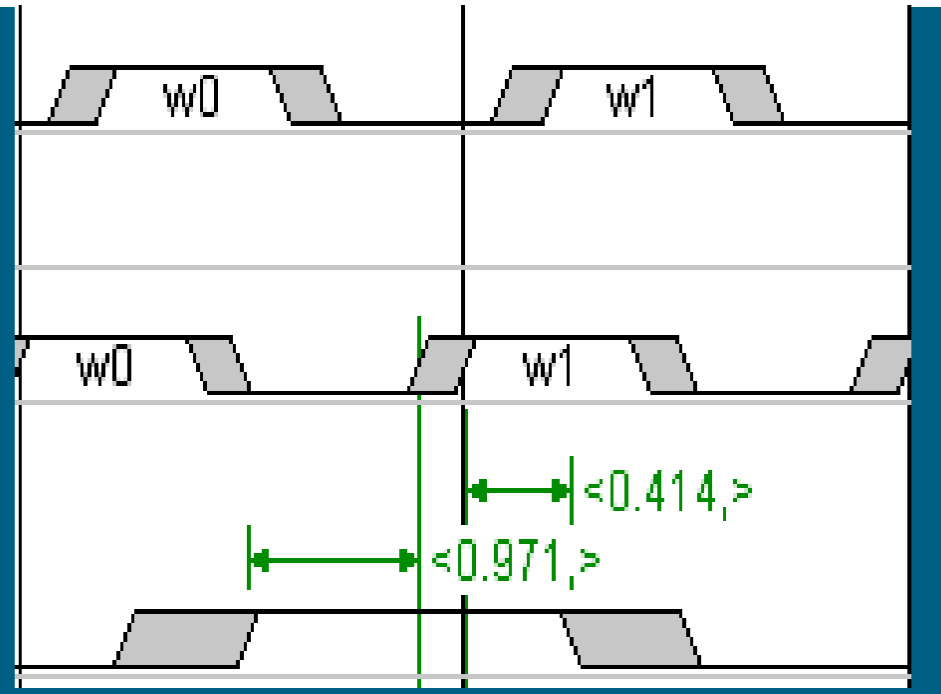
## Constraint-Driven Design



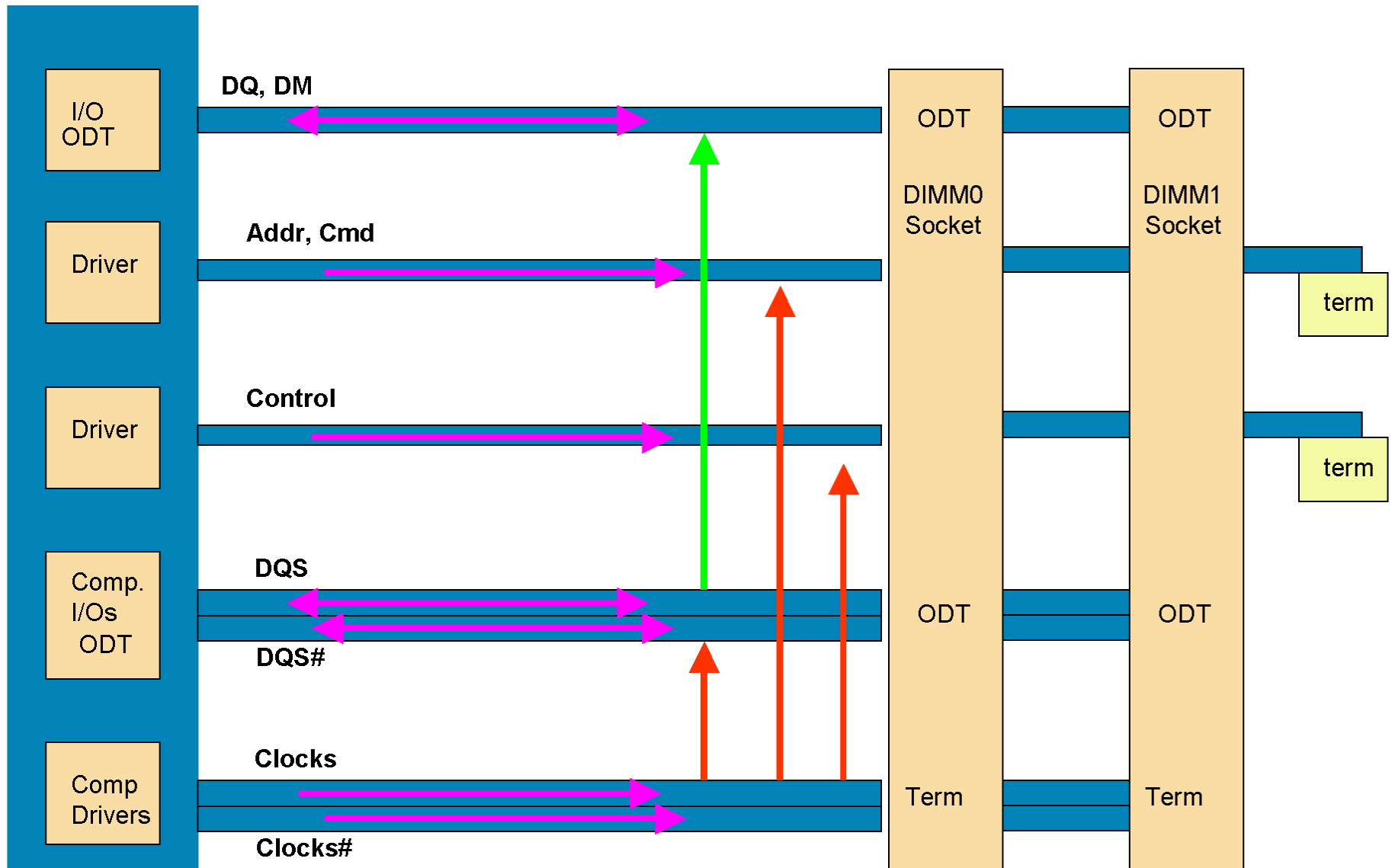
Static Timing Analysis

Signal & Power  
Integrity Analysis

# Static Timing Analysis



# Timing Budget for DDR2

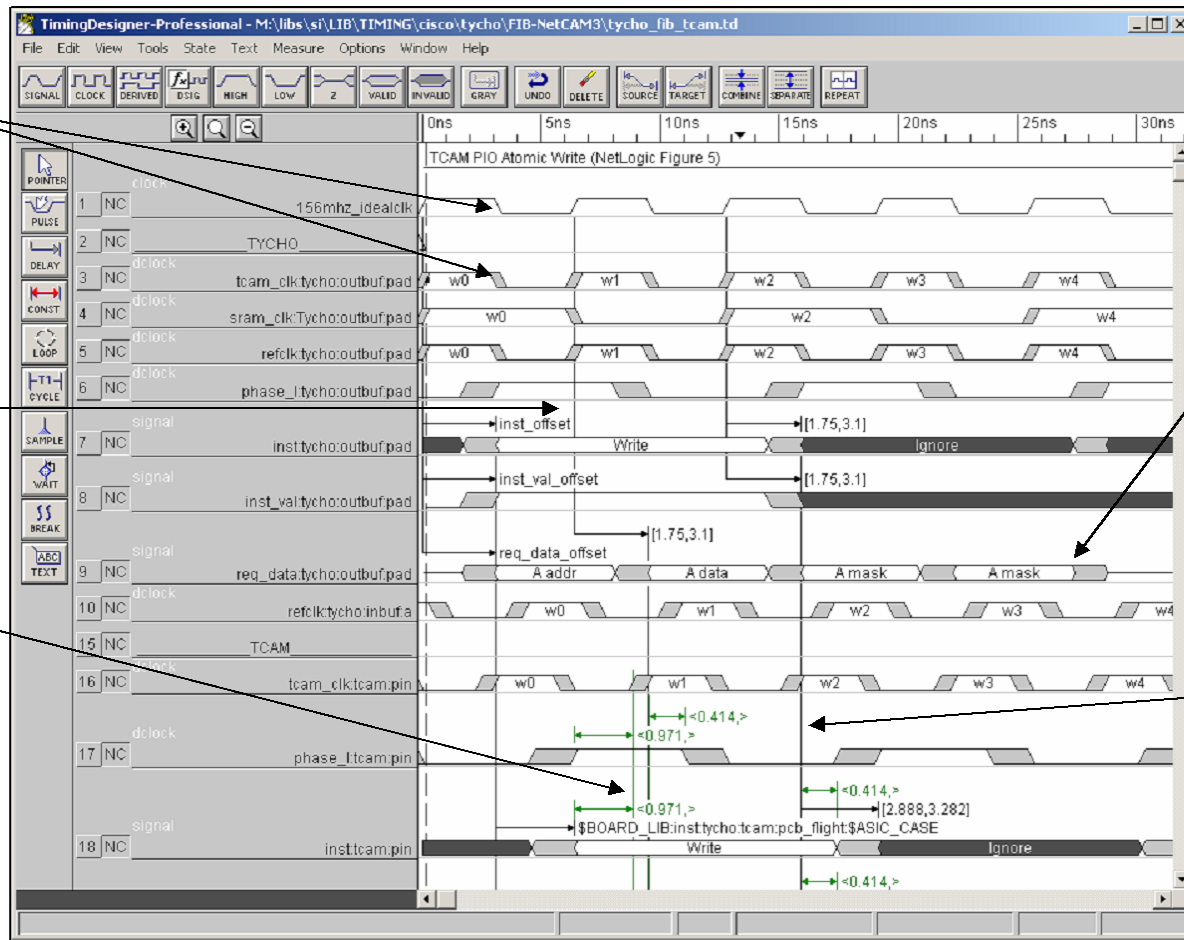


# Develop a Static Timing Model

Clocks and characteristics

Output timing

Input requirements



Bus protocol

Connectivity & delays



# STA for DDR2 is based on vendors datasheet (which are JESD79-2C based)



256Mb: x4, x8, x16 DDR2 SDRAM  
AC Operating Specifications

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 4 of 6)

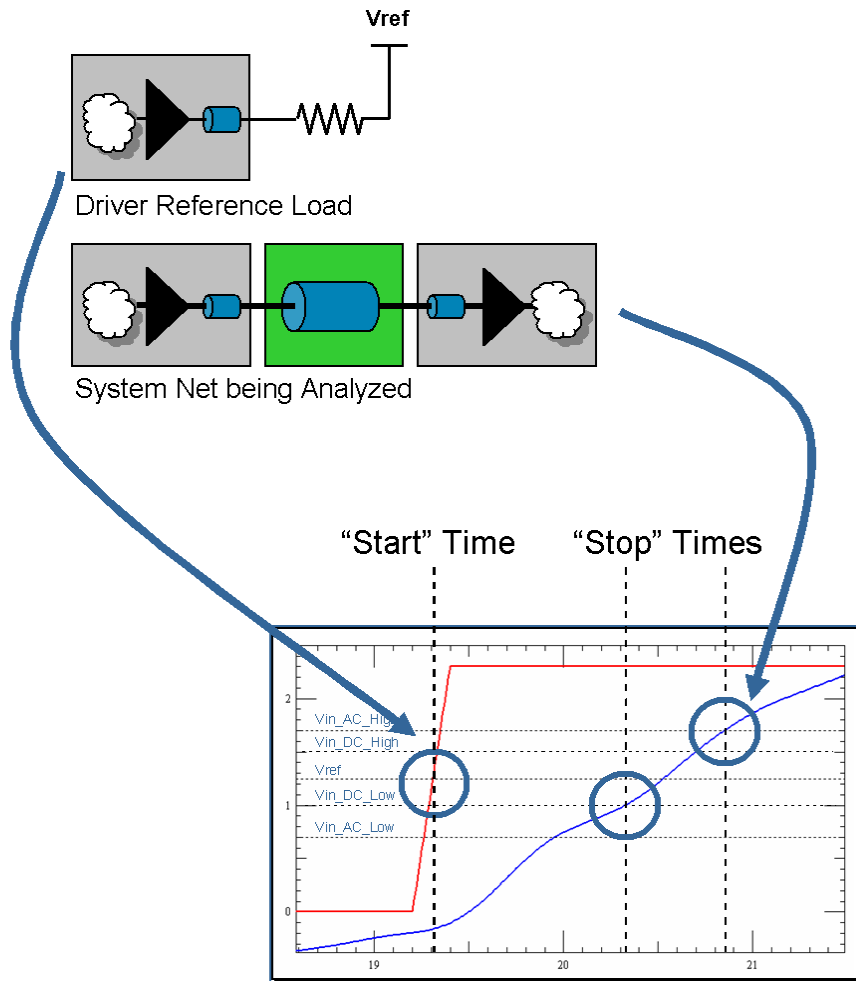
Notes: 1-5; notes appear on page 125; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC Characteristics		-3E		-3		-37E		-5E		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Address and control input pulse width for each input	$t_{IPW}$	0.6		0.6		0.6		0.6		$t_{CK}$	37
Address and control input setup time	$t_{IS_a}$	400		400		500		600		ps	6, 19
Address and control input hold time	$t_{IH_a}$	400		400		500		600		ps	6, 19
Address and control input setup time	$t_{IS_b}$	200		200		250		350		ps	6, 19
Address and control input hold time	$t_{IH_b}$	275		275		375		475		ps	6, 19

# DDR2 Timing

- Data Sheet Timing is with respect to a specific load
  - Reference: 25 ohms to  $V_{DDQ}/2$
  - Timing measured to  $V_{ref}$
- Device timing is measured with respect to thresholds
  - Dependant on operating frequency
  - IO type used (DM\_INPUT\_533/DQFULL\_533, INPUT\_533(ADDR))
  - Specific edge (Rising, Falling)
  - Slew rates of the signals

# Data Sheet Timing and Interconnect Delays



- Interconnect delays from simulations have *start* and *stop* times

*Start* times are based on output timing specs

Reference loads and voltage levels

IBIS  $V_{ref}$ ,  $C_{ref}$ ,  $R_{ref}$ ,  $V_{meas}$

*Stop* times are based on input (setup/hold) timing specs

Measured at defined voltage levels and slew rates

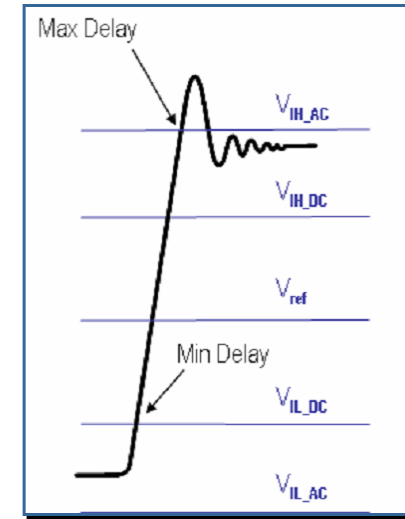


# Device timing (DQ Signals)

Note: Guard bands not shown

## Quality

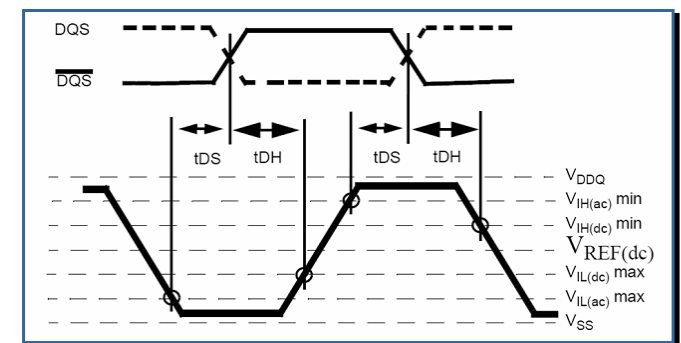
- A rising edge must:
  - Start below  $V_{IL\_DC}$
  - Switch through  $V_{IH\_AC}$
  - Settle above  $V_{IH\_DC}$



SI View

## Timing

- **MIN** delay measured at first crossing of  $V_{IL\_DC}$ 
  - Used to compute hold margin
  - JESD79-2C, page 96, note 21
- **MAX** delay measured at first crossing of  $V_{IH\_AC}$ 
  - Used to compute setup margin
  - JESD79-2C, page 96, note 20



Timing Spec View

# Timing files to implement STA

# 667 DDR2 parts running at 667 DDR2

ADDCMD\_SETUP = 0.200

ADDCMD\_HOLD = 0.275

CTRL\_SETUP = 0.200

CTRL\_HOLD = 0.275

DQ\_SETUP = 0.100

DQ\_HOLD = 0.175

tQHS\_SKEW\_MAX = 0.340

tDQSQ\_SKEW\_MAX = 0.240

#DQ Write timing

SETHLD DQ \*TO R DQS DQ\_SETUP

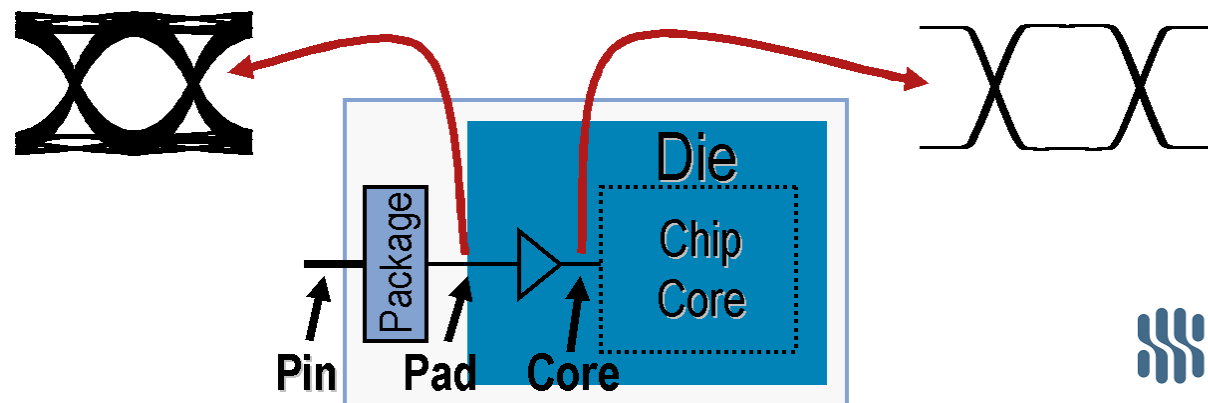
DQ\_HOLD

SETHLD DQ \*TO F DQS DQ\_SETUP

DQ\_HOLD

# DDR2 Slew Rate Derating

- Baseline setup/hold requirements are based on specific voltage and slew rate conditions
- System slew rates rarely conform to measurement conditions  
Loading can vary widely within the same system
- DDR2 slew-rate derating defines adjustments to setup/hold specs based on actual slew rates of input signals



# SiSoft's Slew Rate Methodology

- Device setup/hold times based on nominal (base) values
- Derating tables converted into independent derating values for DQ and DQS nets
- Derating info included in simulation models – measurements & adjustments are automated

DQ Vref->AC Slew Rate |SiSoft\_Derate\_Max

DQ DC->Vref Slew Rate -|SiSoft\_Derate\_Min

**Table 29: DDR2-667 <sup>t</sup>DS, <sup>t</sup>DH Derating Values with Differential Strobe**  
Notes: 1-7; all units in ps

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																		
	2.8 V/ns		2.4 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		
	$\Delta^t$ DS	$\Delta^t$ DH	$\Delta^t$ DS	$\Delta^t$ DH	$\Delta^t$ DS	$\Delta^t$ DH	$\Delta^t$ DS	$\Delta^t$ DH	$\Delta^t$ DS	$\Delta^t$ DH	$\Delta^t$ DS	$\Delta^t$ DH	$\Delta^t$ DS	$\Delta^t$ DH	$\Delta^t$ DS	$\Delta^t$ DH	$\Delta^t$ DS	$\Delta^t$ DH	
2.0	100	63	100	63	100	63	112	75	124	87	136	99	148	111	160	123	172	135	
1.5	67	42	67	42	67	42	79	54	91	66	103	78	115	90	127	102	139	114	
1.0	0	0	0	0	0	0	12	12	24	24	36	36	48	48	60	60	72	72	
0.9	-5	-14	-5	-14	-5	-14	7	-2	19	10	31	22	43	34	55	46	67	58	
0.8	-13	-31	-13	-31	-13	-31	-1	-19	11	-7	23	5	35	17	47	29	59	41	
0.7	-22	-54	-22	-54	-22	-54	-10	-42	2	-30	14	-18	26	-6	38	6	50	18	
0.6	-34	-83	-34	-83	-34	-83	-22	-71	-10	-59	2	-47	14	-35	26	-23	38	-11	
0.5	-60	-125	-60	-125	-60	-125	-48	-113	-36	-101	-24	-89	-12	-77	0	-65	12	-53	
0.4	-100	-188	-100	-188	-100	-188	-88	-176	-76	-164	-64	-152	-52	-140	-40	-128	-28	-116	

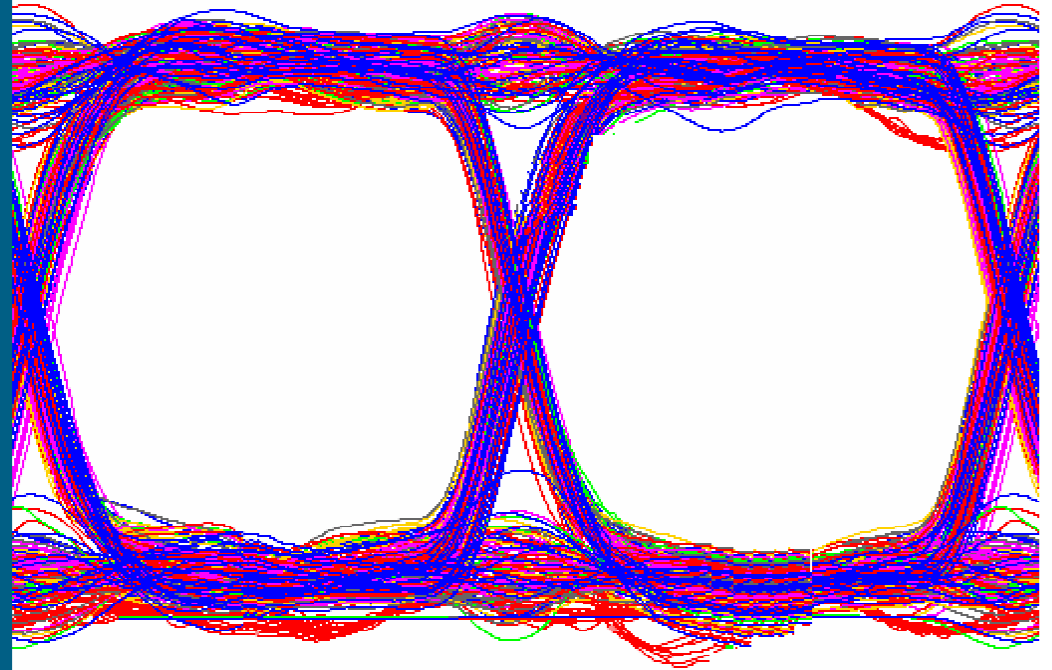
DQS DC->AC Slew Rate |SiSoft\_Derate\_Max

DQS DC->AC Slew Rate -|SiSoft\_Derate\_Min

Nominal slew rate row and column

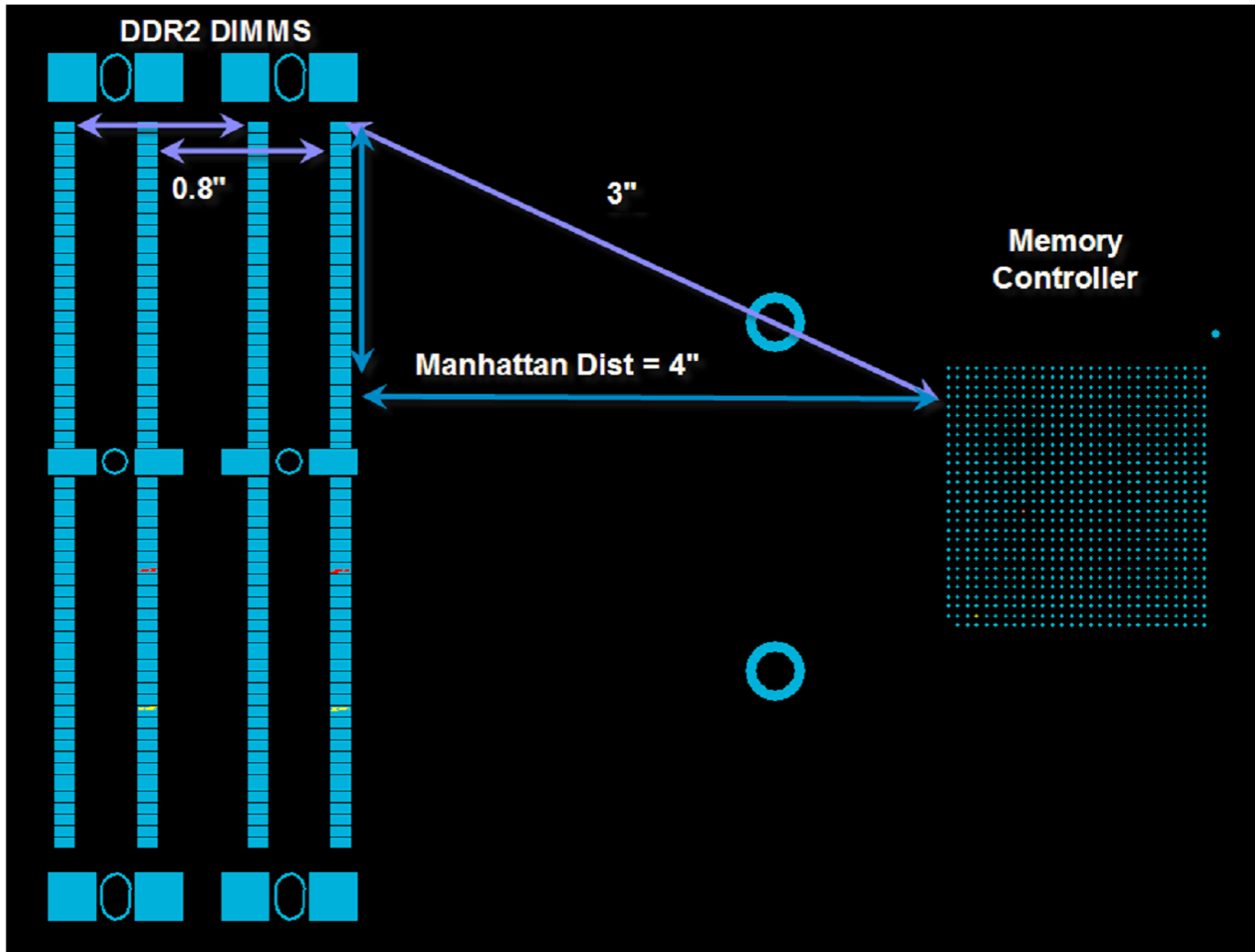


# Pre-route simulations

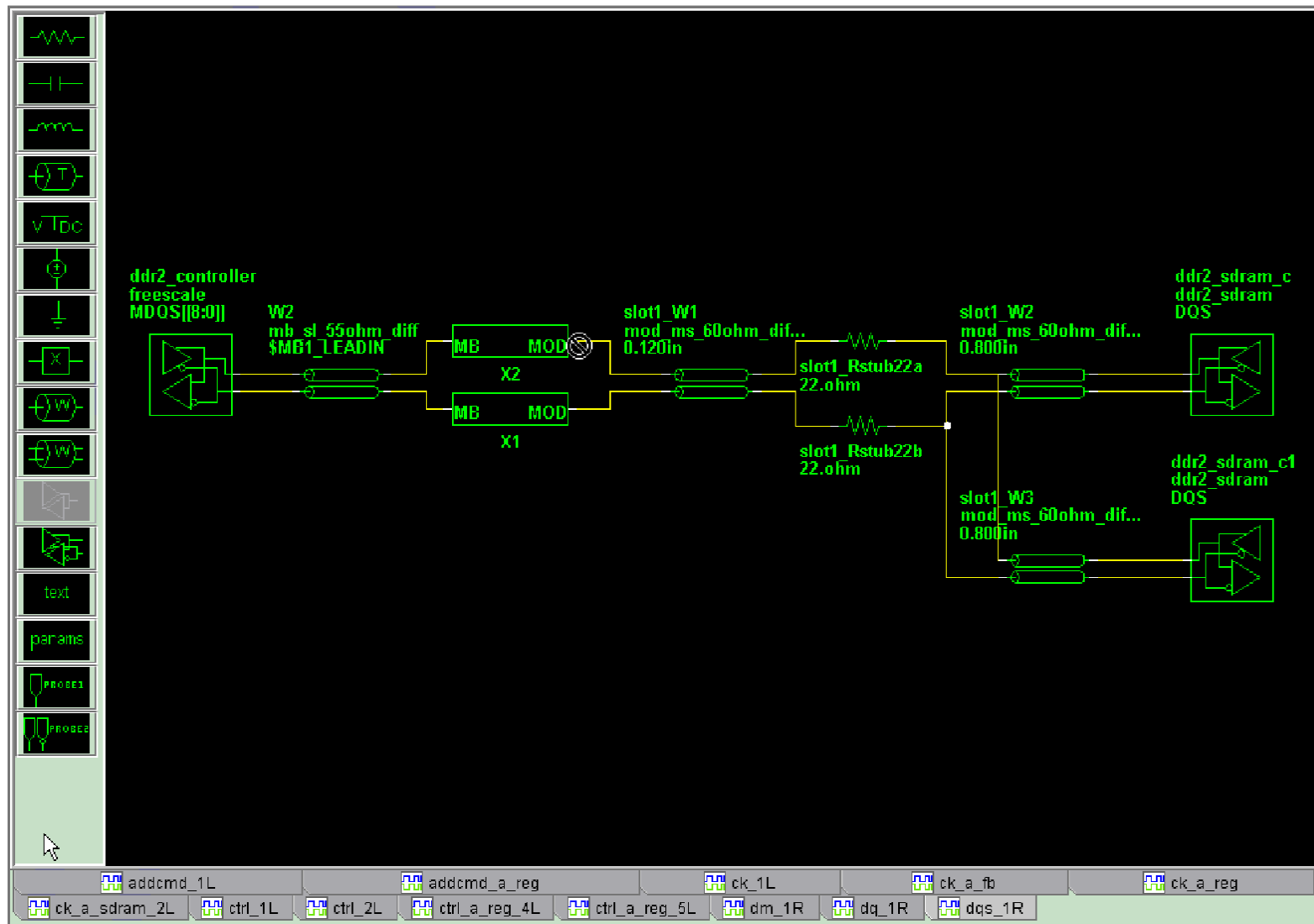




# PCB component placement



# Topologies for current placement



# Extracted Topologies add sweep variables for Cad constraints, and select ODT settings

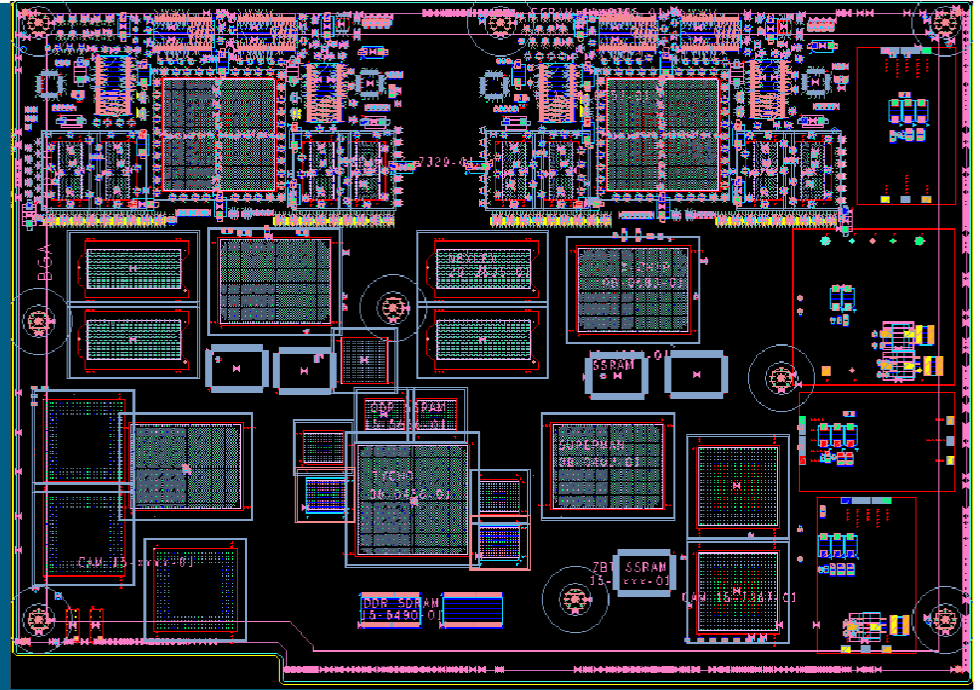
The screenshot displays a circuit simulation environment. On the left is a toolbar with various components like resistors, capacitors, and transmission lines. The main workspace shows a circuit diagram with a PLL (ddr2\_pll) connected to several transmission lines (WTL0, WTL1, WTL2, WTL3a, WTL3b, WTL3b1, WTL3b2) which are connected to four DDR2 SDRAM components (ddr2\_sdram\_1 to ddr2\_sdram\_4). A resistor (R1) is also present. The bottom panel shows a 'Solution Space' table with columns for Transfer Net, Variable, Type, Variation Group, Value 1, and Value 2.

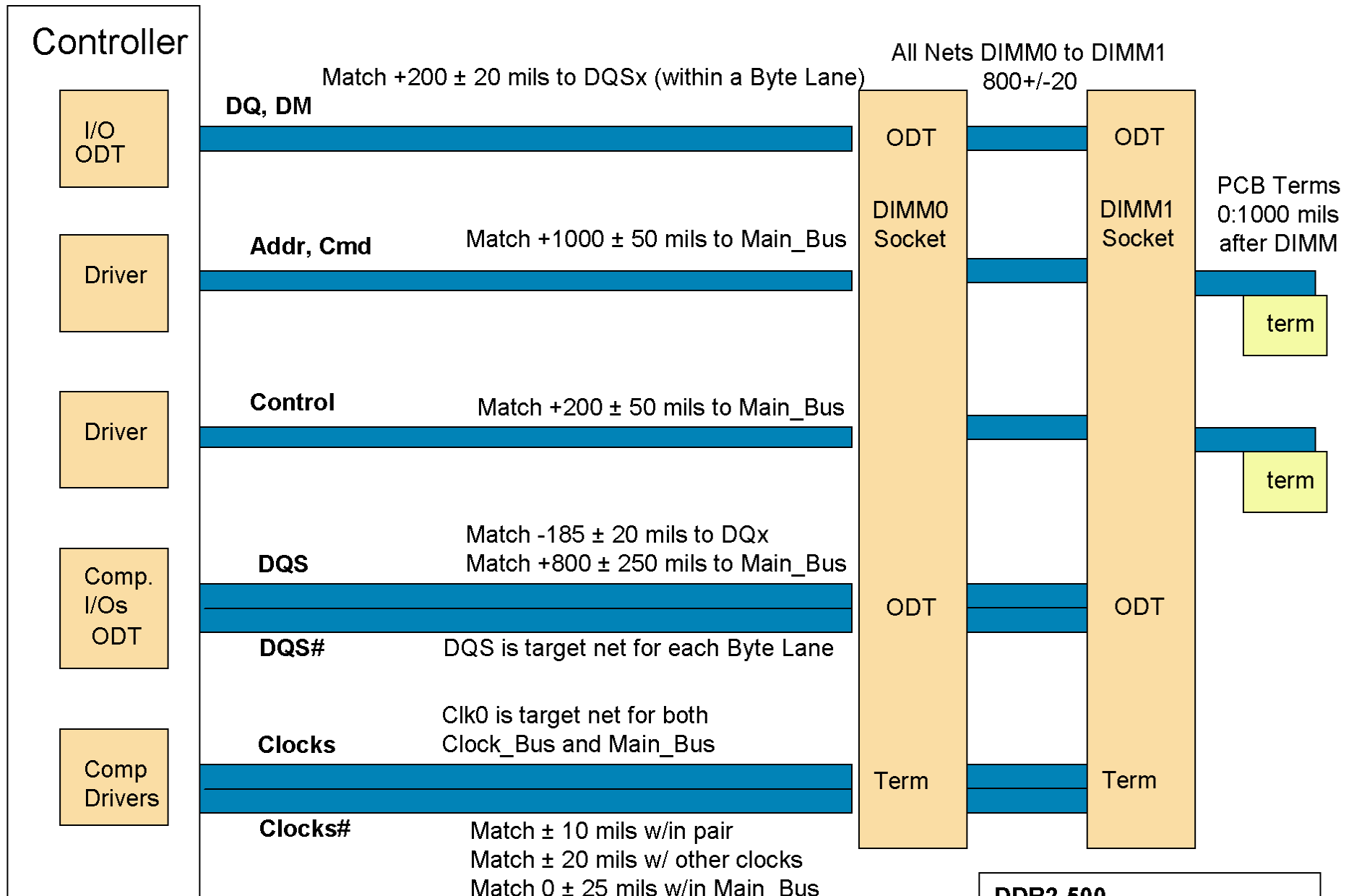
Transfer Net	Variable:	Type:	Variation Group:	Value 1:	Value 2:
ck_a_reg	\$TL0	W Length	length	\$G_A_CK_REG_TL0	\$G_A_CK_REG_TL0
ck_a_reg	\$TL1	W Length	length	\$G_A_CK_REG_TL1	\$G_A_CK_REG_TL1
ck_a_reg	\$TL2	W Length	length	\$G_A_CK_REG_TL2	\$G_A_CK_REG_TL2
ck_a_sdram_2L	\$R1	Resistance	term r	\$G_A_CK_SDRAM_R1	\$G_A_CK_SDRAM_R1
ck_a_sdram_2L	\$TL0	W Length	length	\$G_A_CK_SDRAM_TL0	\$G_A_CK_SDRAM_TL0
ck_a_sdram_2L	\$TL1	W Length	length	\$G_A_CK_SDRAM_TL1	\$G_A_CK_SDRAM_TL1
ck_a_sdram_2L	\$TL2	W Length	length	\$G_A_CK_SDRAM_TL2	\$G_A_CK_SDRAM_TL2
ck_a_sdram_2L	\$TL3	W Length	length	\$G_A_CK_SDRAM_TL3	\$G_A_CK_SDRAM_TL3

# Verify the pre-route timing across case

Setup Margin (ns)	Hold Margin (ns)	Rmin Etch Delay (ns)	Rmax Etch Delay (ns)	Fmin Etch Delay (ns)	Fmax Etch Delay (ns)	Transfer Net
0.037	0.784	1.331	1.71	1.331	1.71	DQS_ECC_2R_2Slot
0.153	0.585	1.206	1.616	1.205	1.614	DQS_2R_2Slot
0.828	1.01	1.037	1.511	1.072	1.412	Pre_reg_cmd_slot1
0.807	1.03	1.153	1.675	1.189	1.575	Pre_reg_cmd_slot2
0.375	1.127	1.154	1.907	1.195	1.748	Pre_reg_CS
0.617	1.006	1.033	1.865	1.067	1.744	Pre_reg_addcmd
0.344	0.232	1.132	1.795	1.143	1.741	DQ_2R_2Slot
0.395	0.305	1.293	1.662	1.294	1.603	DM_2R_2Slot
1.223	1.411	0.827	1.244	0.771	1.312	Post_reg_addcmd_LB
1.169	1.255	0.756	1.34	0.623	1.376	Post_reg_addcmd_RB
1.442	1.228	0.701	1.091	0.615	1.08	Post_Reg_CTRL_4L
0.875	1.356	0.819	1.592	0.733	1.656	Post_Reg_CTRL_5L

# Routing Rules development for CAD

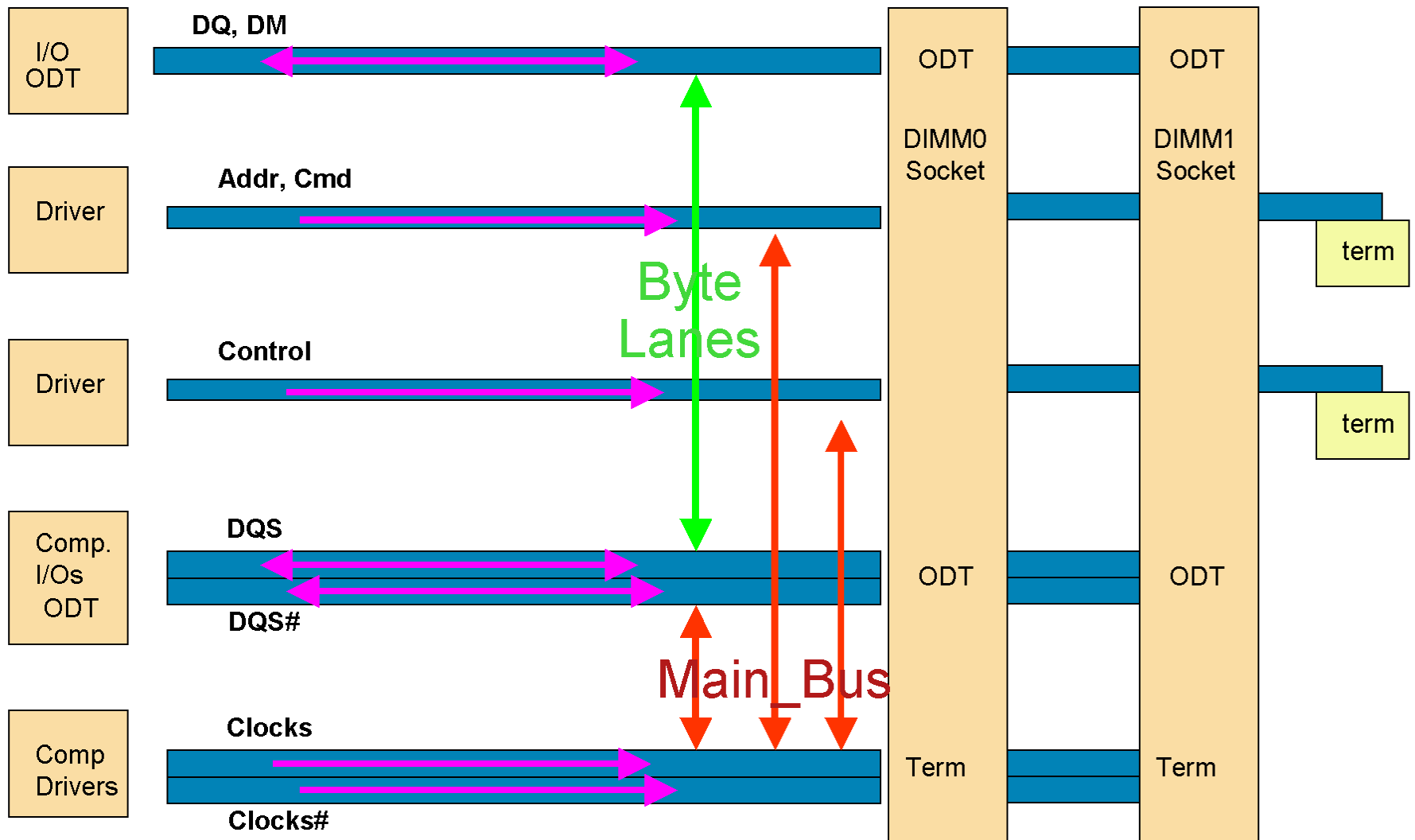




**DDR2-500  
 JEDEC Standard "A" & "B"**

DDR2 "Main\_Bus" Length  
 is approx. 4000 mils nominal

# Define rule sets to meet Timing



# Rules in Allegro CMS

Allegro Constraint Manager (connected to Allegro PCB Design 610 15.51) - [Nets: Routing]

File Edit Objects Column View Analyze Audit Tools Window Help

Electrical Constraint Set

- Signal Integrity
- Timing
- Routing
- All Constraints

Net

- Signal Integrity
- Timing
- Routing
  - Wiring
  - Impedance
  - Min/Max Propagation Delays
  - Total Etch Length
  - Differential Pair
  - Relative Propagation Delay
- Custom Measurement
- General Properties

DRC

- Electrical
- Spacing
- Physical
- Design

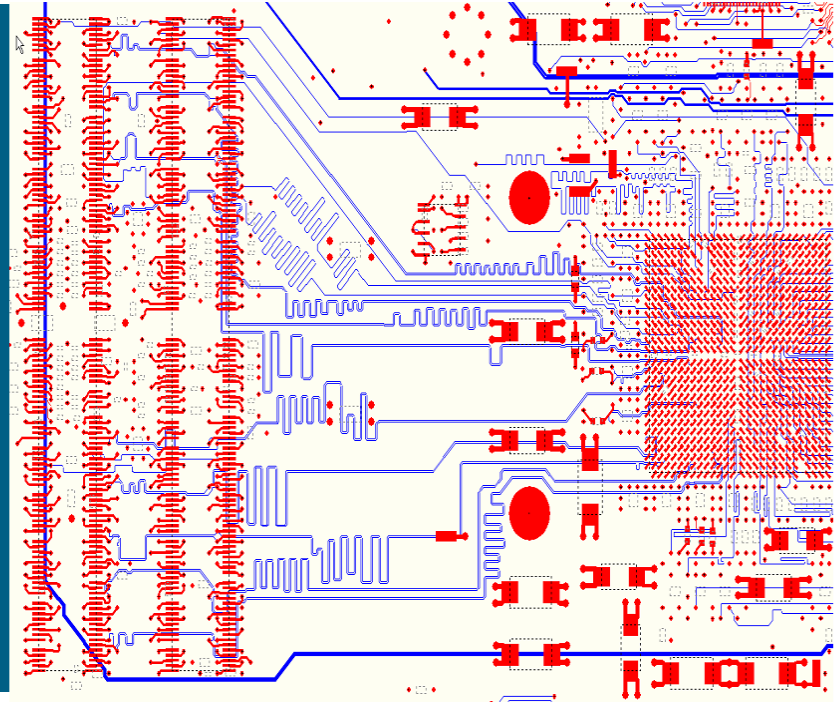
Objects	Reference	Pin Pair	Pin Delay		Scope	Relative Delay		
			Pin 1 mil	Pin 2 mil		Delta:Tolerance ns	Actual	Margin
RP_DATA_BUS								0.23 MIL
RP_DATA_LANE_0								9.93 MIL
RP_DATA_LANE_1								1.65 MIL
U1U.F3:J3D.143 [MEM_D15]					Global	185 MIL:10 MIL		0.07 MIL 9.93 MIL
U1U.F6:J3D.22 [MEM_D11]					Global	185 MIL:10 MIL		3.02 MIL 6.98 MIL
U1U.G4:J3D.142 [MEM_D14]					Global	185 MIL:10 MIL		6.27 MIL 3.73 MIL
U1U.G5:J3D.21 [MEM_D10]					Global	185 MIL:10 MIL		0.53 MIL 9.47 MIL
U1U.H1:J3D.16 [MEM_DQS]					Global	:0 MIL		TARGET
U1U.H3:J3D.15 [MEM_DQS]					Global	0 MIL:10 MIL		0.41 MIL 9.59 MIL
U1U.H4:J3D.136 [MEM_DM]					Global	185 MIL:10 MIL		5.12 MIL 4.88 MIL
U1U.J5:J3D.134 [MEM_D13]					Global	185 MIL:10 MIL		0.79 MIL 9.21 MIL
U1U.J6:J3D.13 [MEM_D9]					Global	185 MIL:10 MIL		8.35 MIL 1.65 MIL
U1U.K4:J3D.12 [MEM_D8]					Global	185 MIL:10 MIL		1.53 MIL 8.47 MIL
U1U.K5:J3D.133 [MEM_D12]					Global	185 MIL:10 MIL		0.3 MIL 9.7 MIL
RP_DATA_LANE_2								0.09 MIL
RP_DATA_LANE_3								3.51 MIL
RP_DATA_LANE_4								1.83 MIL
RP_DATA_LANE_5								2.41 MIL
RP_DATA_LANE_6								3.22 MIL
RP_DATA_LANE_7								0.14 MIL
RP_DATA_LANE_8								0.19 MIL
RP_DDR2_CLOCKS_FAR								2.49 MIL

Click and drag to change column size

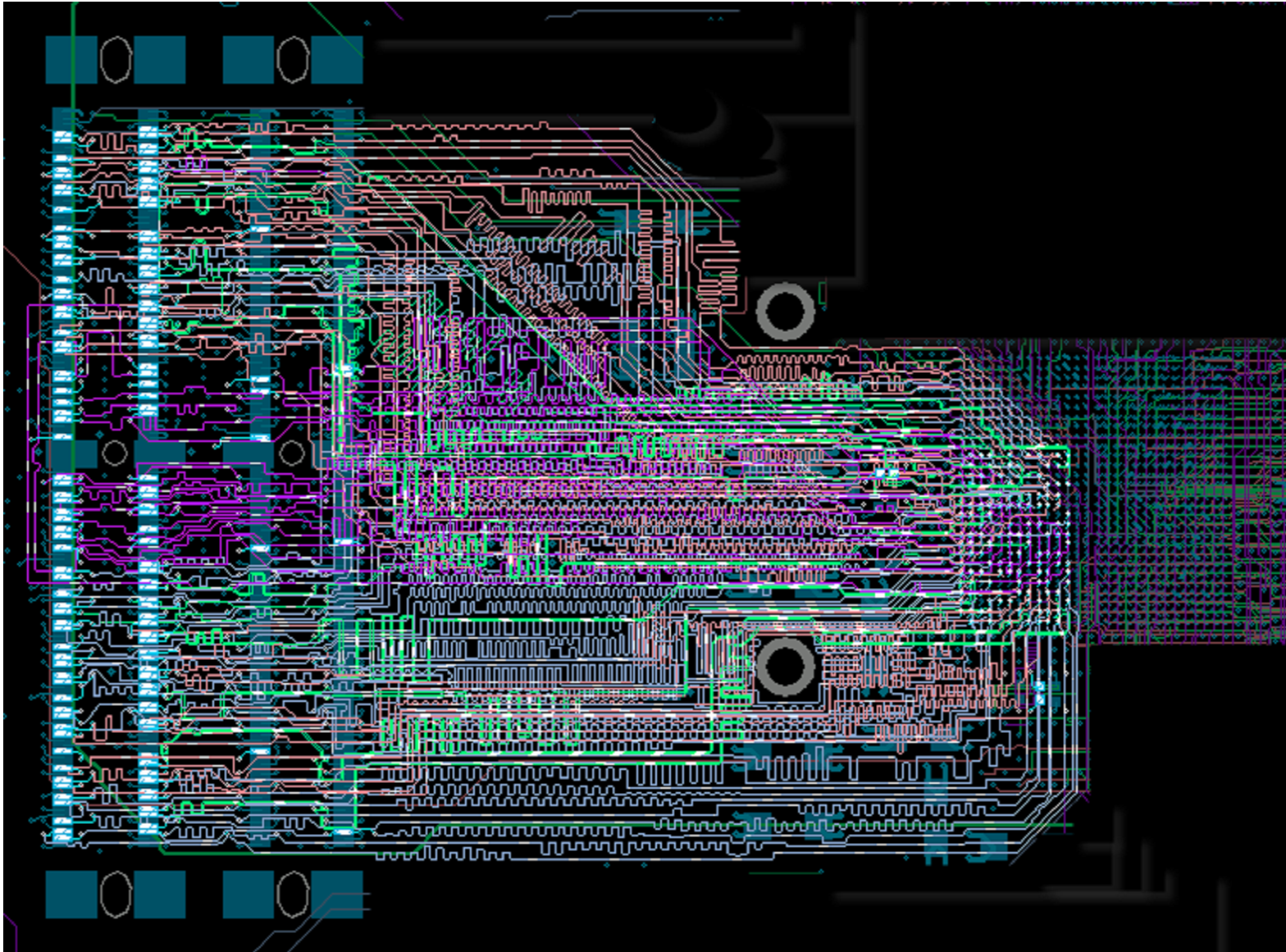
SYNC XNET



# Post Route Simulations



# Fully routed Allegro design



# QSI for Post Route Simulations

**Extended Net Simulation**

Available: 3751

Included: 175

Xtalk Scan Violations Only

**Simulation Mode**

SIVTiming

Crosstalk

Incremental

**Post-Layout Operations**

Transfer Net	Pin Equivalent Net	Extended Net	Simulate	Simulation Status	Simulate Incrementally	Data Rate	Type	Mode	Coupling Type	Crosstalk Group
addcmd_1L	2p_1o_1i_A_1u	rp_base%DDR_CAS_L	Yes	Unsimulated	No	5.0ns	Data	Single Ended	Sync	addcmd_1L
addcmd_1L	2p_1o_1i_A_1u	rp_base%DDR_MA[13:0]	Yes	Unsimulated	No	5.0ns	Data	Single Ended	Sync	addcmd_1L
addcmd_1L	2p_1o_1i_A_1u	rp_base%DDR_MBA[2:0]	Yes	Unsimulated	No	5.0ns	Data	Single Ended	Sync	addcmd_1L
addcmd_1L	2p_1								Sync	addcmd_1L
addcmd_1L	2p_1								Sync	addcmd_1L

**Post-Layout Simulation Control**

**Corners:**

Etch

SE TE FE

SS

IC TT

FF

State:

Drivers:

Receivers:

AC Noise:

**Reference Schematic Overrides:**

Use for Drivers & Receivers

Use for Corners

**Simulation Control**

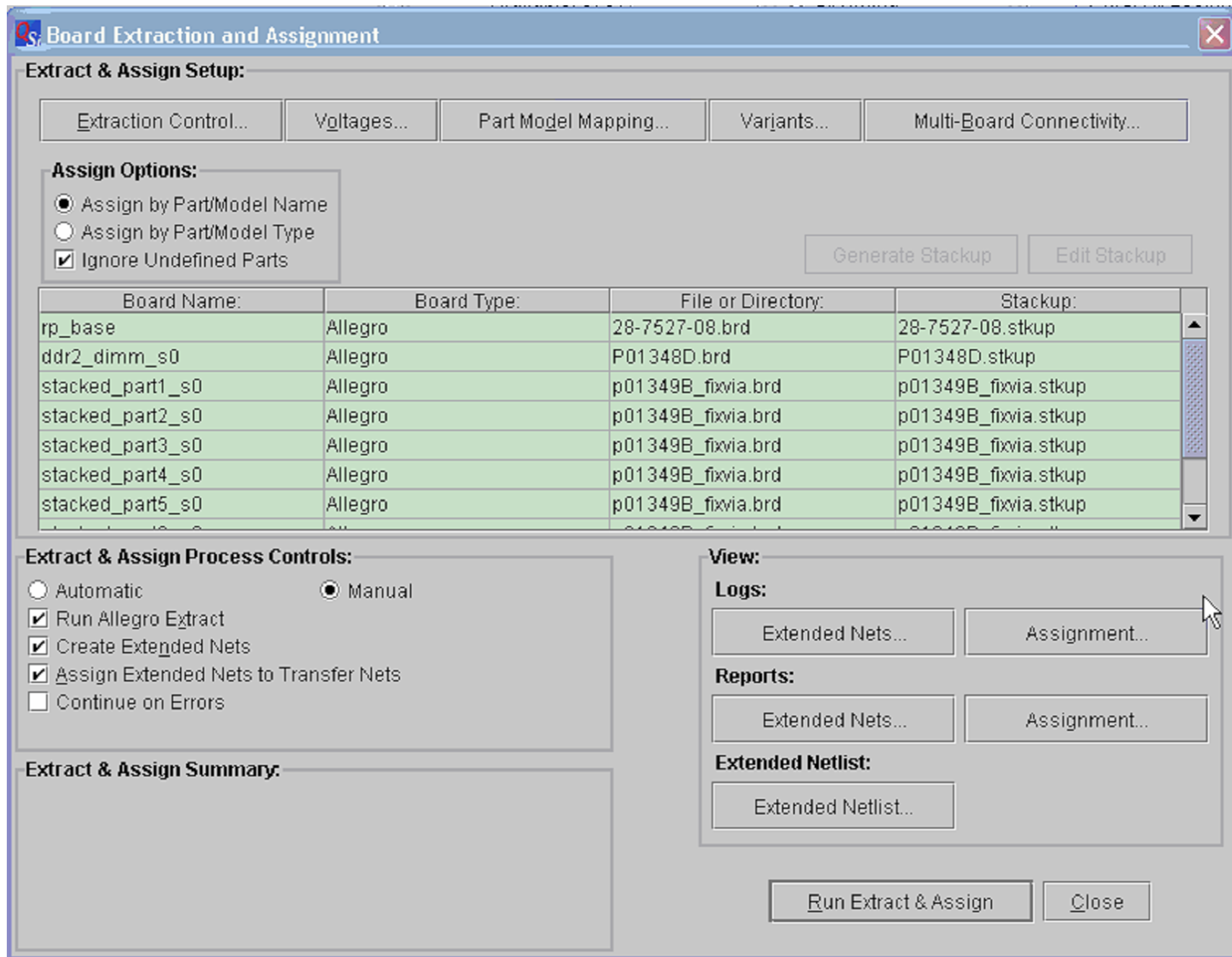
Default AC Noise: +/-0.00V

Transfer Net	State	AC Noise Source	AC Noise
addcmd_1L	A	Transfer Net	+/-0.0V
addcmd_a_reg	default	Transfer Net	+/-0.00V
ck_1L	A	Transfer Net	+/-0.0V
ck_a_fb	default	Transfer Net	+/-0.00V
ck_a_reg	default	Transfer Net	+/-0.00V
ck_a_sdrum_2L	default	Transfer Net	+/-0.00V
ctrl_1L	A	Transfer Net	+/-0.0V
ctrl_2L	default	Transfer Net	+/-0.00V
ctrl_a_reg_4L	default	Transfer Net	+/-0.00V
ctrl_a_reg_5L	default	Transfer Net	+/-0.00V
dm_1R	A	Transfer Net	+/-0.0V
dq_1R	A	Transfer Net	+/-0.0V
dqs_1R	A	Transfer Net	+/-0.0V

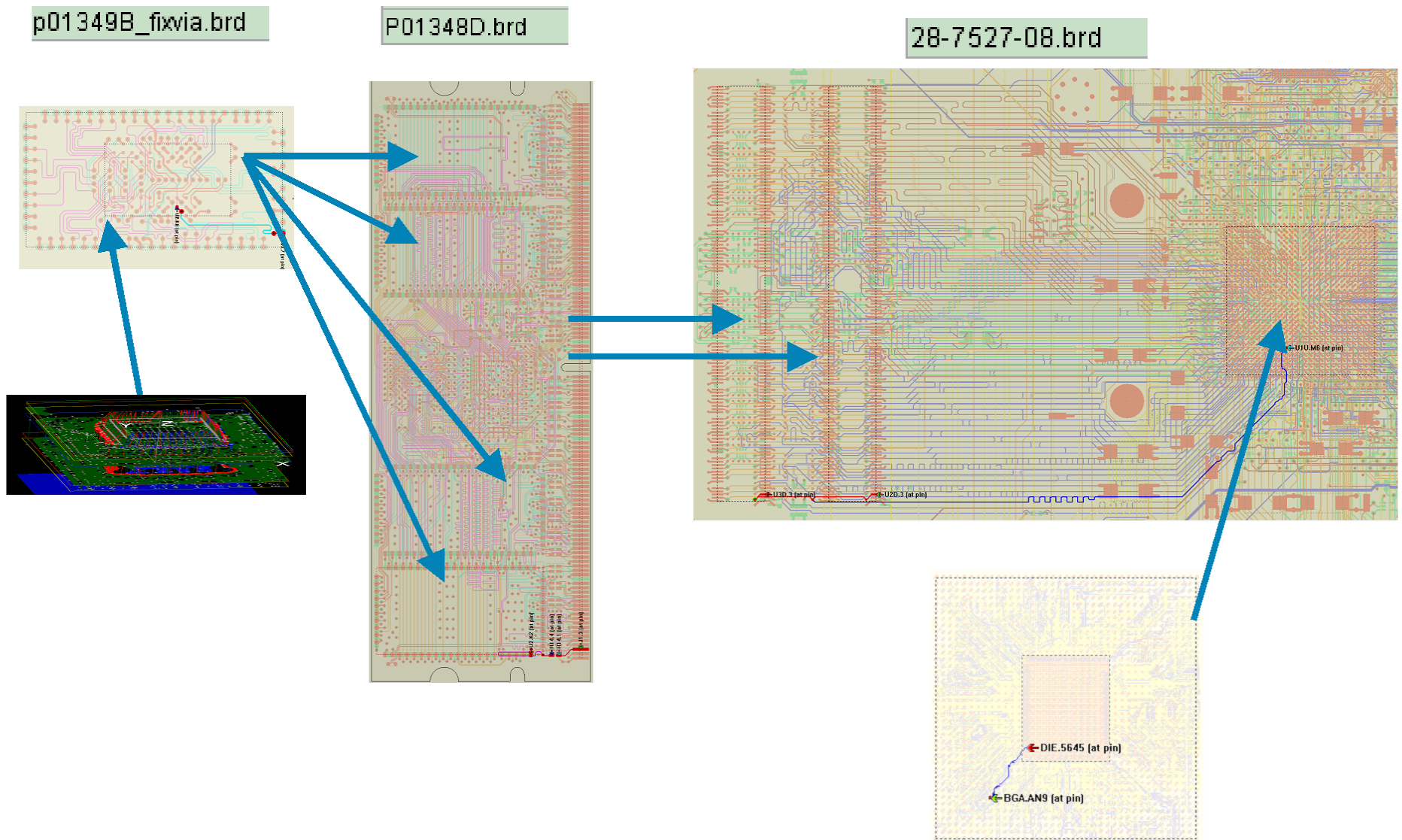
12985\_08\_2006\_c2 © 2006 Cisco Systems, Inc. All rights reserved. Cisco Confidential

27

# Multi Board Extractions with QSI



# Multi Board Extractions with QSI



# Transfer Nets in QSI

**Transfer Net Properties**

**Transfer Nets:**

Transfer Net	Clock Domain	Data Rate	Switching Frequency	Type	Mode	Source Probe Points	Target Probe Points	Jitter	Uncorrelate Etch Facto
dm_1R	ddr2_dq_rate	2.5ns	400.0MHz	Data	Single_Ended	SL_pad	pad	N/A	
<b>dq_1R</b>	<b>ddr2_dq_rate</b>	<b>2.5ns</b>	<b>400.0MHz</b>	<b>Data</b>	<b>Single_Ended</b>	<b>SL_pad</b>	<b>pad</b>	<b>N/A</b>	
dqs_1R	ddr2_dqs_rate	2.5ns	400.0MHz	Strobe	Differential	SL_pad	pad	0	

**Nodes:**

Designator	Subcircuit Port	Part	Pin Names	Model	Model Type
ddr2_controller	ddr2_controller	freescala	MDQ[[63:0]],MDQS[[8:0]],MDQS_B[[8:0]],MECC[[7:0]]	ddr2_io_full	I/O
ddr2_sdram	ddr2_sdram	ddr2_sdram	DQ[7:0],DQS,DQS#	DQFULL_533	I/O
ddr2_sdram1	ddr2_sdram1	ddr2_sdram	DQ[7:0],DQS,DQS#	DQFULL_533	I/O

[Edit Designator Properties](#)

**Transfers:**

Source(s)	Target(s)	From	To	Timed From
ddr2_controller	ddr2_controller	ddr2_contr...	<b>ddr2_sdram</b>	ddr2_contr...
ddr2_sdram	ddr2_sdram	ddr2_contr...	ddr2_sdra...	ddr2_contr...
ddr2_sdram1	ddr2_sdram1	ddr2_sdram	ddr2_contr...	ddr2_sdram
		ddr2_sdra...	ddr2_contr...	ddr2_sdra...

**Transfer Model Overrides:**

Designator	Model
ddr2_controller	ddr2_io_half
ddr2_sdram	DQHALF_800
ddr2_sdram1	DQHALF_ODT75_...

# Stimulus Setup in QSI

```

rise_time           100pS           T:
character_time      100pS           U:

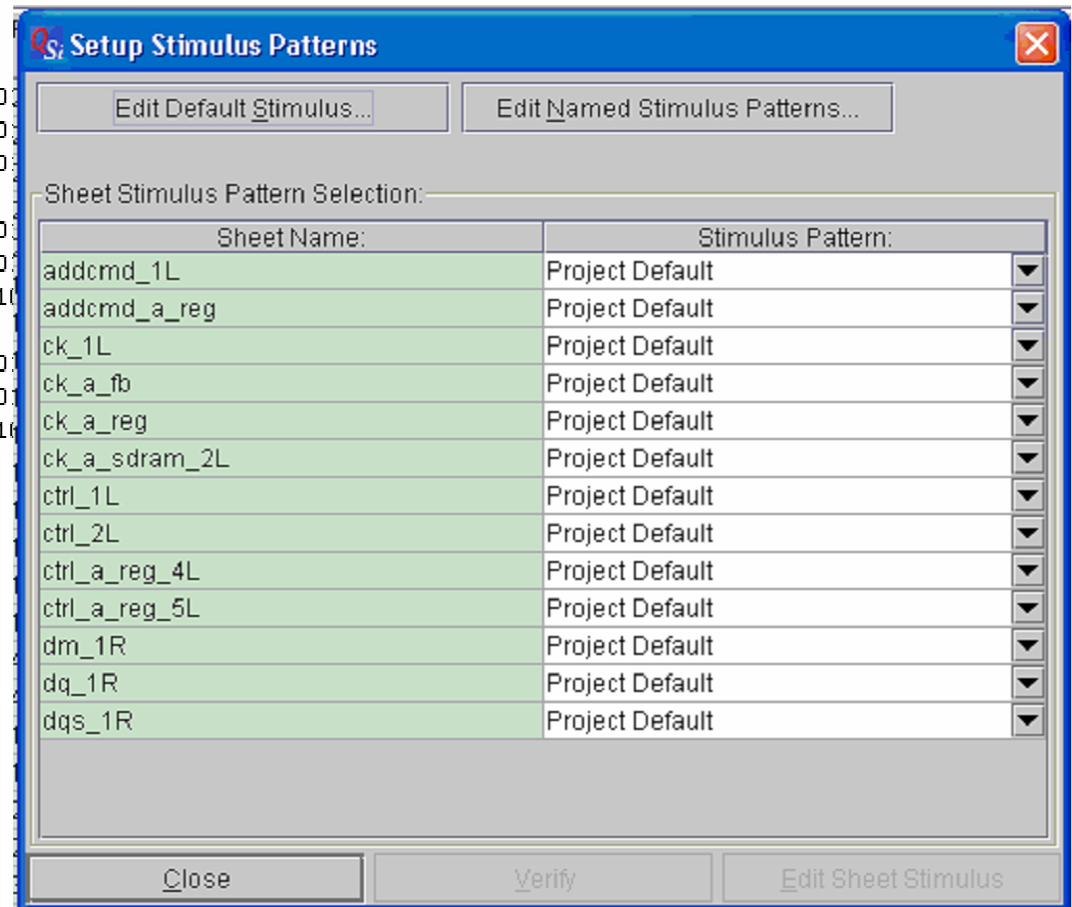
*data               0110010101

* PRBS

data                000001011001000111110100110
data_victim         010101010101010101010101010
data_aggressor      000001011001000111110100110

clock               010101010101010101010101010
clock_victim        010101010101010101010101010
clock_aggressor     1010101010101010101010101010

strobe              010101010101010101010101010
strobe_victim       010101010101010101010101010
strobe_aggressor   1010101010101010101010101010
  
```



# Waveform and Timing Report

	A	B	C	D	E	F	G	H	I	J	K	L	M	N
1	Setup Margin (ns)	Hold Margin (ns)	Rmin Etch Delay (ns)	Rmax Etch Delay (ns)	Fmin Etch Delay (ns)	Fmax Etch Delay (ns)	Transfer Net							
2	No AC specs	No AC specs	1.072	1.373	1.072	1.373	PRE_PLL_CLK							
3	No AC specs	No AC specs	0.403	0.617	0.403	0.613	PLL_SDRAM_CLK							
4	No AC specs	No AC specs	0.358	0.627	0.36	0.632	pll_reg_clk							
5	No AC specs	No AC specs	0.38	0.552	0.381	0.55	PLL_FDBK							
6	0.037	0.784	1.331	1.71	1.331	1.71	DQS_ECC_2R_2Slot							
7	0.153	0.585	1.206	1.616	1.205	1.614	DQS_2R_2Slot							
8	0.828	1.01	1.037	1.511	1.072	1.412	Pre_reg_cmd_slot1							
9	0.807	1.03	1.153	1.675	1.189	1.575	Pre_reg_cmd_slot2							
10	0.375	1.127	1.154	1.907	1.195	1.748	Pre_reg_CS							
11	0.617	1.006	1.033	1.865	1.067	1.744	Pre_reg_addcmd							
12	0.344	0.232	1.132	1.795	1.143	1.741	DQ_2R_2Slot							
13	0.395	0.305	1.293	1.662	1.294	1.603	DM_2R_2Slot							
14	1.223	1.411	0.827	1.244	0.771	1.312	Post_reg_addcmd_LB							
15	1.169	1.255	0.756	1.34	0.623	1.376	Post_reg_addcmd_RB							
16	1.442	1.228	0.701	1.091	0.615	1.08	Post_Reg_CTRL_4L							
17	0.875	1.356	0.819	1.592	0.733	1.656	Post_Reg_CTRL_5L							
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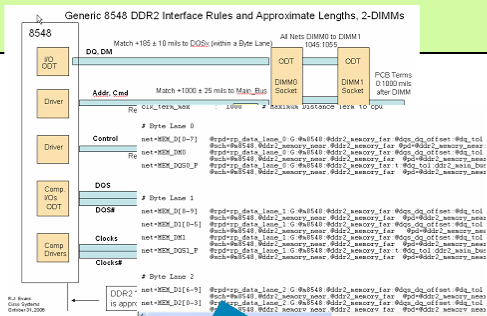
[Waveform Quality](#) / 
 [Waveform Overshoot](#) / 
 [Eye Rollups](#) / 
 [Eye Details](#) / 
 [Waveform Margin By Tnet](#) / 
 [Waveform Margin By Variation](#) / 
 [Model Overview](#) / 
 [Timing An:](#)

Ready NUM

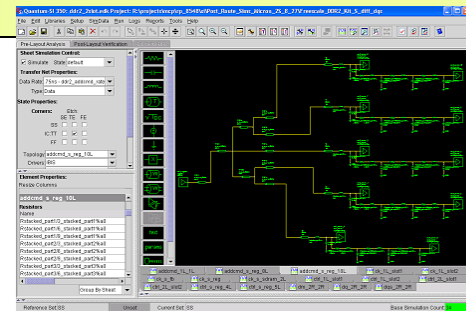


# Design Kit Strategy for Reuse

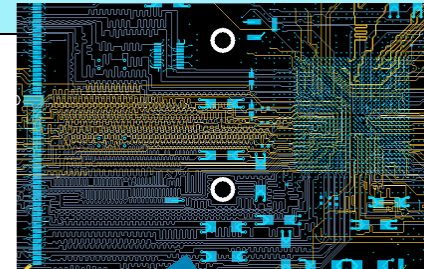
## Design Constraints



## SiSoft Interface Design Kit Pre- & Post-Route



## ECAD Interface CAD Clip



## HSD Web-based Repository

# Summary

- Definition of HSD
- Static Timing Analysis for DDR
- Pre-route simulations (Scan the design space)
- Routing Rules development for CAD
- Full post route simulations
- Summary



# References

- SiSoft-Micron Web based Presentation,  
“Bowling for Picoseconds Integrating DDR2/DDR3 Timing”
- Micron DDR2 Datasheet  
<http://download.micron.com/pdf/datasheets/dram/ddr2/256MbDDR2.pdf>
- JEDEC DDR2 Spec: JESD79-2C  
<http://www.jedec.org/download/search/JESD79-2C.pdf>
- Micron DDR2 Datasheet  
<http://download.micron.com/pdf/datasheets/dram/ddr2/1GbDDR2.pdf>
- SiSoft-Micron DDR2 Paper  
<http://www.sisoft.com/papers.asp>

- Dear IEEE RTP EMC Chapter members:

Our next meeting is on Tuesday, September 4, 2007 at Underwriter's Laboratory. 5:30 PM is the start time. Below is an abstract of the presentation and Steven Scearce's biography. If interested, please RSVP. Food will be served. Mark your calendar and hope to see you there.

**Presentation Abstract:** PCB level SI tools and strategy

I will discuss the current tools and strategy my team uses use for PCB level high speed design. We can follow the design flow from the pre route simulation/ rule development, to the full post route verification of the design. Specifically we will examine use of the SiSoft tool for control of the Spice simulations and timing of the design for a DDR2 implementation.

**Author Biography:**

Stephen Scearce is currently is working as the manager of the High Speed Design team at Cisco System Inc, and has worked in HSD team as a signal integrity engineer for 4 years at Cisco. Before joining the central HSD team, Stephen worked for the Cisco ATG as an EMC/Safety/NEBS designer. Prior to working at Cisco, Stephen worked for NASA LaRC as a research engineer in the Electromagnetics research branch HIRF team. His research interests include power integrity and signal integrity full channel design (Die to Die). Stephen has 3 US patents and 2 pending patents. He received his BS and MSEE from Old Dominion University, Norfolk VA.

Sincerely,

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