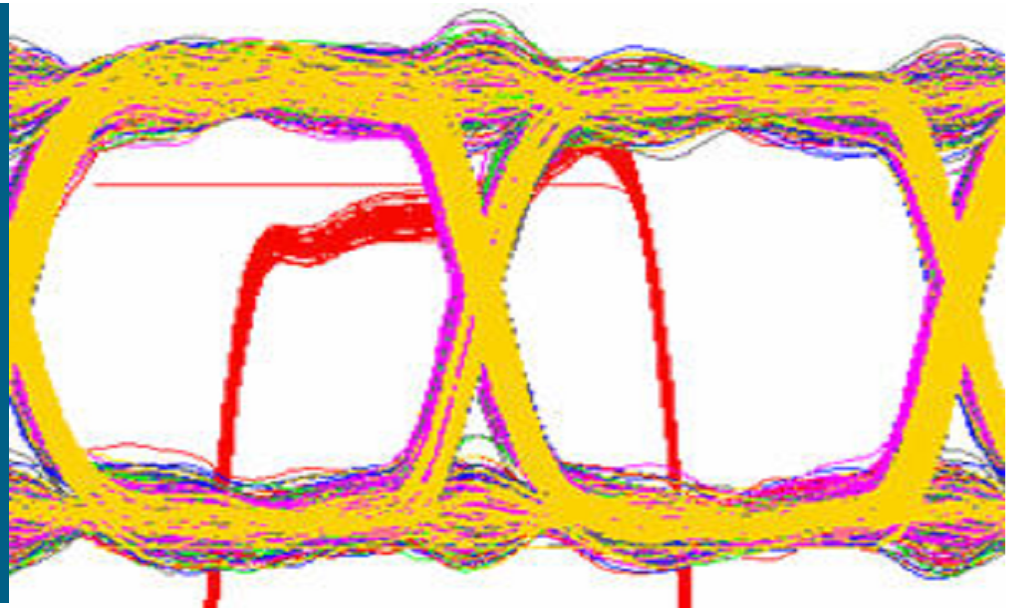
PCB level SI tools and strategy



Stephen Scearce
High Speed Design Team Manager
Cisco Systems Inc, RTP NC

Q1 FY 2008

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PCB level SI tools and strategy

- Definition of HSD
- Static Timing Analysis for DDR
- Pre-route simulations (Scan the design space)
- Routing Rules development for CAD
- Full post route simulations
- Summary

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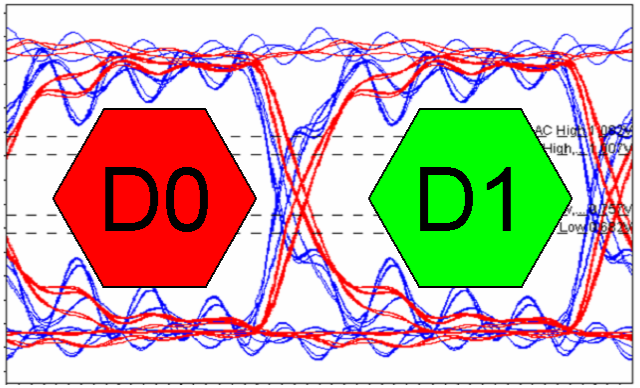
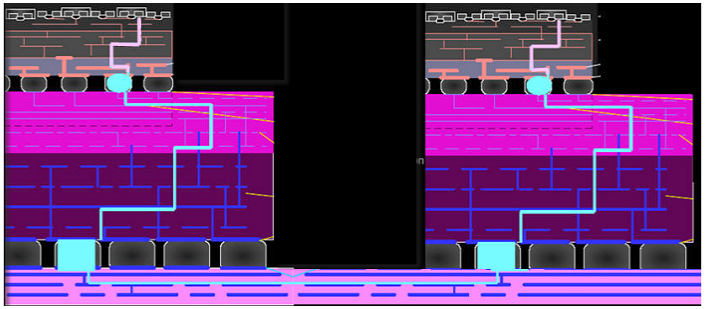
What Is *High Speed Design?*

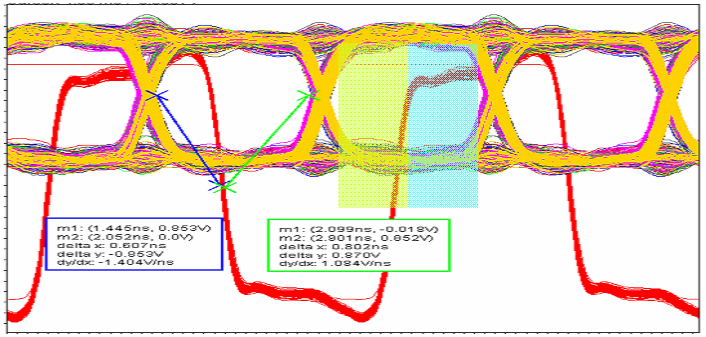
Getting the right data



To the right place



At the right time



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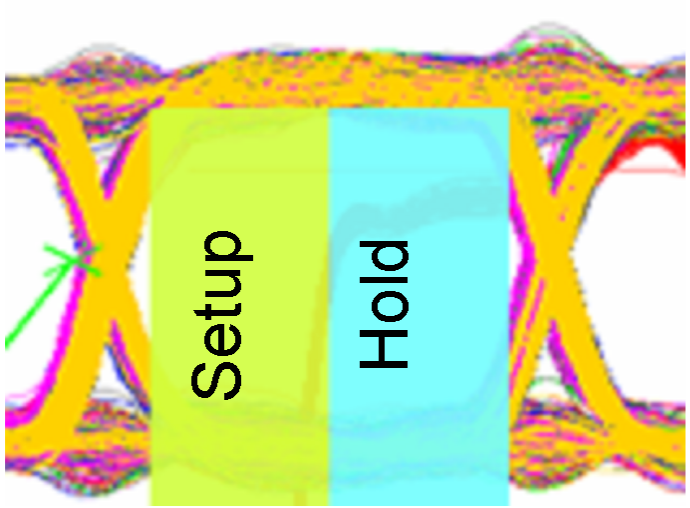
High Speed Design is the study of analog effects on Timing



- Component timing (process)
- Voltage
- Temperature
- Package & PCB routing lengths
- PCB manufacturing variations (Z_0, loss)
- Reflection/Overshoot
- ISI
- SSN/SSO
- Crosstalk…

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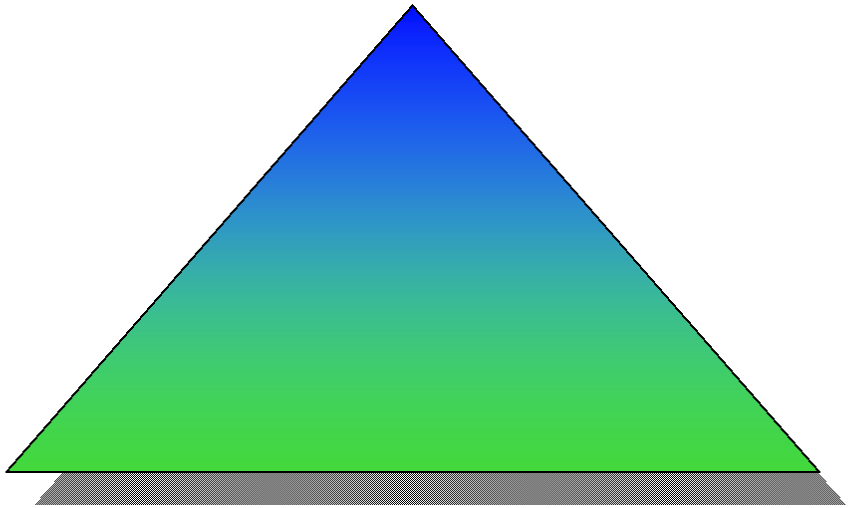
High Speed Design

Constraint-Driven Design



Static Timing Analysis

Signal & Power Integrity Analysis

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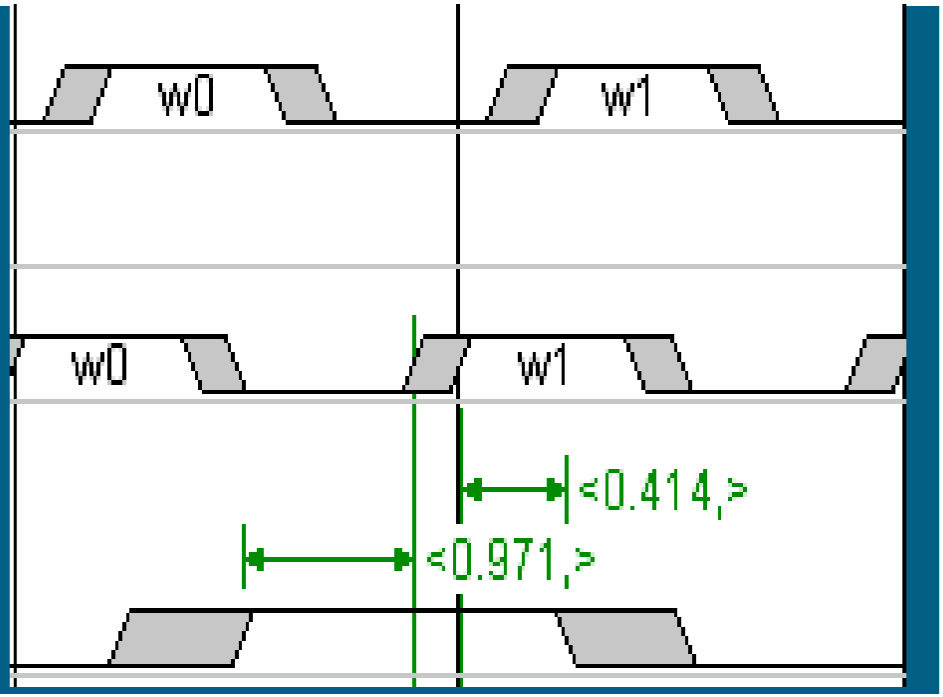
Static Timing Analysis



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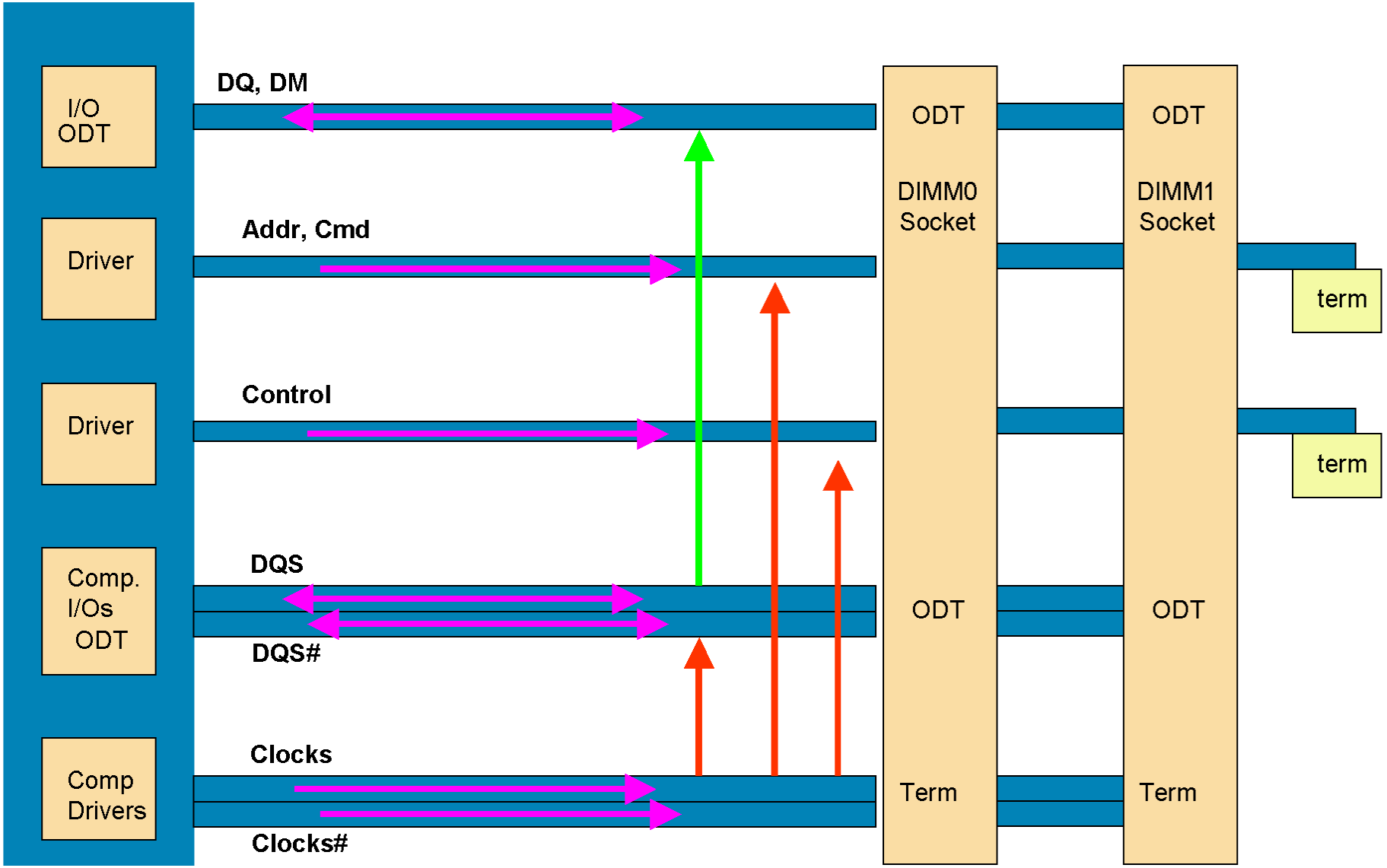
Timing Budget for DDR2



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Develop a Static Timing Model

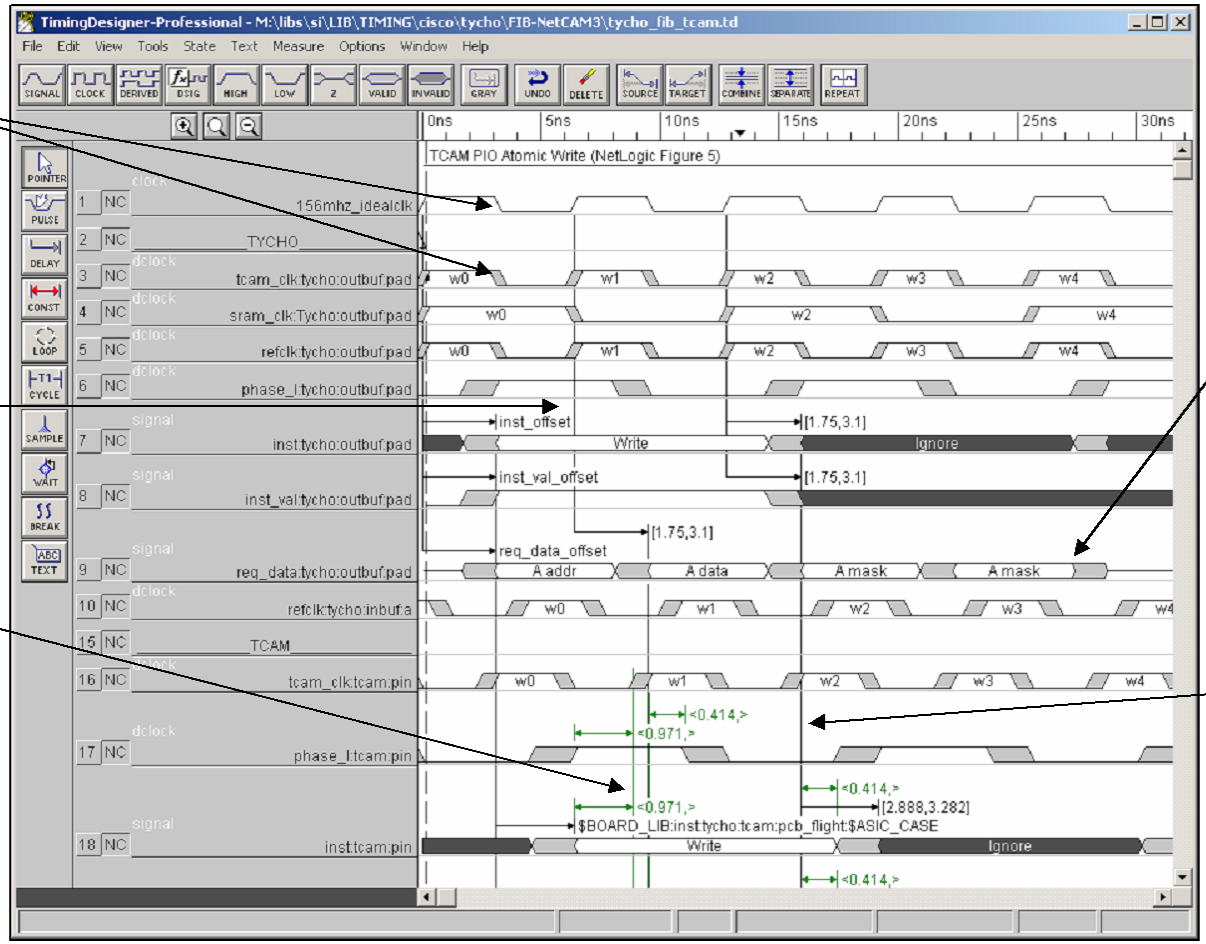
Clocks and characteristics

Output timing

Input requirements

Bus protocol

Connectivity & delays



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STA for DDR2 is based on vendors datasheet (which are JESD79-2C based)

256Mb: x4, x8, x16 DDR2 SDRAM
AC Operating Specifications

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 4 of 6)
Notes: 1–5; notes appear on page 125; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC Characteristics		-3E		-3		-37E		-5E		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Address and control input pulse width for each input	^{t}IPW	0.6		0.6		0.6		0.6		^{t}CK	37
Address and control input setup time	$^{t}IS_a$	400		400		500		600		ps	6, 19
Address and control input hold time	$^{t}IH_a$	400		400		500		600		ps	6, 19
Address and control input setup time	$^{t}IS_b$	200		200		250		350		ps	6, 19
Address and control input hold time	$^{t}IH_b$	275		275		375		475		ps	6, 19

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DDR2 Timing

- Data Sheet Timing is with respect to a specific load
  - Reference: 25 ohms to VDDQ/2
  - Timing measured to Vref
- Device timing is measured with respect to thresholds
  - Dependant on operating frequency
  - IO type used (DM_INPUT_533/DQFULL_533, INPUT_533(ADDR)
  - Specific edge (Rising, Falling)
  - Slew rates of the signals

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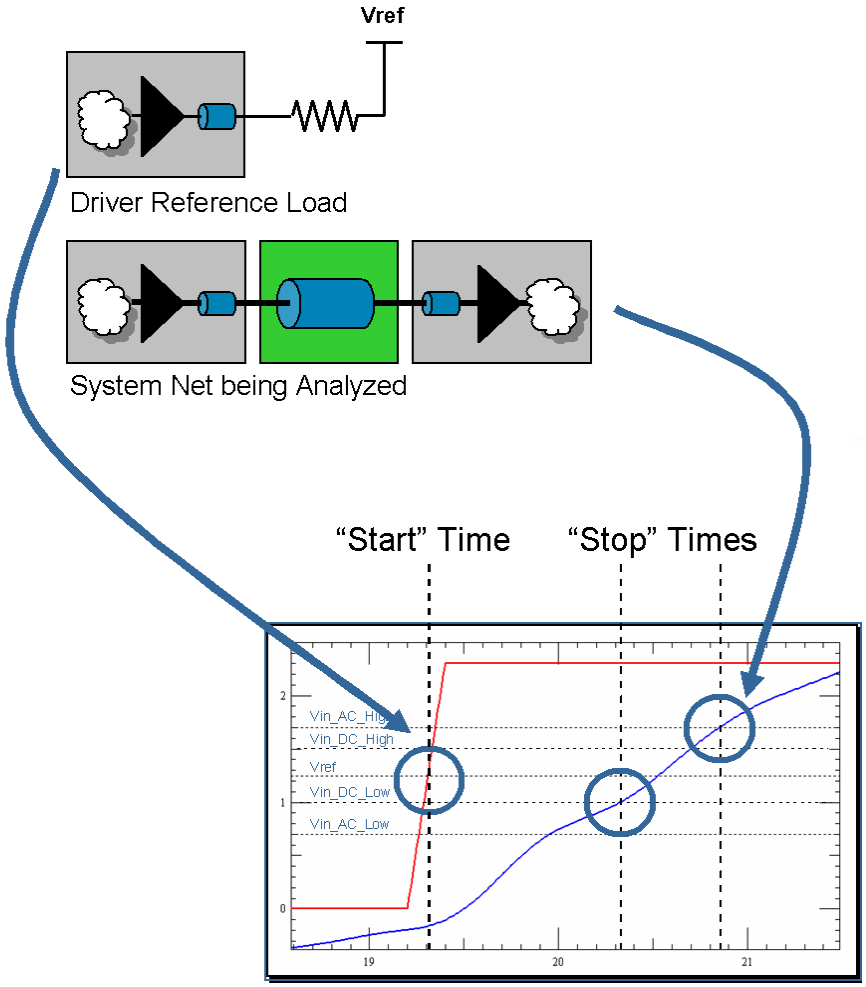
Data Sheet Timing and Interconnect Delays



- Interconnect delays from simulations have *start* and *stop* times
  - *Start* times are based on output timing specs
    - Reference loads and voltage levels
    - IBIS Vref, Cref, Rref, Vmeas
  - *Stop* times are based on input (setup/hold) timing specs
    - Measured at defined voltage levels and slew rates

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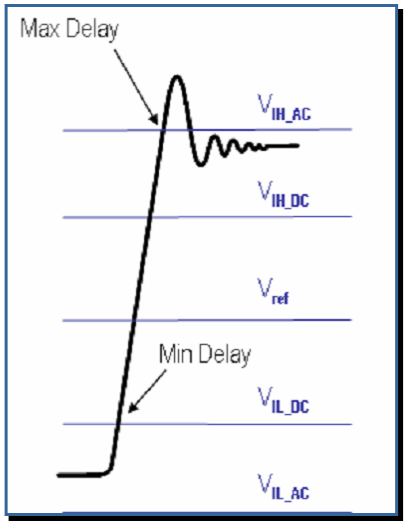
Device timing (DQ Signals)

Note: Guard bands not shown



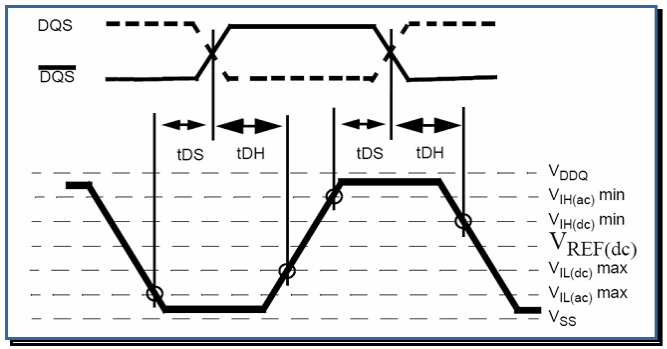
SI View

Quality

- A rising edge must:
  - Start below VIL_DC
  - Switch through VIH_AC
  - Settle above VIH_DC

Timing

- **MIN** delay measured at first crossing of VIL_DC
  - Used to compute hold margin
  - JESD79-2C, page 96, note 21
- **MAX** delay measured at first crossing of VIH_AC
  - Used to compute setup margin
  - JESD79-2C, page 96, note 20



Timing Spec View

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Timing files to implement STA

```
#  667 DDR2 parts running at 667 DDR2
   ADDCMD_SETUP = 0.200
   ADDCMD_HOLD  = 0.275

   CTRL_SETUP = 0.200
   CTRL_HOLD  = 0.275

   DQ_SETUP = 0.100
   DQ_HOLD  = 0.175

   tQHS_SKEW_MAX =   0.340
   tDQSQ_SKEW_MAX =   0.240

#DQ Write timing
 SETHLD  DQ *TO R DQS  DQ_SETUP
          DQ_HOLD

 SETHLD  DQ *TO F DQS  DQ_SETUP
          DQ_HOLD
```


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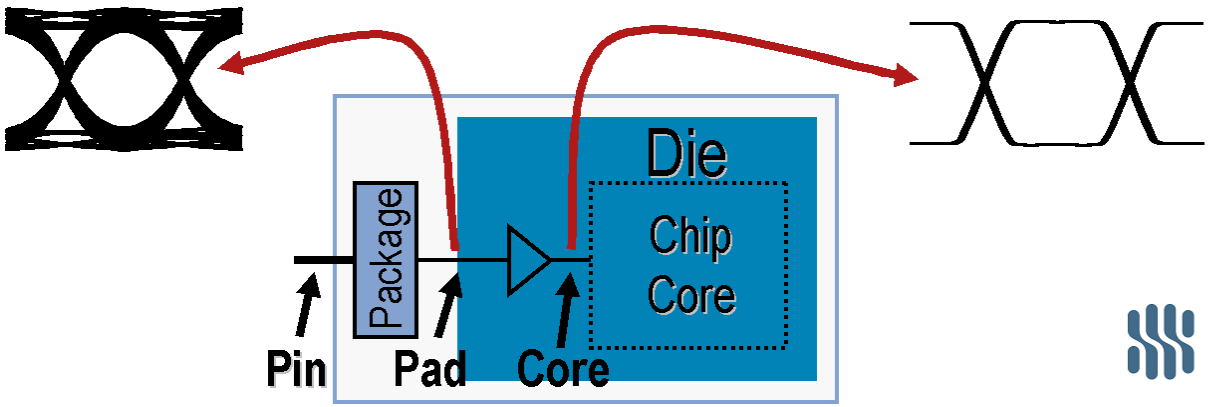
DDR2 Slew Rate Derating

- Baseline setup/hold requirements are based on specific voltage and slew rate conditions
- System slew rates rarely conform to measurement conditions
  - Loading can vary widely within the same system
- DDR2 slew-rate derating defines adjustments to setup/hold specs based on actual slew rates of input signals



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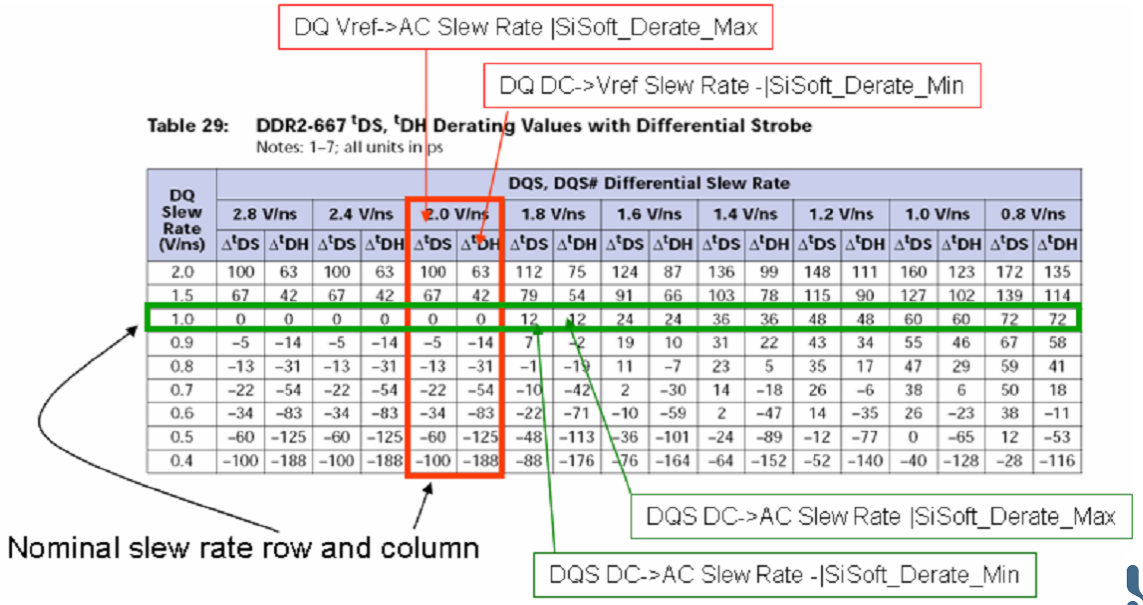
SiSoft's Slew Rate Methodology

- Device setup/hold times based on nominal (base) values
- Derating tables converted into independent derating values for DQ and DQS nets
- Derating info included in simulation models – measurements & adjustments are automated



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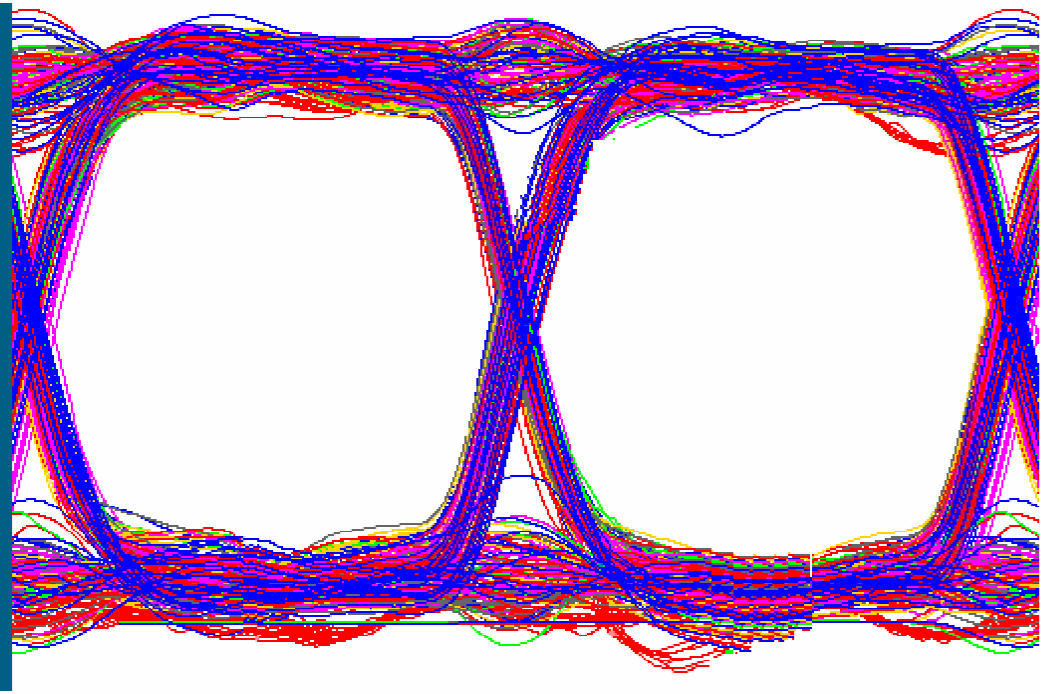
Pre-route simulations



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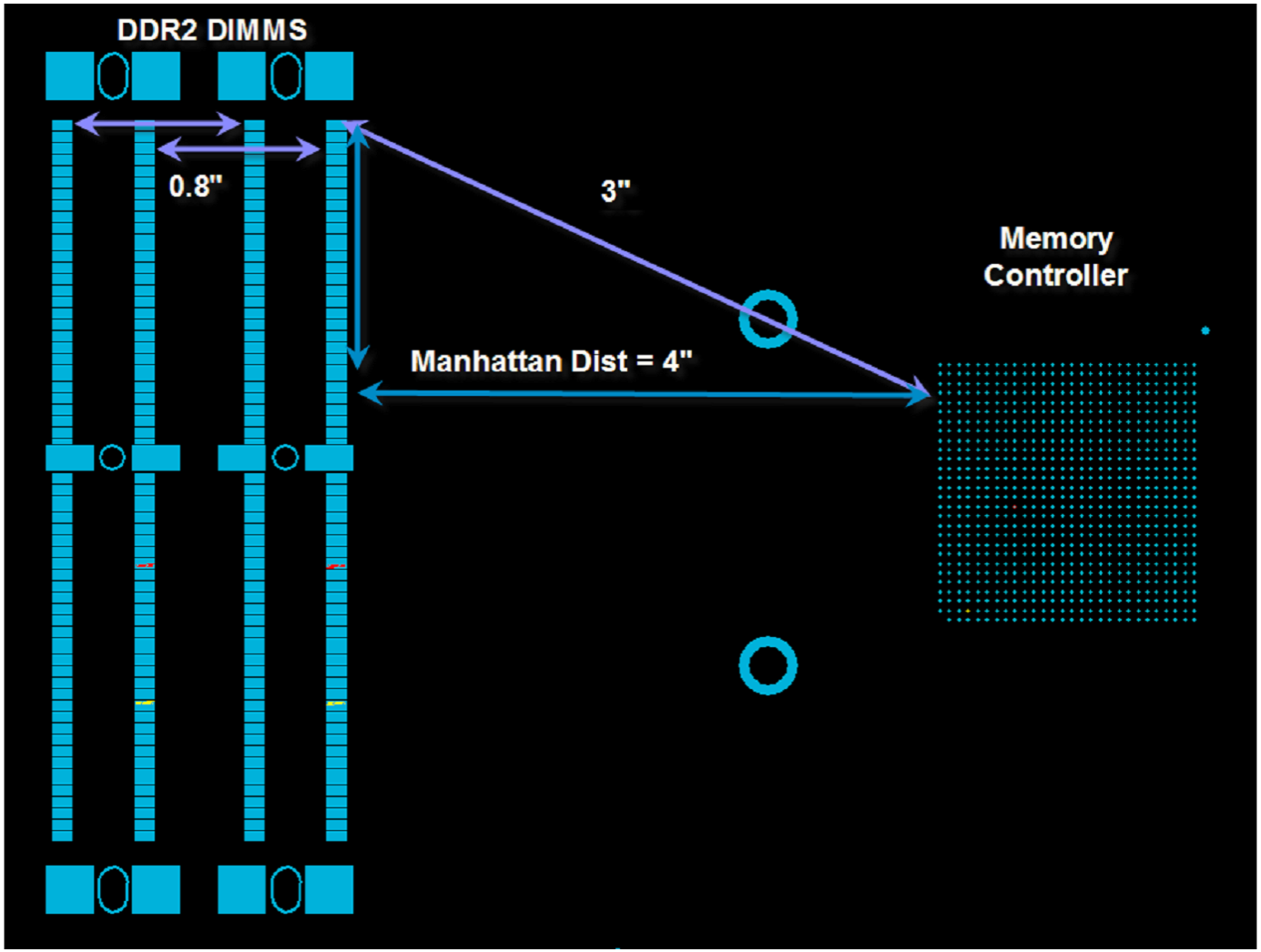
PCB component placement



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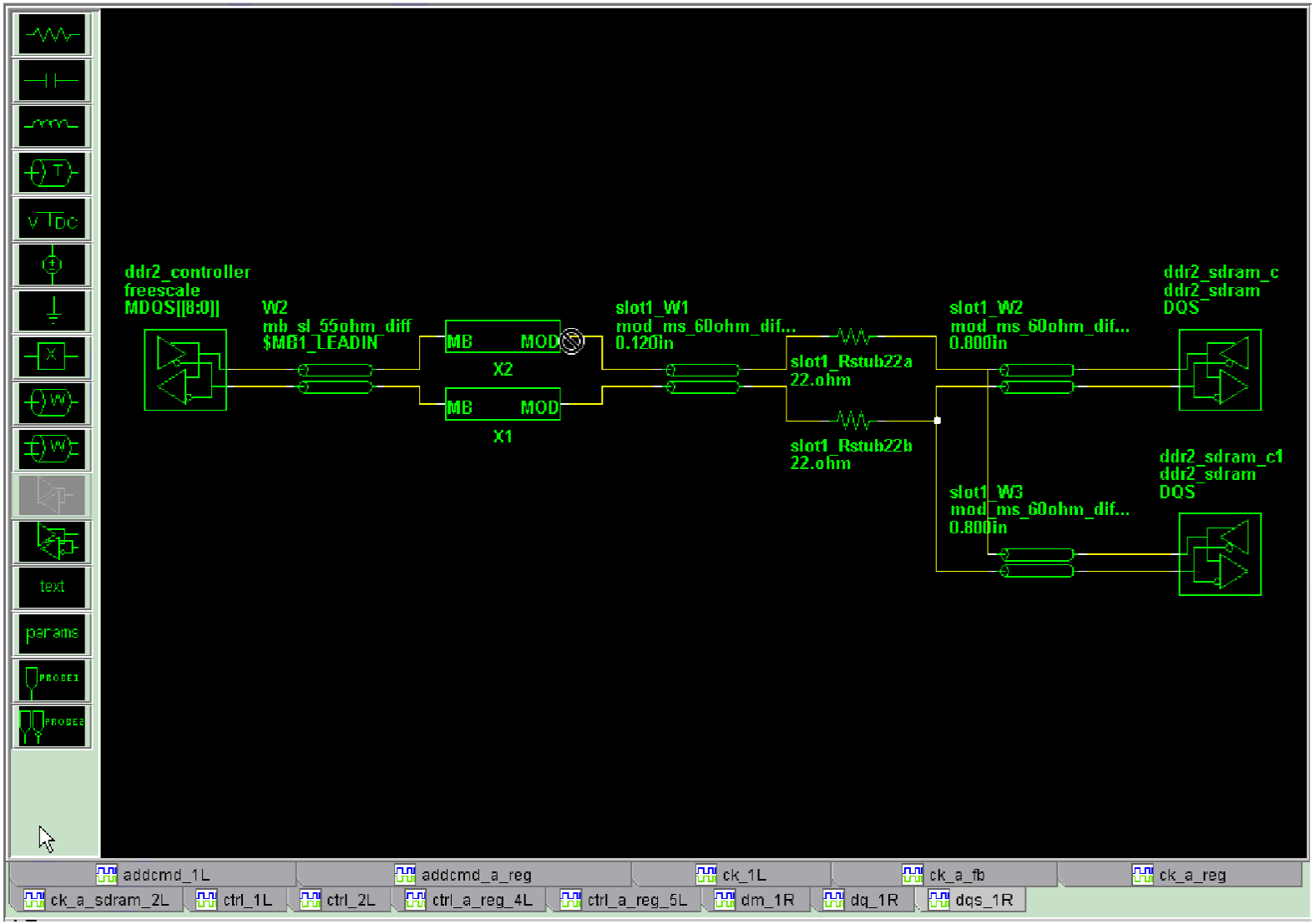
Topologies for current placement



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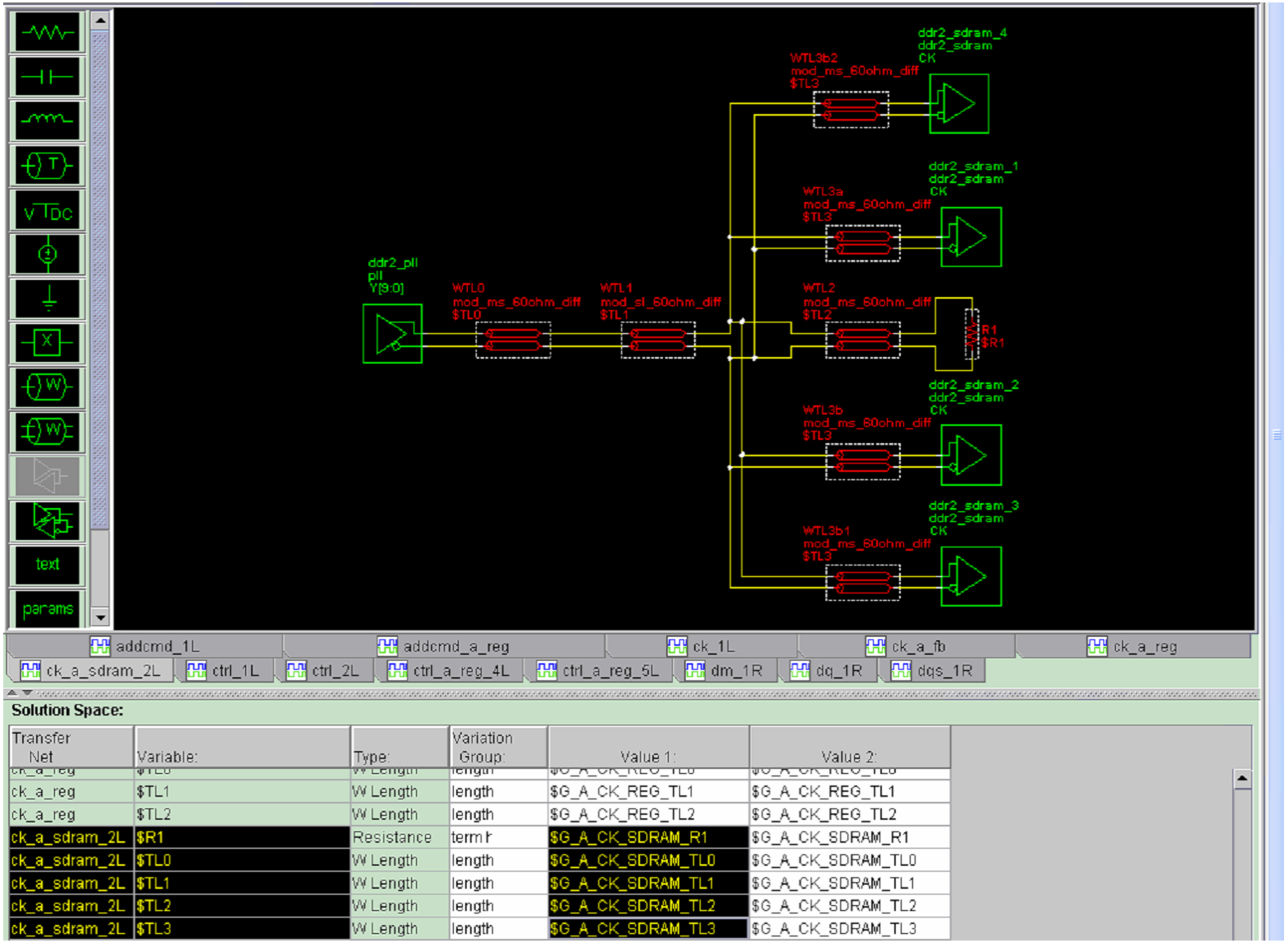
Extracted Topologies add sweep variables for Cad constraints, and select ODT settings



Solution Space:

Transfer Net	Variable:	Type:	Variation Group:	Value 1:	Value 2:
ck_a_reg	$TL1	W Length	length	$G_A_CK_REG_TL1	$G_A_CK_REG_TL1
ck_a_reg	$TL2	W Length	length	$G_A_CK_REG_TL2	$G_A_CK_REG_TL2
ck_a_sdram_2L	$R1	Resistance	term r	$G_A_CK_SDRAM_R1	$G_A_CK_SDRAM_R1
ck_a_sdram_2L	$TL0	W Length	length	$G_A_CK_SDRAM_TL0	$G_A_CK_SDRAM_TL0
ck_a_sdram_2L	$TL1	W Length	length	$G_A_CK_SDRAM_TL1	$G_A_CK_SDRAM_TL1
ck_a_sdram_2L	$TL2	W Length	length	$G_A_CK_SDRAM_TL2	$G_A_CK_SDRAM_TL2
ck_a_sdram_2L	$TL3	W Length	length	$G_A_CK_SDRAM_TL3	$G_A_CK_SDRAM_TL3

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Verify the pre-route timing across case

Setup Margin (ns)	Hold Margin (ns)	Rmin Etch Delay (ns)	Rmax Etch Delay (ns)	Fmin Etch Delay (ns)	Fmax Etch Delay (ns)	Transfer Net
0.037	0.784	1.331	1.71	1.331	1.71	DQS_ECC_2R_2Slot
0.153	0.585	1.206	1.616	1.205	1.614	DQS_2R_2Slot
0.828	1.01	1.037	1.511	1.072	1.412	Pre_reg_cmd_slot1
0.807	1.03	1.153	1.675	1.189	1.575	Pre_reg_cmd_slot2
0.375	1.127	1.154	1.907	1.195	1.748	Pre_reg_CS
0.617	1.006	1.033	1.865	1.067	1.744	Pre_reg_addcmd
0.344	0.232	1.132	1.795	1.143	1.741	DQ_2R_2Slot
0.395	0.305	1.293	1.662	1.294	1.603	DM_2R_2Slot
1.223	1.411	0.827	1.244	0.771	1.312	Post_reg_addcmd_LB
1.169	1.255	0.756	1.34	0.623	1.376	Post_reg_addcmd_RB
1.442	1.228	0.701	1.091	0.615	1.08	Post_Reg_CTRL_4L
0.875	1.356	0.819	1.592	0.733	1.656	Post_Reg_CTRL_5L

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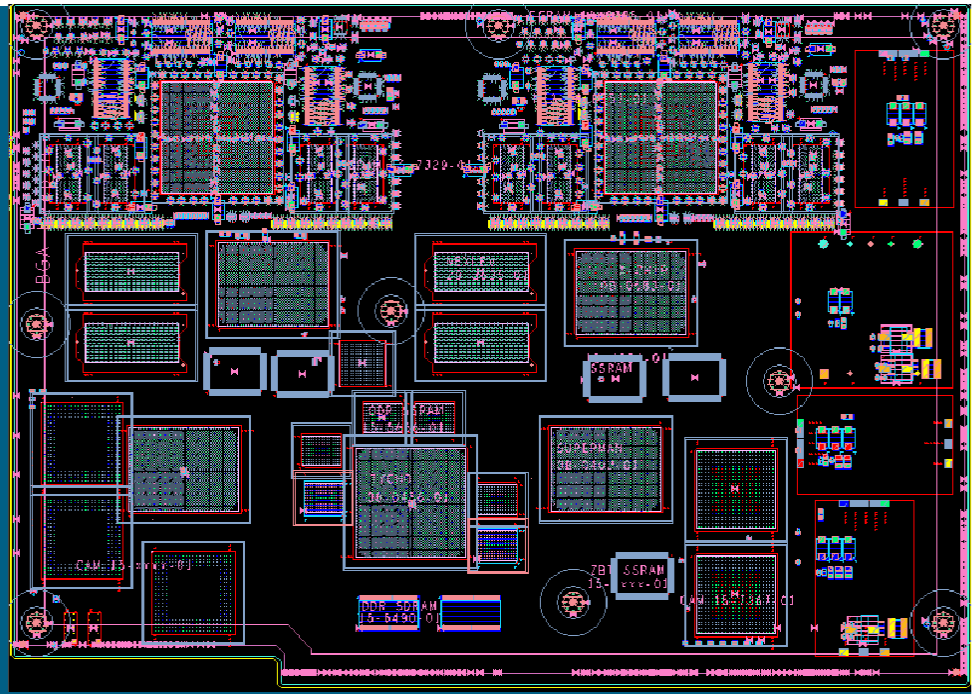
Routing Rules development for CAD



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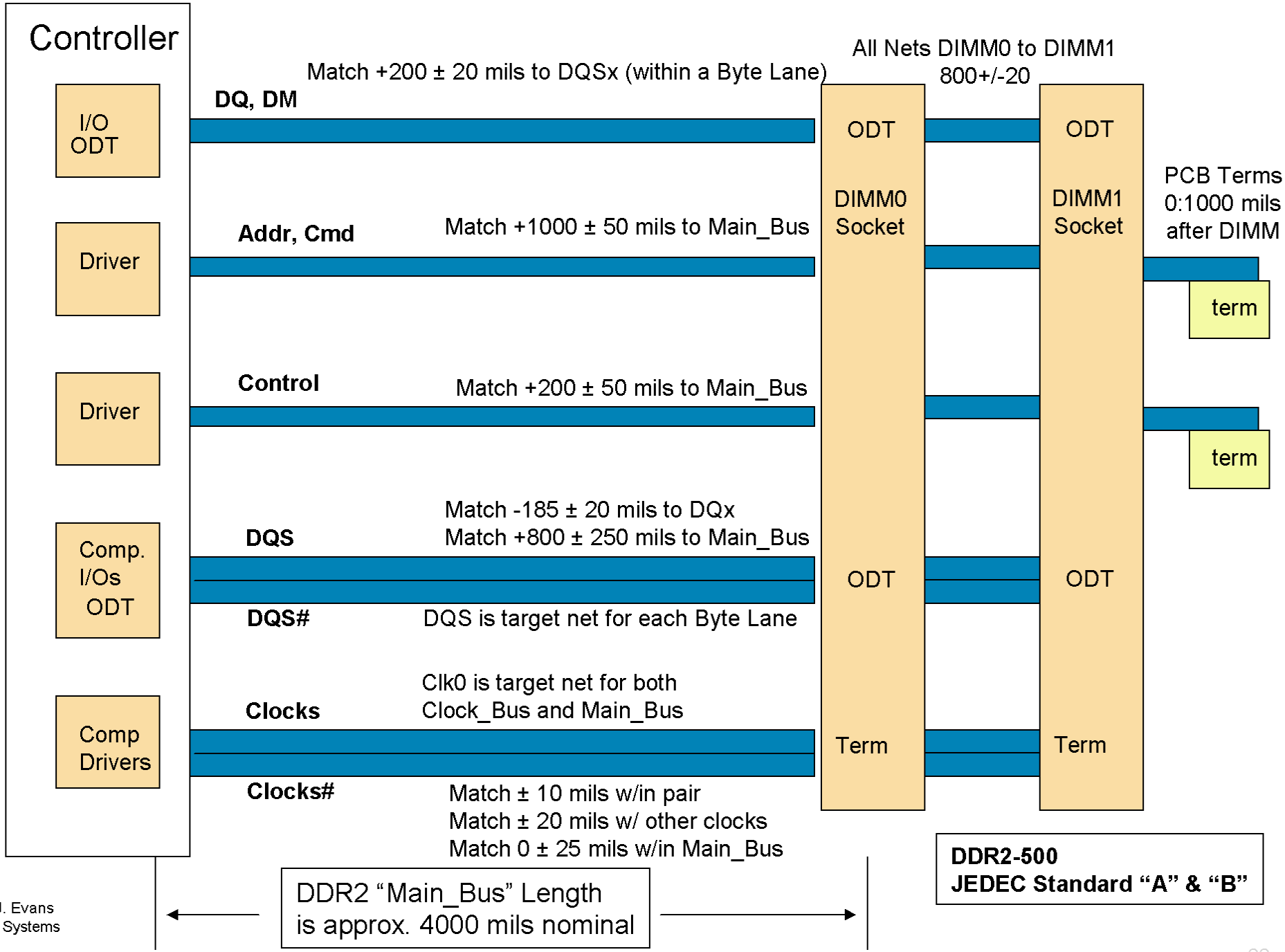

Dr R.J. Evans
Cisco Systems

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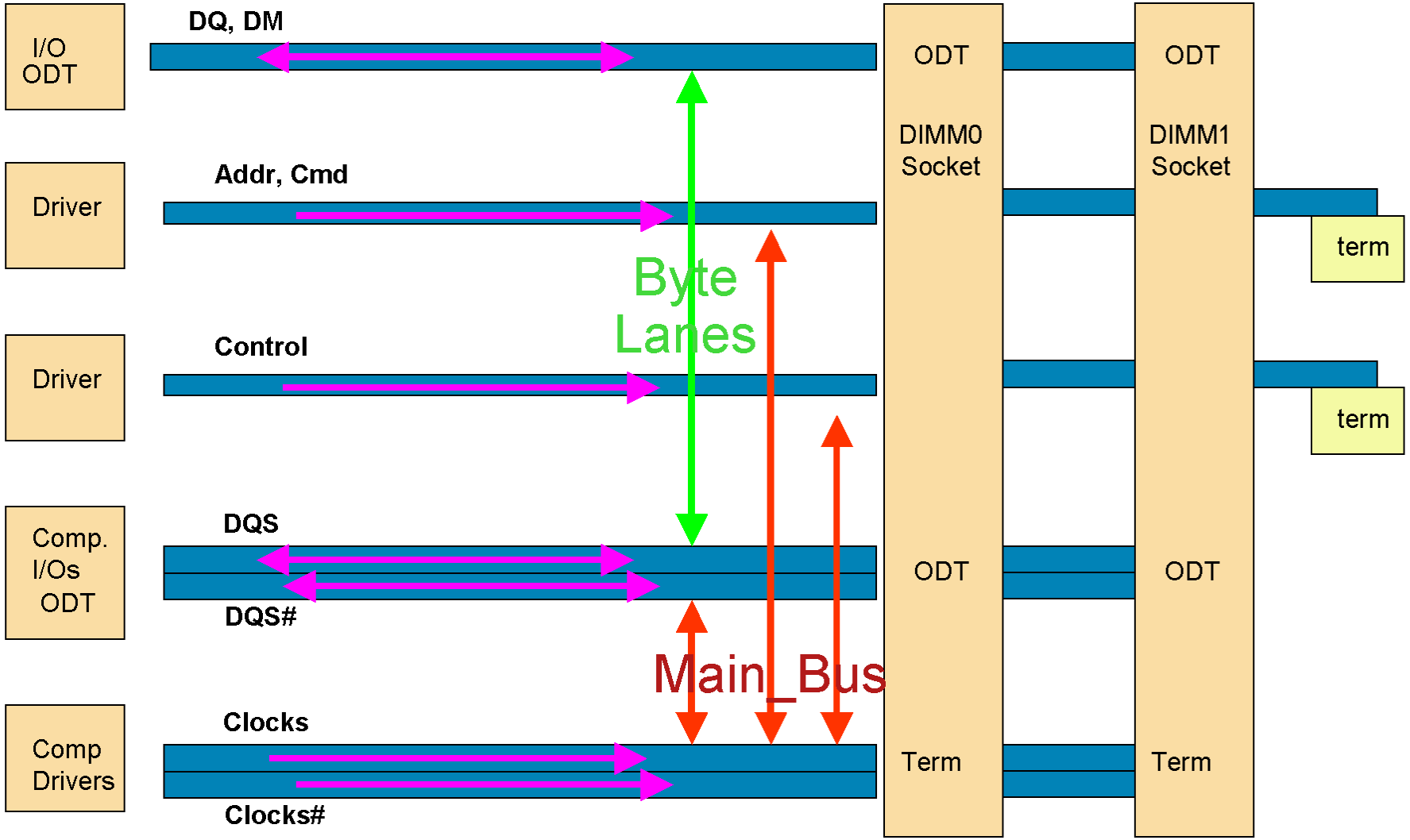
Define rule sets to meet Timing



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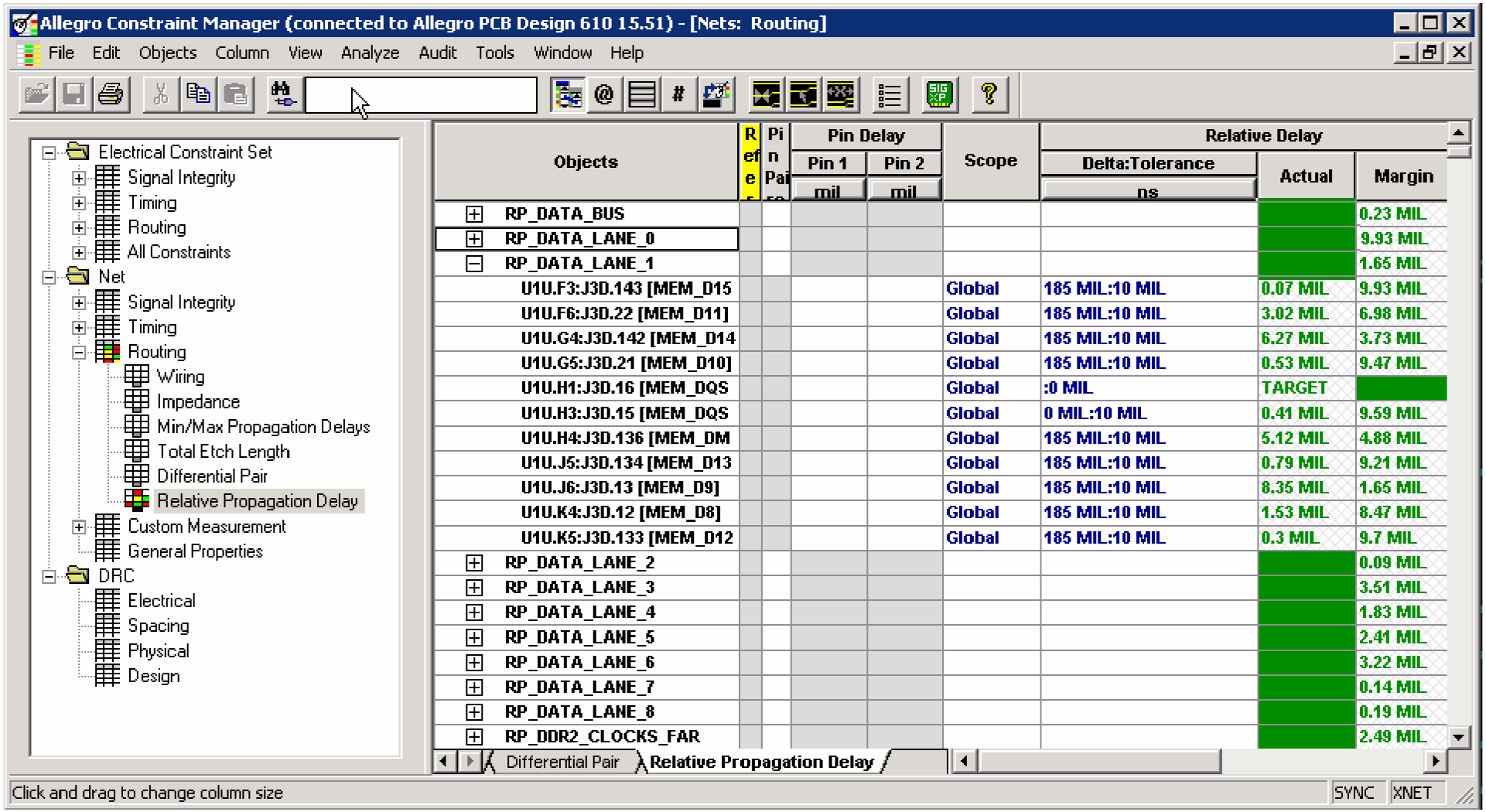
Rules in Allegro CMS



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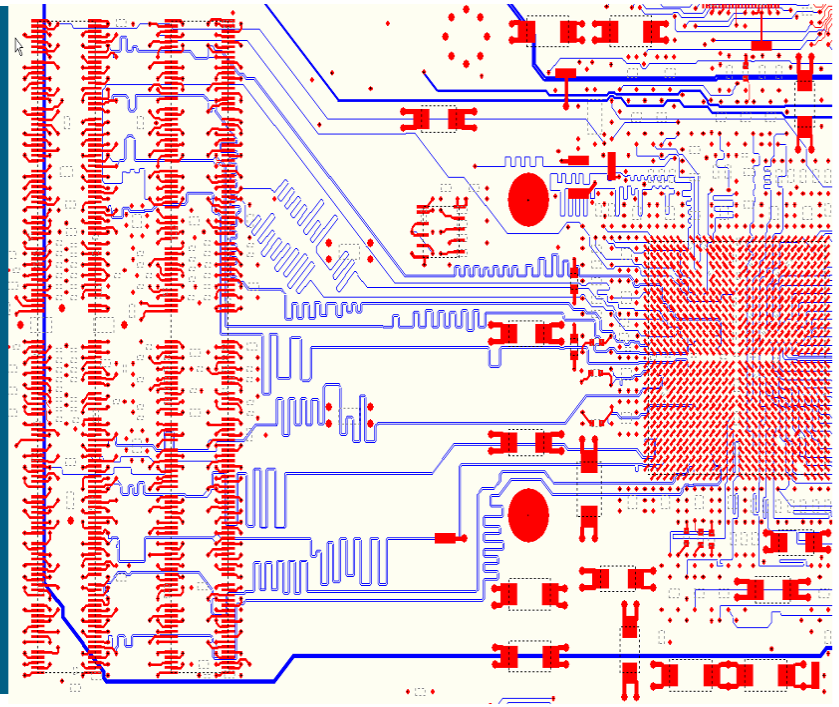
Post Route Simulations



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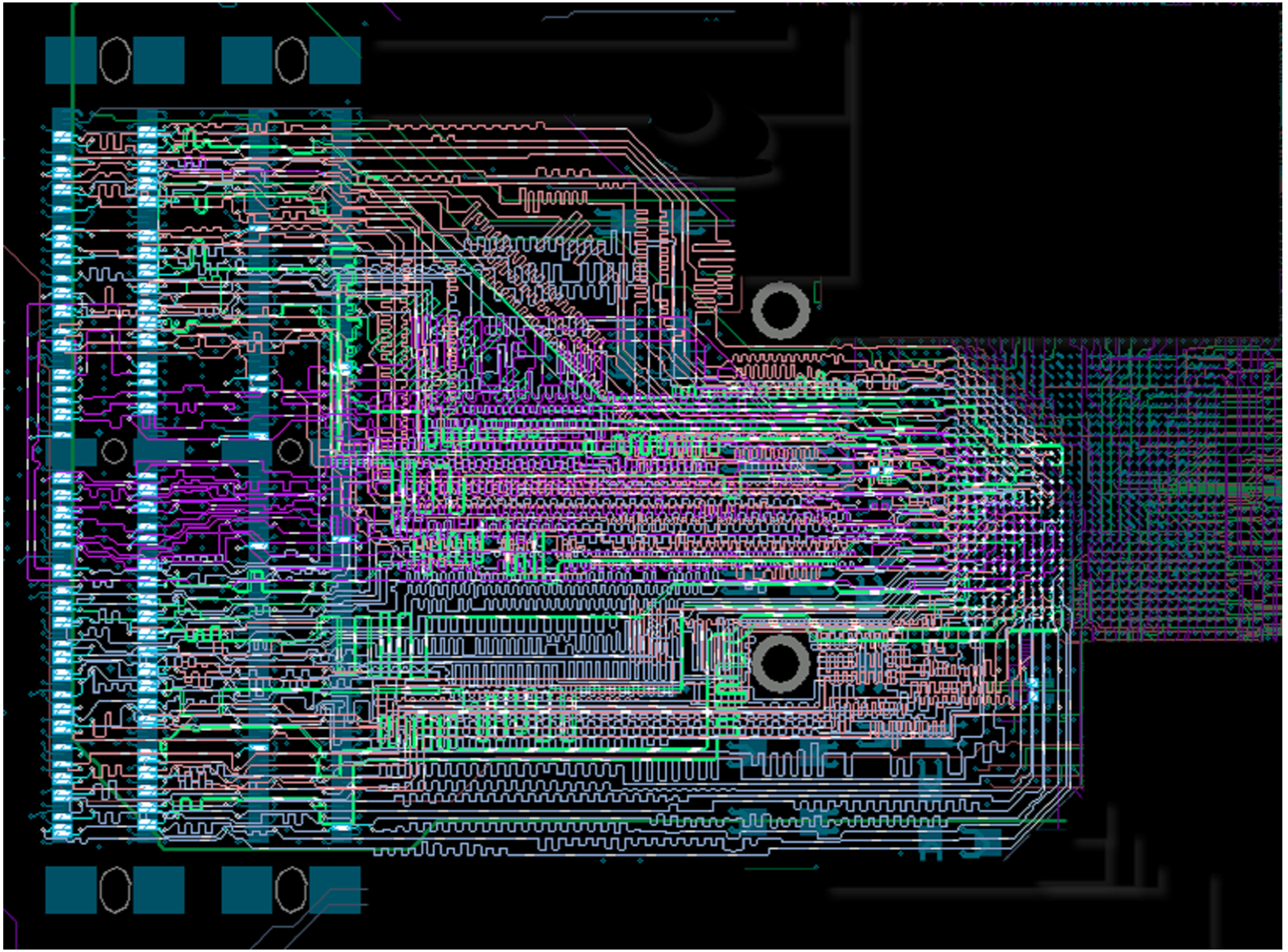
Fully routed Allegro design



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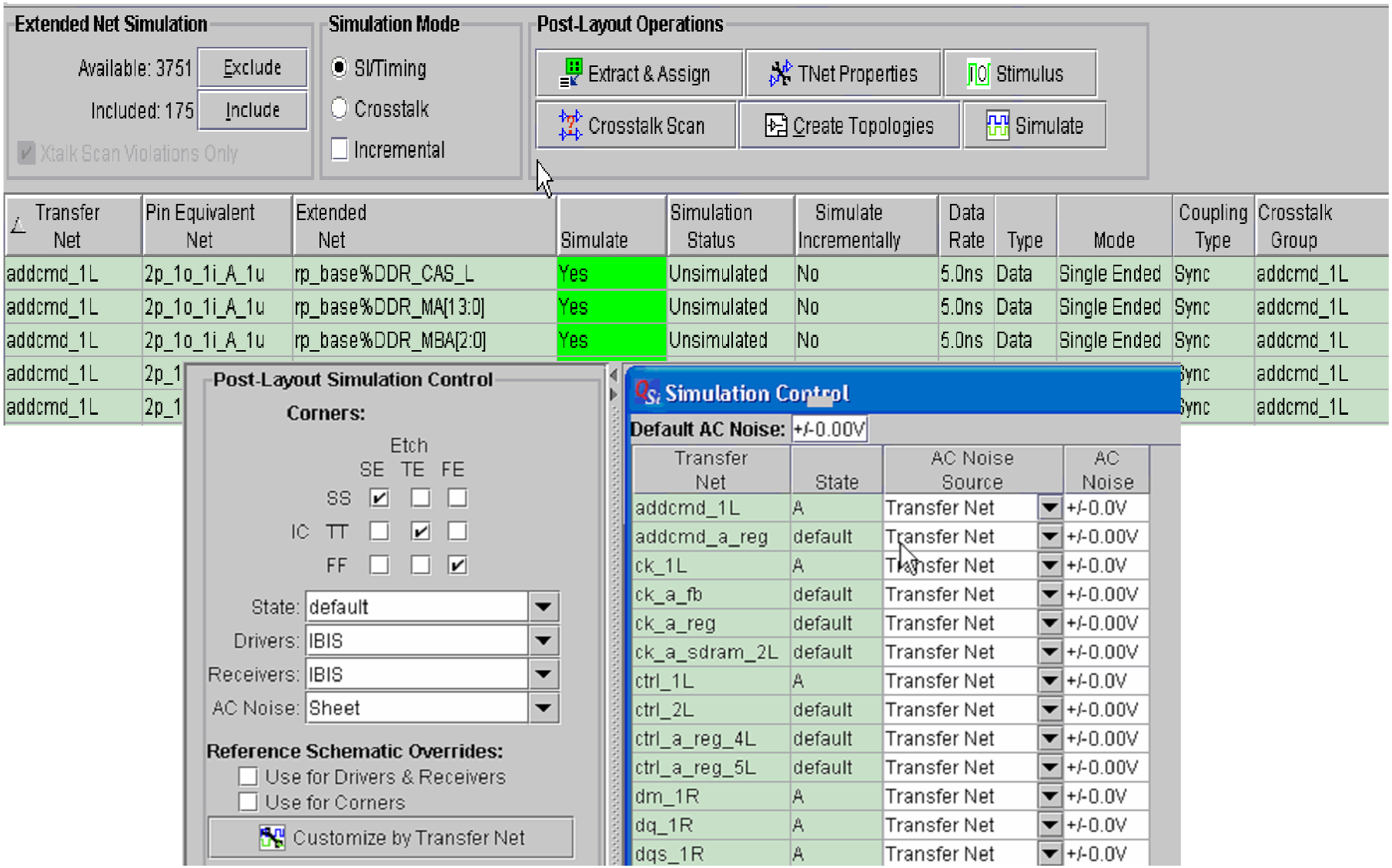
QSI for Post Route Simulations



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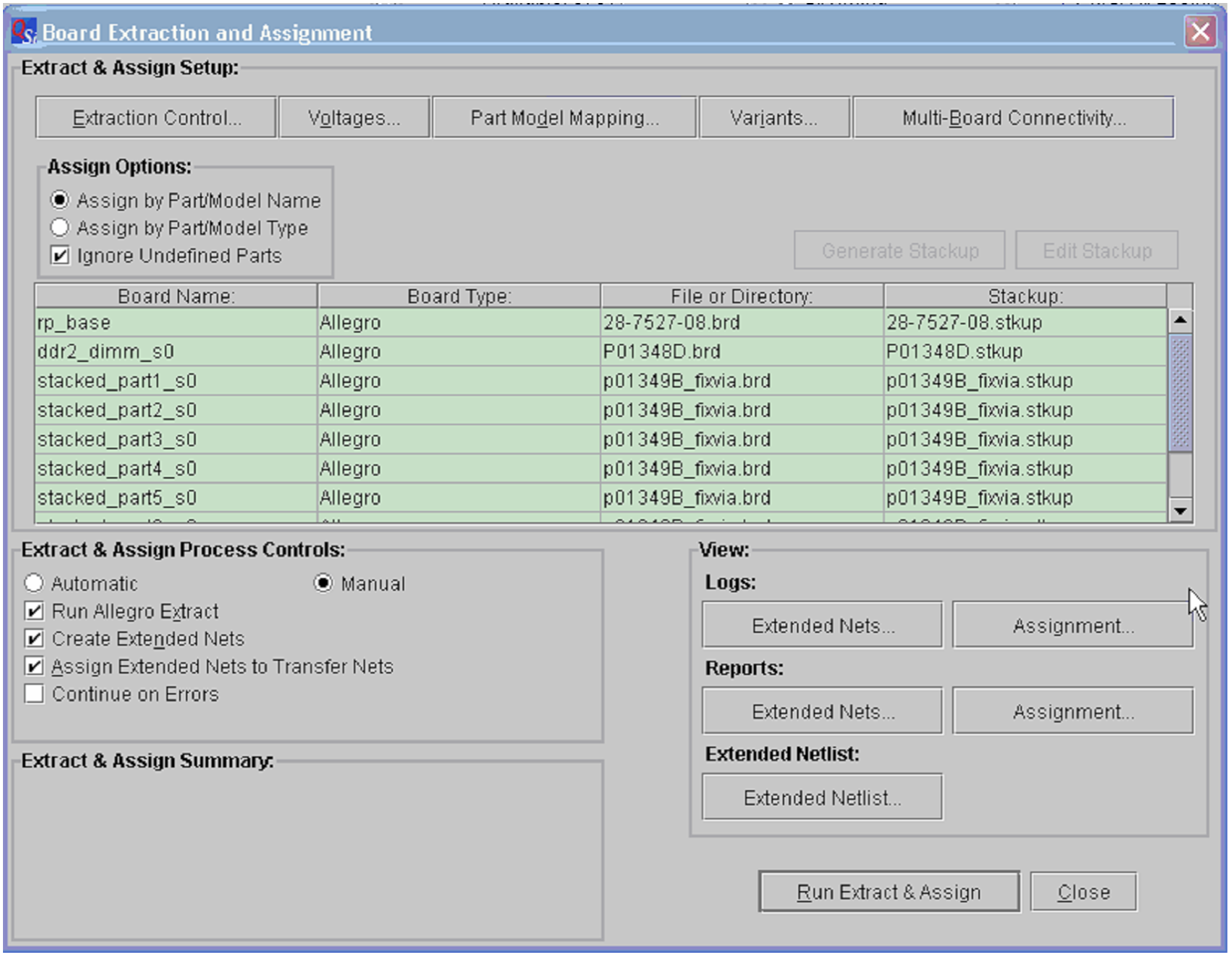
Multi Board Extractions with QSI



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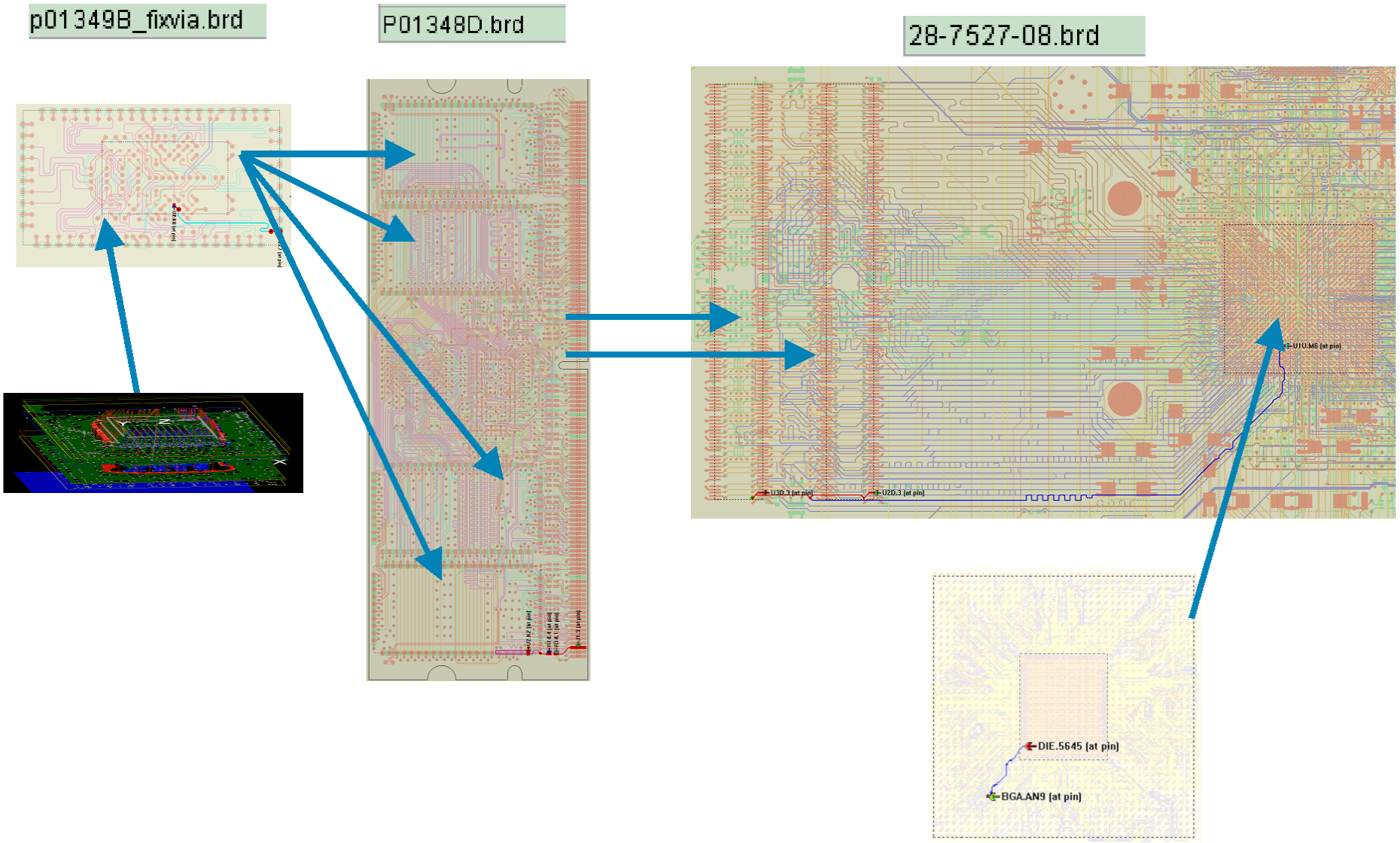
Multi Board Extractions with QSI



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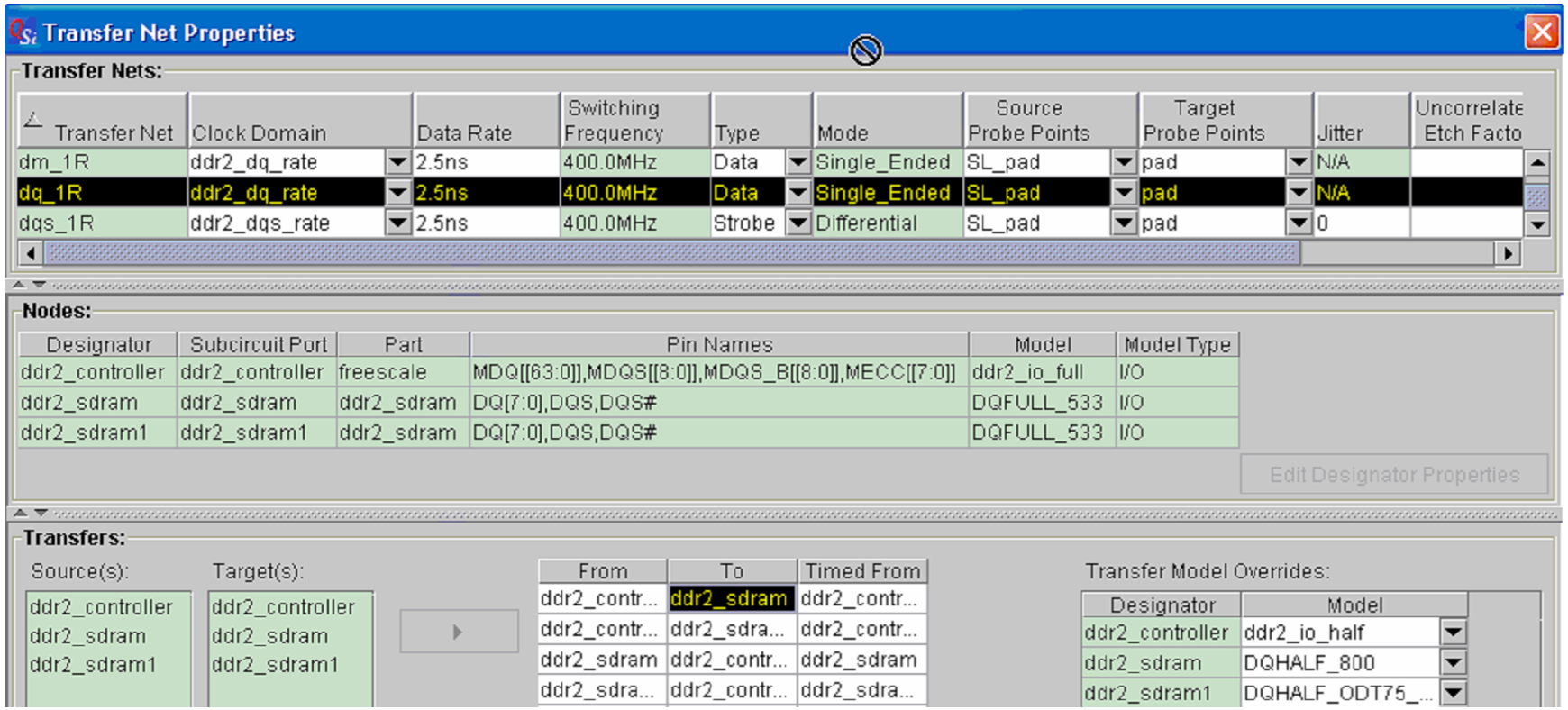
Transfer Nets in QSI



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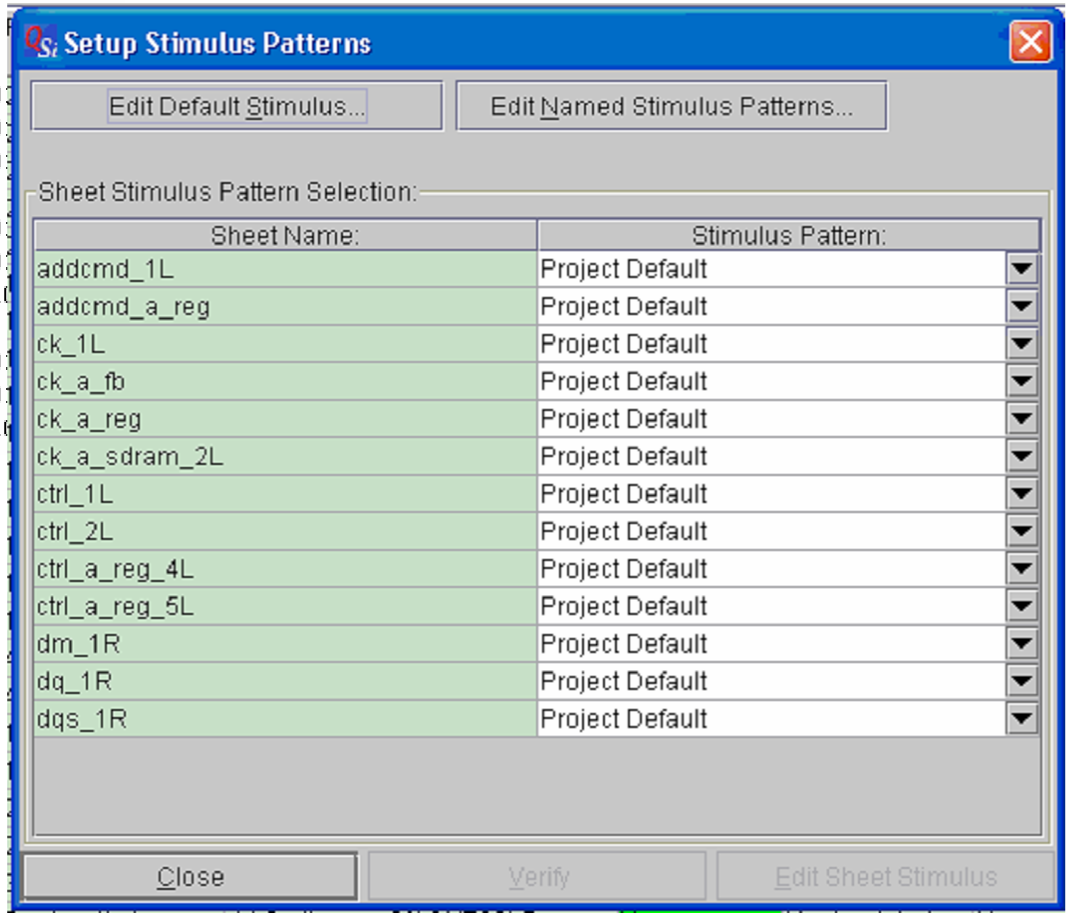
Stimulus Setup in QSI

```
rise_time              100pS                          T
character_time         100pS                          U

*data                   0110010101
* PRBS
data                   00000101100100011111010011
data_victim            01010101010101010101010101
data_aggressor         00000101100100011111010011

clock                  01010101010101010101010101
clock_victim           01010101010101010101010101
clock_aggressor        10101010101010101010101010

strobe                 01010101010101010101010101
strobe_victim          01010101010101010101010101
strobe_aggressor       10101010101010101010101010
```



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Waveform and Timing Report

	A	B	C	D	E	F	G
1	Setup Margin (ns)	Hold Margin (ns)	Rmin Etch Delay (ns)	Rmax Etch Delay (ns)	Fmin Etch Delay (ns)	Fmax Etch Delay (ns)	Transfer Net
2	No AC specs	No AC specs	1.072	1.373	1.072	1.373	PRE_PLL_CLK
3	No AC specs	No AC specs	0.403	0.617	0.403	0.613	PLL_SDRAM_CLK
4	No AC specs	No AC specs	0.358	0.627	0.36	0.632	pll_reg_clk
5	No AC specs	No AC specs	0.38	0.552	0.381	0.55	PLL_FDBK
6	0.037	0.784	1.331	1.71	1.331	1.71	DQS_ECC_2R_2Slot
7	0.153	0.585	1.206	1.616	1.205	1.614	DQS_2R_2Slot
8	0.828	1.01	1.037	1.511	1.072	1.412	Pre_reg_cmd_slot1
9	0.807	1.03	1.153	1.675	1.189	1.575	Pre_reg_cmd_slot2
10	0.375	1.127	1.154	1.907	1.195	1.748	Pre_reg_CS
11	0.617	1.006	1.033	1.865	1.067	1.744	Pre_reg_addcmd
12	0.344	0.232	1.132	1.795	1.143	1.741	DQ_2R_2Slot
13	0.395	0.305	1.293	1.662	1.294	1.603	DM_2R_2Slot
14	1.223	1.411	0.627	1.244	0.771	1.312	Post_reg_addcmd_LB
15	1.169	1.255	0.756	1.34	0.623	1.376	Post_reg_addcmd_RB
16	1.442	1.228	0.701	1.091	0.615	1.08	Post_Reg_CTRL_4L
17	0.875	1.356	0.819	1.592	0.733	1.656	Post_Reg_CTRL_5L
18							
19							
20							
21							
22							
23							
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26							
27							
28							
29							
30							
31							

Waveform Quality / Waveform Overshoot / Eye Rollups / Eye Details / Waveform Margin By Tnet / Waveform Margin By Variation / Model Overview / Timing Ana

Ready NUM

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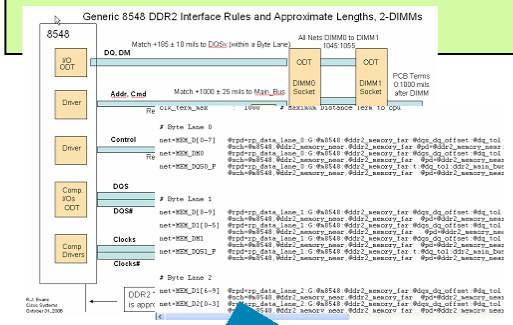
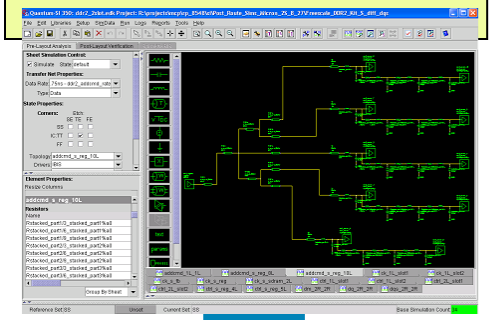
Design Kit Strategy for Reuse

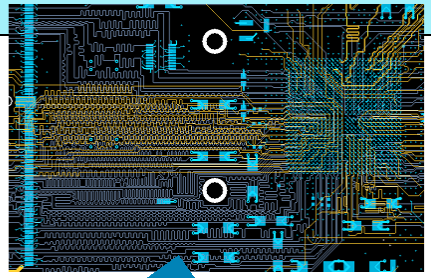
Design Constraints



SiSoft Interface Design Kit Pre- & Post-Route



ECAD Interface CAD Clip



HSD Web-based Repository

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Summary

- Definition of HSD
- Static Timing Analysis for DDR
- Pre-route simulations (Scan the design space)
- Routing Rules development for CAD
- Full post route simulations
- Summary

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References

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  "Bowling for Picoseconds Integrating DDR2/DDR3 Timing"
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  http://download.micron.com/pdf/datasheets/dram/ddr2/256MbDDR2.pdf
- JEDEC DDR2 Spec: JESD79-2C
  http://www.jedec.org/download/search/JESD79-2C.pdf
- Micron DDR2 Datasheet
  http://download.micron.com/pdf/datasheets/dram/ddr2/1GbDDR2.pdf
- SiSoft-Micron DDR2 Paper
  http://www.sisoft.com/papers.asp

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- Dear IEEE RTP EMC Chapter members:

  Our next meeting is on Tuesday, September 4, 2007 at Underwriter's Laboratory. 5:30 PM is the start time. Below is an abstract of the presentation and Steven Scearce's biography. If interested, please RSVP. Food will be served. Mark your calendar and hope to see you there.

  Presentation Abstract: PCB level SI tools and strategy

  I will discuss the current tools and strategy my team uses use for PCB level high speed design. We can follow the design flow from the pre route simulation/ rule development, to the full post route verification of the design. Specifically we will examine use of the SiSoft tool for control of the Spice simulations and timing of the design for a DDR2 implementation.

  Author Biography:

  Stephen Scearce is currently is working as the manager of the High Speed Design team at Cisco System Inc, and has worked in HSD team as a signal integrity engineer for 4 years at Cisco. Before joining the central HSD team, Stephen worked for the Cisco ATG as an EMC/Safety/NEBS designer. Prior to working at Cisco, Stephen worked for NASA LaRC as a research engineer in the Electromagnetics research branch HIRF team. His research interests include power integrity and signal integrity full channel design (Die to Die). Stephen has 3 US patents and 2 pending patents. He received his BS and MSEE from Old Dominion University, Norfolk VA.

  Sincerely,

  Eric R Schumann
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