Application of X2Y Capacitors in Power Delivery Networks

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Getting a Handle on PCB Power Delivery

- PCB Power delivery is dominated by:
  - Inductance
    - Limits useful frequency range of each PDN element
  - Resonance
    - Sets worst case noise

Getting a Handle on PCB Power Delivery

- Inductance
  - Limits performance of ***every*** PDN component
  - Compensated by capacitive component w/ ***less*** inductance
- Examples:
  - VRM ⇨ Bulk Caps
  - Bulk caps ⇨ Ceramic caps
  - Ceramic caps ⇨ Power cavity

Getting a Handle on PCB Power Delivery

- Resonance
  - Occurs wherever a large phase transition (>135°) occurs in the PDN transfer function
    - Typical: Inductive Z_{MAG} crosses capacitive Z_{MAG}
    - Magnitude depends on Z_{CHAR}, and Q- both increase w/ inductance
  - Modal occurs at locations and frequencies where reflections from the structure boundaries strongly reinforce

Getting a Handle On Bypass Networks

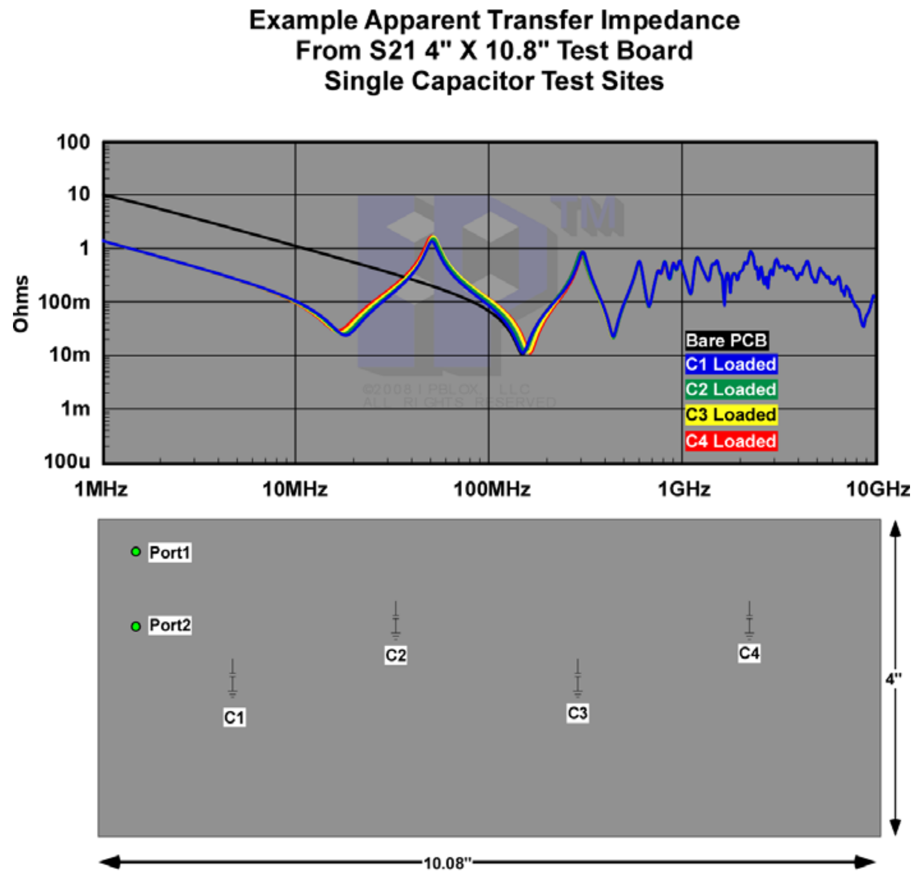
- Bypass networks are a source of much confusion:
- Confusion results primarily from misconceptions of spatial behavior of the planes

PDN Impedance

- At least two impedances:
  - Impedance seen by any particular load
  - Plane cavity spreading inductance limits between IC power via attach and bypass cap attach
- Distributed impedance presented to composite loads

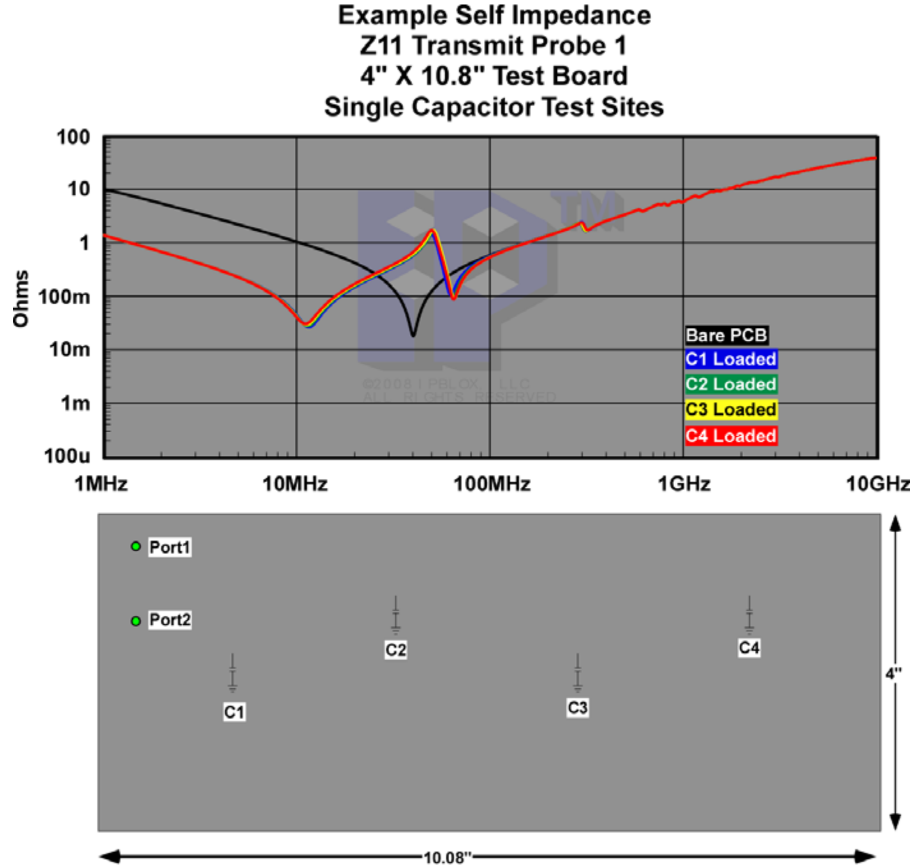
Plane Impedance from S21
One Cap at a Time

- Receive port S21 represents port to port insertion loss
  - Varies w/ position of ports
  - Distorted by series loss:
    - Plane L/R looks like lower shunt Z
- Cap position doesn't seem to matter
  - This is a fallacy



Plane Impedance from Z11?

- Single Port
  - Plane spreading inductance dominates
- Probing awkward
  - Can be derived from S21 w/ probes on either side of PCB
- Tells the truth (sort of)
  - About attachment the size of the probe ports only
- Spreading inductance varies little from small probe radius to distant caps



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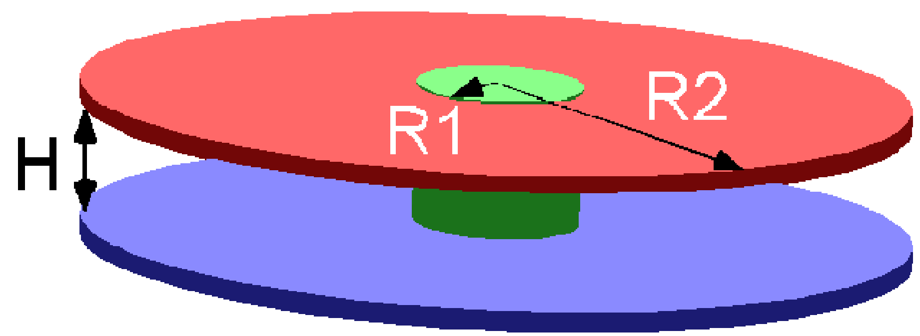
Power Plane Paradoxes

- Power cavities are low inductance capacitors:
  - Parallel plates, inductance set by cavity height and aspect ratio between ports
  - Resonate w/ discrete caps
    - $F_{RES} \approx 1/(2\pi(ESL_{BYPASS} * C_{CAVITY})^{0.5})$
- Power cavity spreading inductance limits HF performance
  - Power cavity spreading inductance isolates bypass caps from IC power connections
  - Spreading inductance increases logarithmically w/ radius

Plane Inductive Behavior

- Incremental impedance from any point decreases linearly with: circumference, radius, time
- Conversely impedance increases linearly w/ frequency, IE inductive transfer function
  - Hence planes appear inductive @ HF



Inductance = 5.08nH * H(inches) * ln(R2/R1)
0.20nH * H(mm) * ln(R2/R1)

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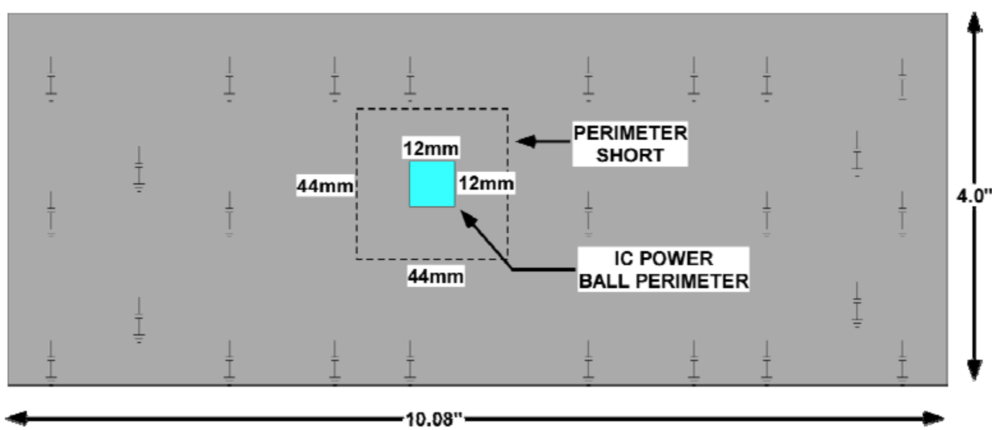
IC Point of View

- IC's typically have multiple power pins spread over some area of PCB
- Much lower spreading L than colinear VNA ports
- Significant sensitivity to capacitor proximity
- Evaluate interconnect w/ perimeter short model

EXAMPLE 10" x 4" PCB, ONE IC
SCATTERED BYPASS CAPS



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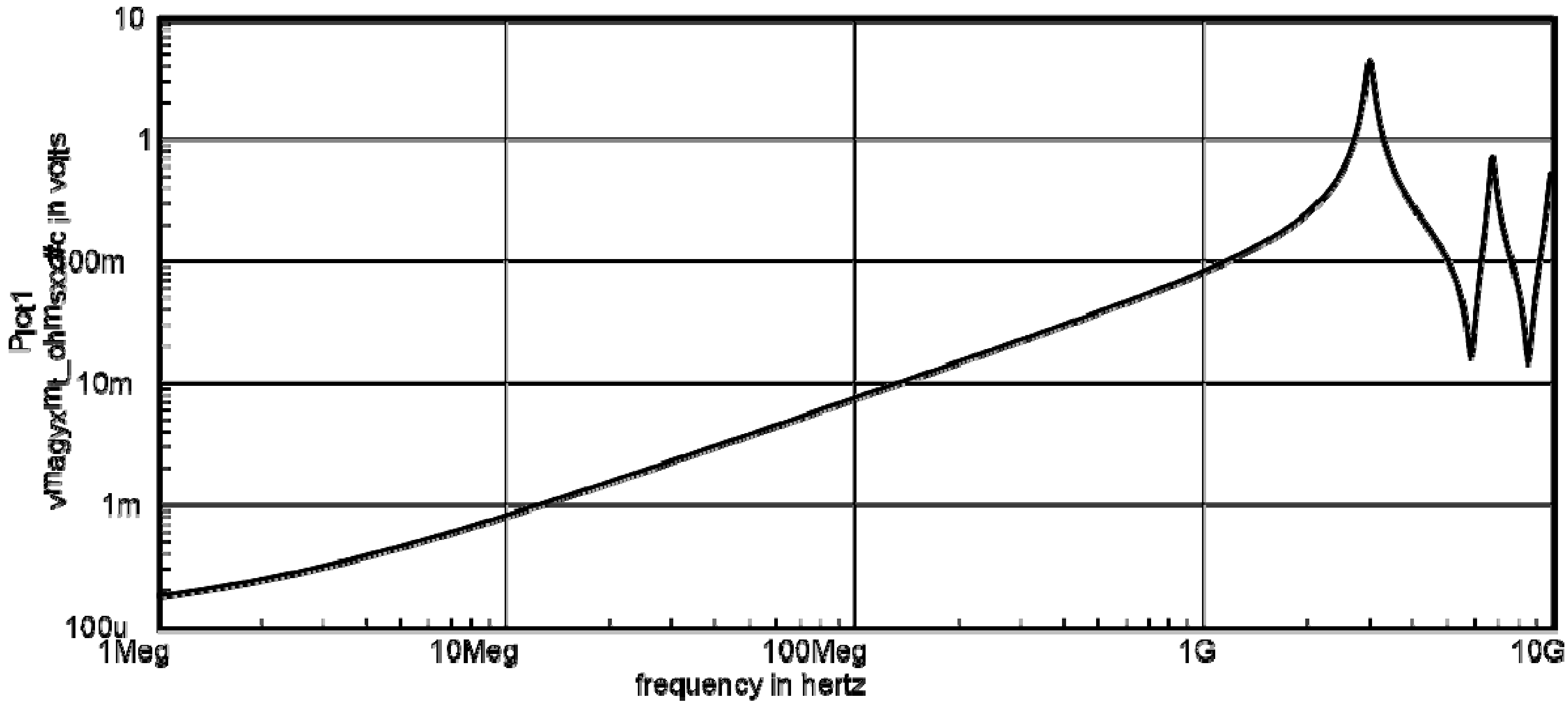
Shorted Perimeter Around IC

- Response **very** different than single VNA port



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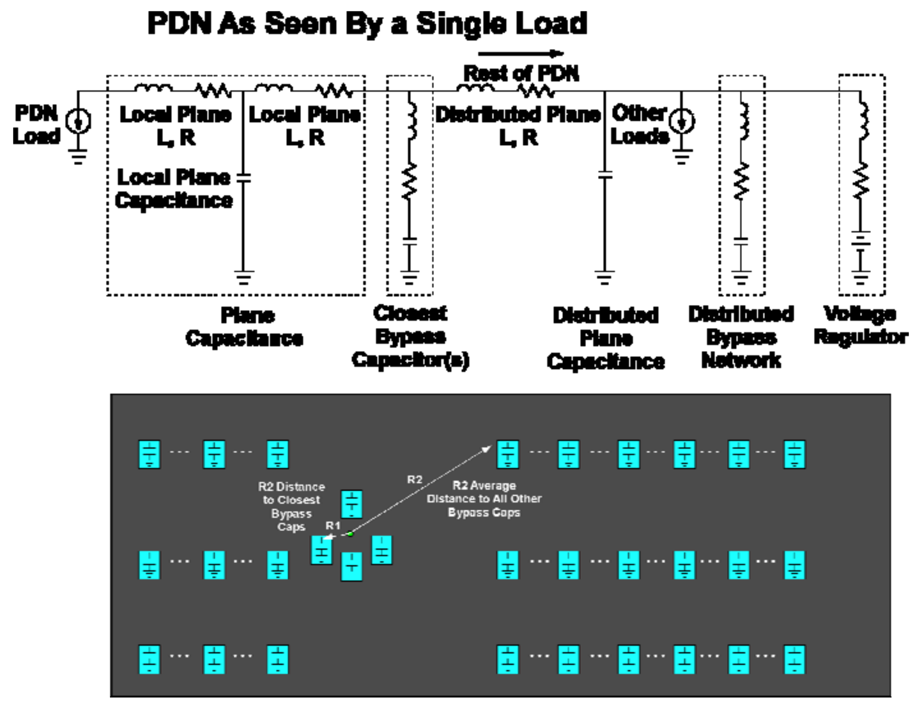
Simplified PDN Model, Single Load

- To a single load, plane L/R fundamentally limits Z_{MIN}
- Current divides between closest bypass caps and rest of PDN through planes
- Closest caps are most important
  - Other caps appear through plane spreading inductance / delay
  - Spreading inductance beyond closest caps ***usually*** small
    - Depends on dielectric thickness
  - Other loads filter through spreading inductance and local caps



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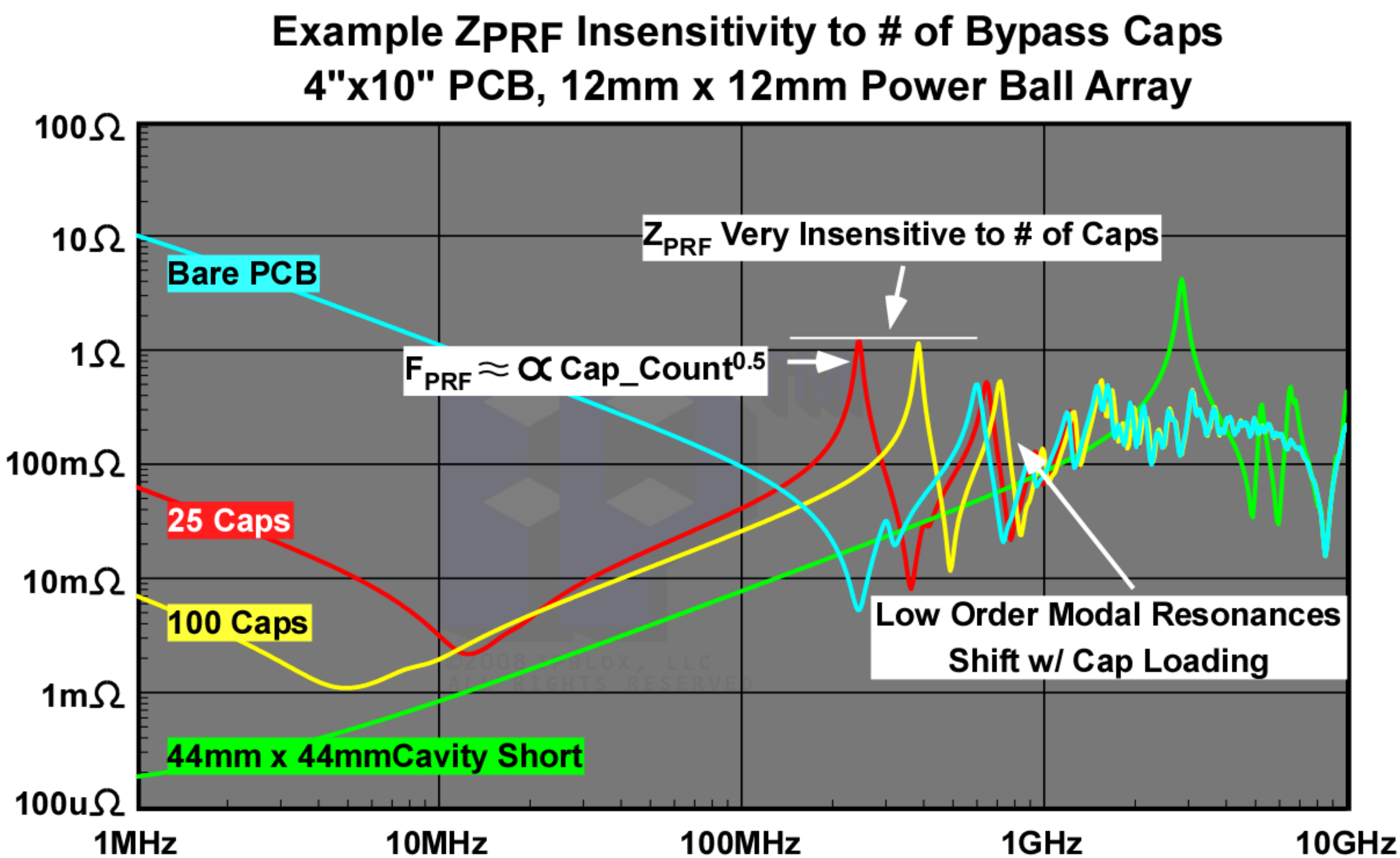
Bypass / Cavity PRF



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Key Bypass Issues

- Position of bypass capacitors relative to loads does matter
- The distributed inductance of the ***bypass network*** w/the plane cavity set F_{PRF}
- The inductance and ESR of ***Each*** bypass cap largely sets the Z_{PRF} ***Independent*** of F_{PRF}

Distributed Inductance and F_{PRF}

- Parallel resonance occurs where:

  $jwL_{BYPASS\_NETWORK} = 1/jwC_{POWER\_CAVITY}$
  - Move resonance by manipulating the bypass network inductance
  - The number of caps needed is:

    $N_{CAPS} = ESL_{MOUNTED\_CAP} / L_{BYPASS\_TARGET}$
- F_{PRF} is relatively insensitive to capacitor positions for any practical design
  - Assumes capacitors distributed
- F_{PRF} only moves as square root of capacitor count
- Loading a PCB w/ bypass caps shifts the lower modal resonances

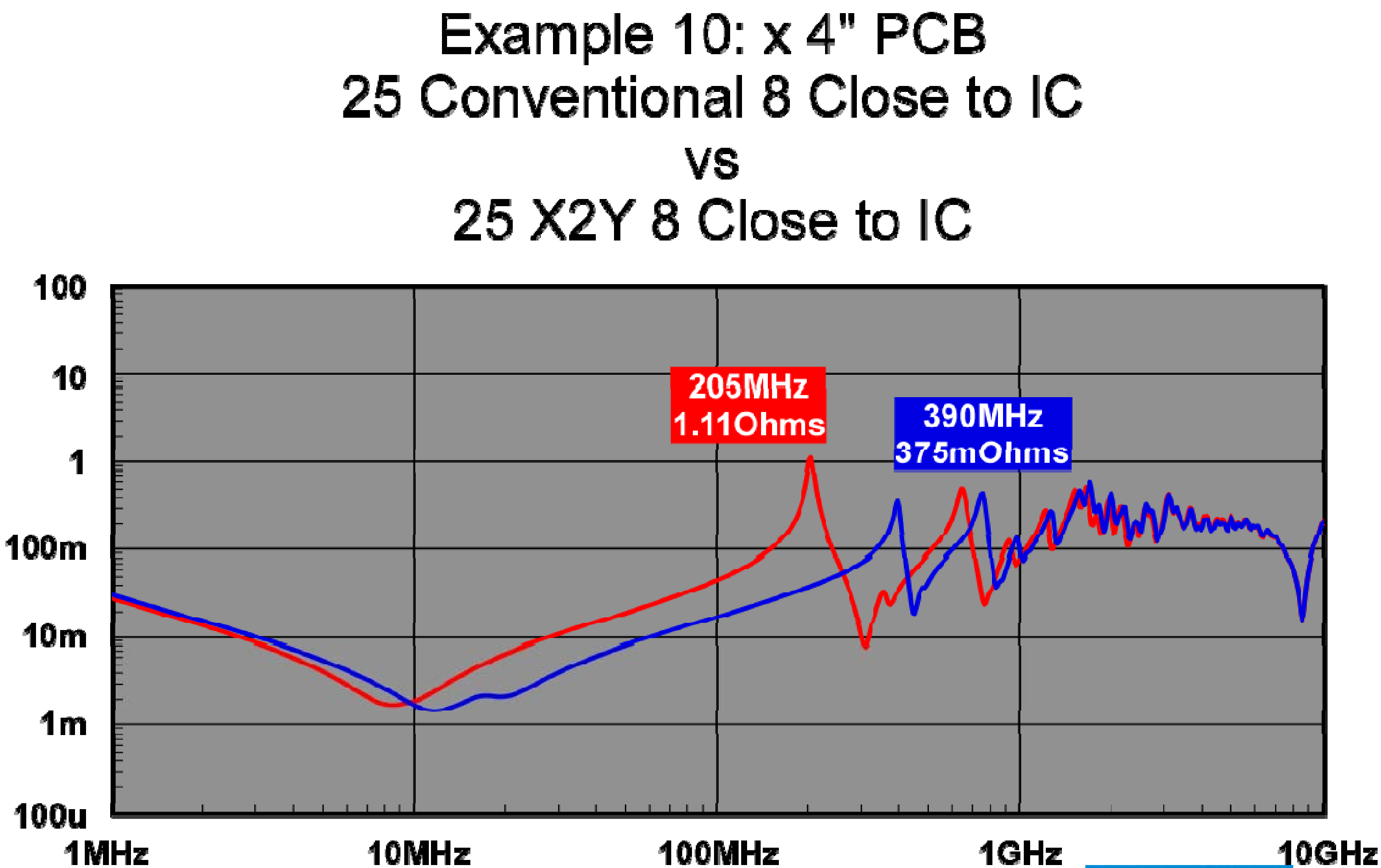
Z_{PRF}

- First order approximation of undamped PDN peak impedance, Z_{PRF}:
  - Is independent of the number of capacitors: N
    - In practice drops slowly as N drives F_{PRF} up due to cavity skin, dielectric losses & capacitor ESR changes
  - Is proportional to $ESL_{MOUNTED\_CAP}/ESR_{CAP}$
    - Lower mounted inductance / better caps improve
    - Damping can greatly improve
    - Combination of lower Q caps and damping very effective

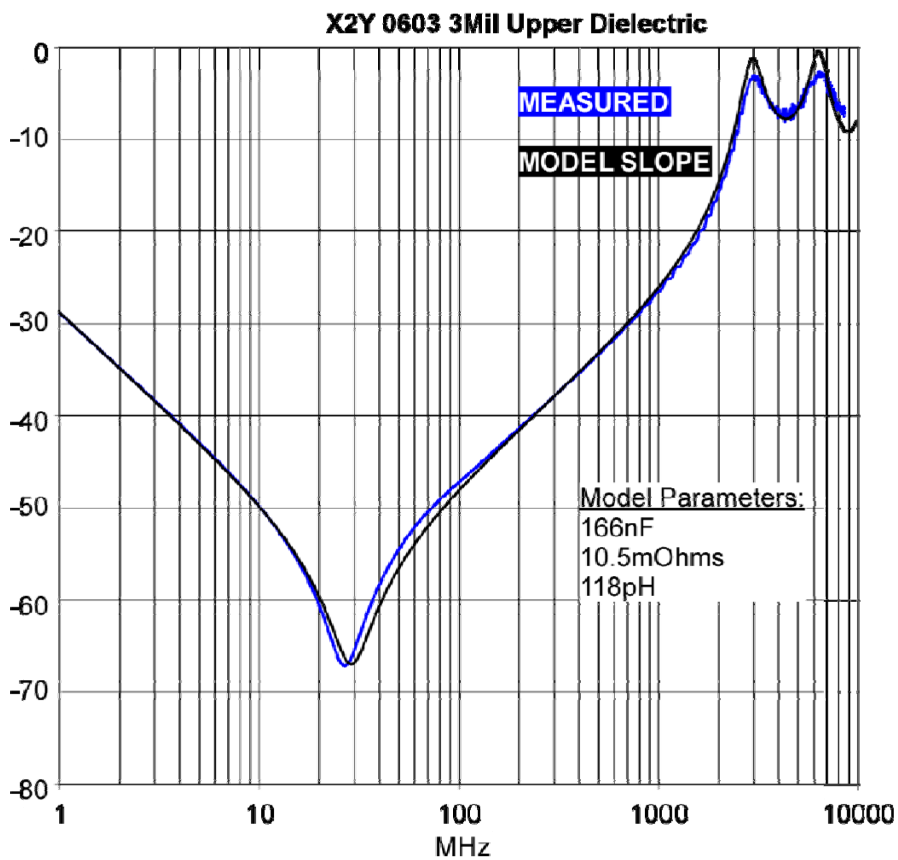
Z_{PRF} Insensitivity to # Caps

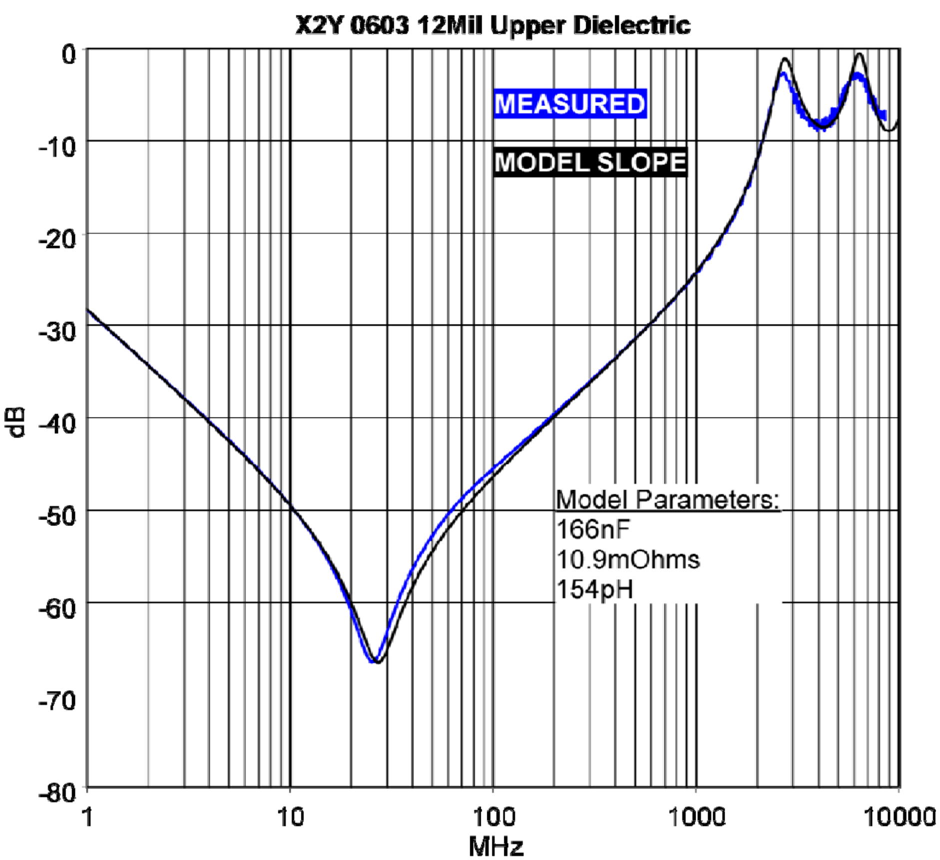
- For high Q networks:
  - $Z_{PRF} \approx Z_{CHAR} * Q$
    - $Z_{CHAR} = L_{NETWORK}^{0.5} * C_{CAVITY}^{-0.5}$
    - $Q = jw_{PRF} L_{NETWORK} / R_{NETWORK}$
      - $jw_{PRF} \approx 1/(2\pi * (L_{NETWORK} * C_{CAVITY})^{0.5})$
    - $Q = L_{NETWORK}^{0.5} * C_{CAVITY}^{-0.5} / R_{NETWORK}$
  - $Z_{PRF} = L_{NETWORK} / (C_{CAVITY} * R_{NETWORK})$
    - $L_{NETWORK} = ESL_{MOUNTED\_CAP} / N$
    - $R_{NETWORK} = ESR_{CAP} / N$
  - $Z_{PRF} = ESL_{MOUNTED\_CAP} / (C_{CAVITY} * ESR_{CAP})$

Move F_{PRF}, Reduce Z_{PRF} w/ Lower Q Caps



X2Y® Low MOUNTED L Caps





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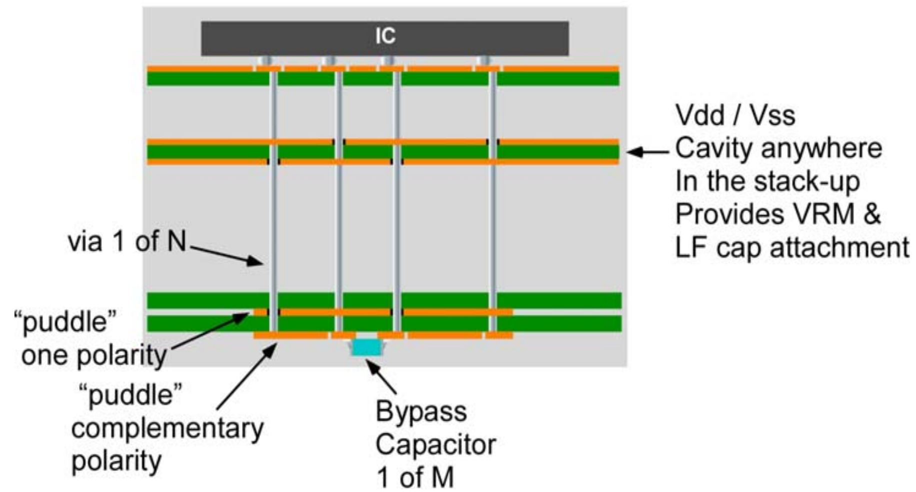
Puddle Concept

- Shares bypass capacitors and vias
  - When used for backside caps improves cap utilization and reduces Q
- Backside caps attach-
  - To an etch puddle as shown, OR
  - An etch ring
    - Puddle avoids spreading L
- Locate bypass caps on surface closest to puddle/ring
- Vdd DC distribution on internal layers

“Puddle” Concept Back-side Bypass Capacitors



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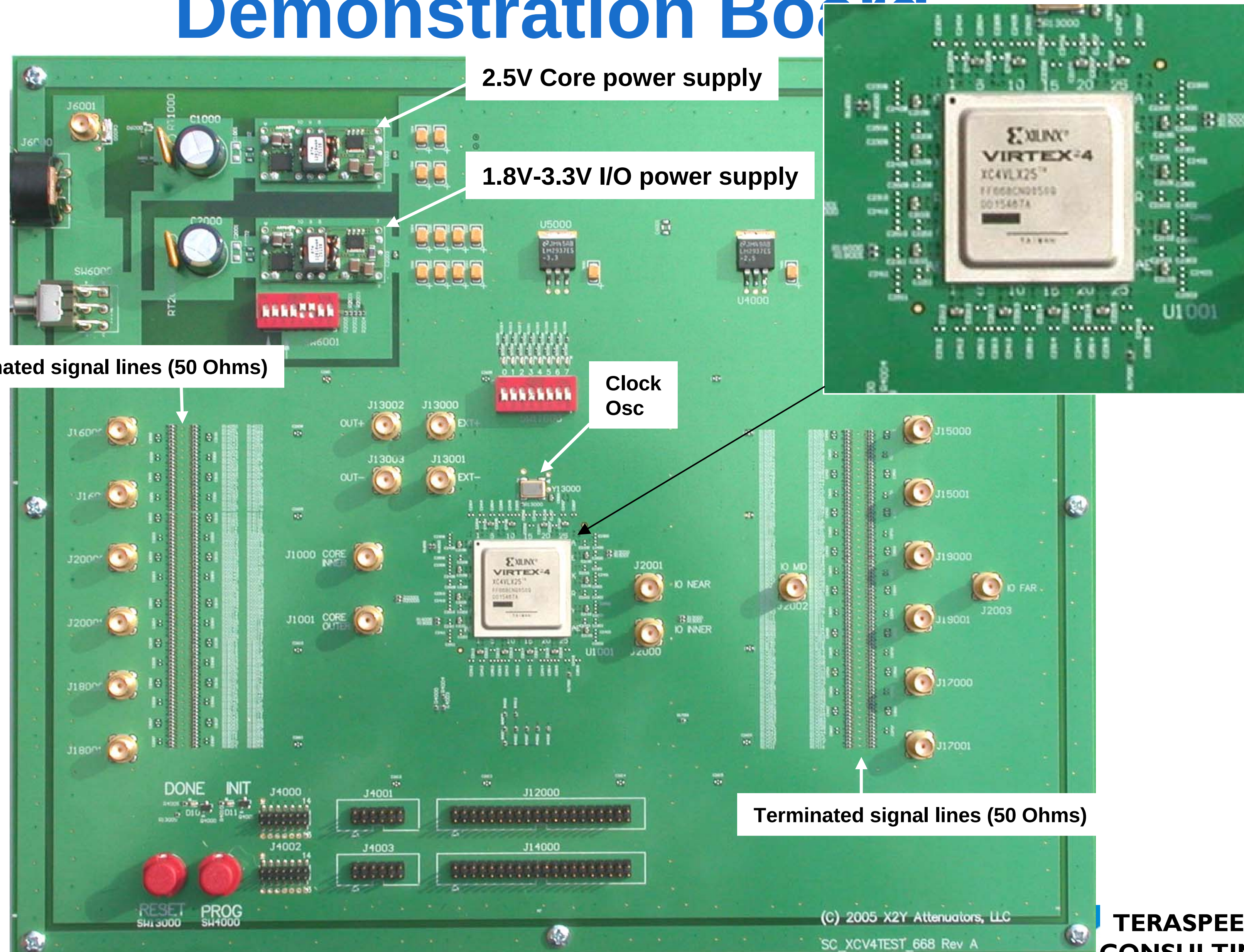
Demonstration Board



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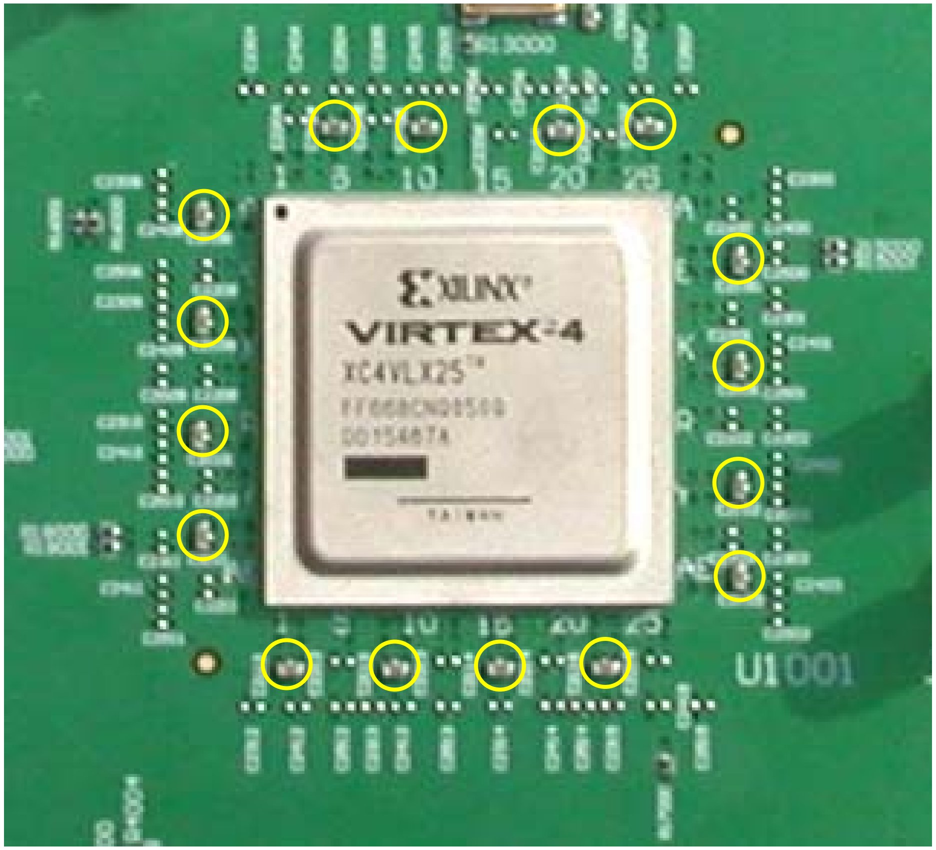
FPGA Bypass Design

- Two bypass capacitor options:
  - 16 X2Y 0603 100nF capacitors (shown circled)
  - Up to 64 conventional 0402 capacitors (unpopulated positions at right)
  - 16 of the 64 conventional on same radius as X2Y capacitors



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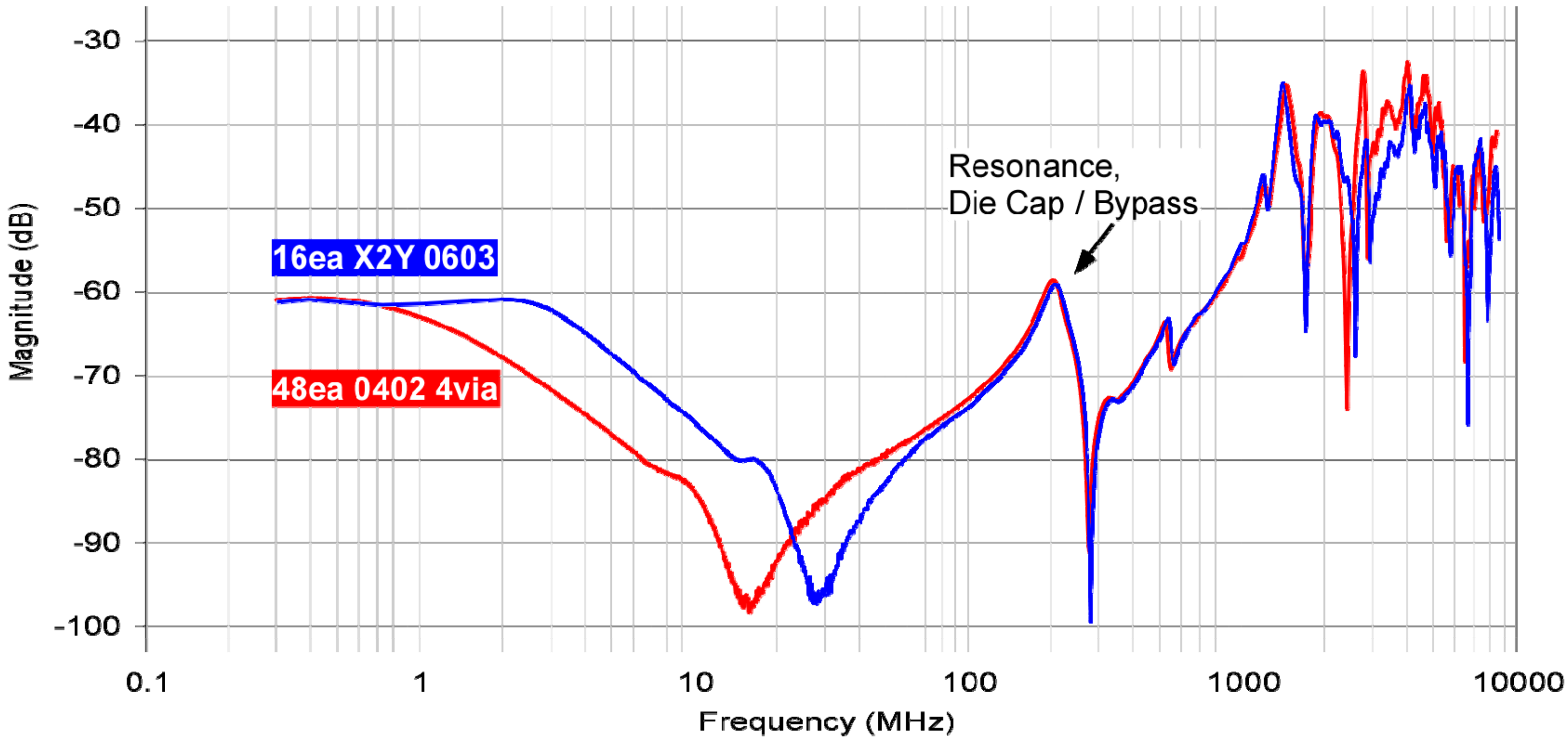
Test PCB VNA Measurments

- 16 X2Y® using 96 vias total same inductive response as 48 0402s using 192 vias total



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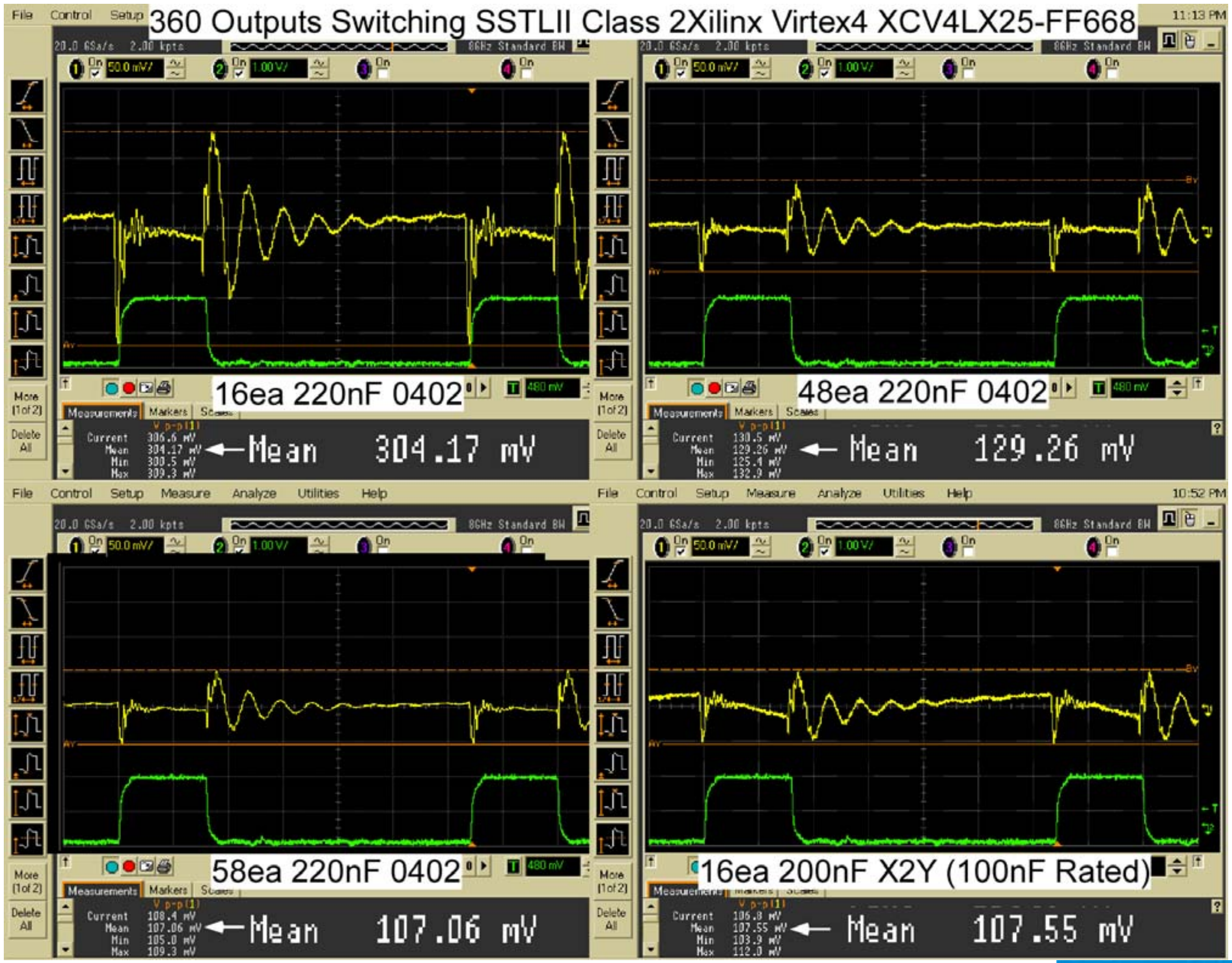
Test Board Noise Measurements



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Example Altera StratixII GX Eval Bd

- PCB Demonstrates SerDes Performance of Altera StratixII GX FPGAs
- Comparison of original conventional MLCC based bypass and X2Y® based bypass

Transmit Analog: VCCH

- Original Design
  - 2 x 330uF tantalum caps + 20 MLCCs
  - 1D < 80mOhms equivalent resistive to 250MHz
    - Ignores spatial effects and IC parasitics
    - Spatial effects dominate above 10MHz
  - Most caps on back
    - Typical as caps congest precious PCB component side
    - Aggravates # of caps needed
    - Raises Q of bypass network to plane resonance

Transmit Analog: VCCH

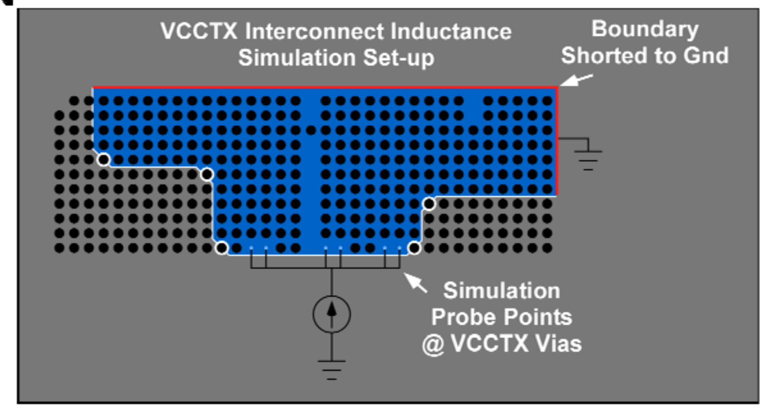
- X2Y® Design
  - Preserve 1D performance of orig.
  - 2 x 330uF tantalum caps + 2 MLCCs + 7 X2Y®
  - 1/3 caps & much lower inductance:
    - Capacitor + mount L much smaller w/ X2Y for like mounts
    - X2Y's mounted on top surface closer to planes
      - X2Y caps fit on top because so few needed
  - Smaller plane area used
    - More realistic to actual designs
    - Raises F_{PRF}
    - Also rasise Z_{PRF}

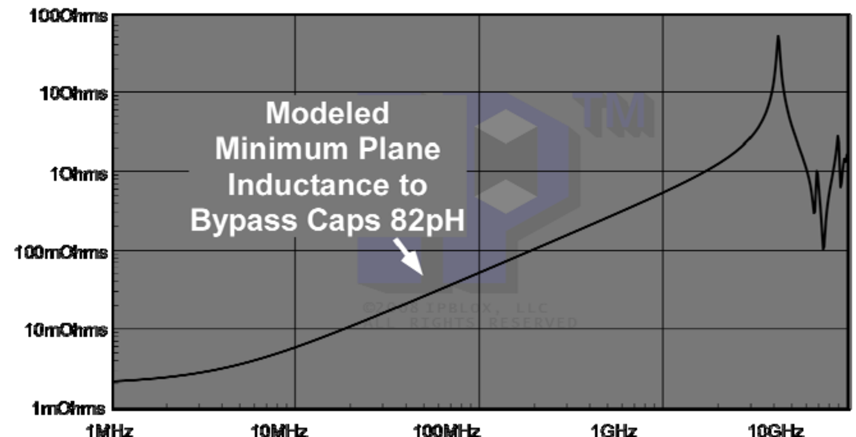
Determining PDN Interconnect Limits

- No amount of bypass capacitors can overcome the intrinsic impedance of the interconnects between the nearest bypass and the power pins
- Shorted boundary model identifies those limits

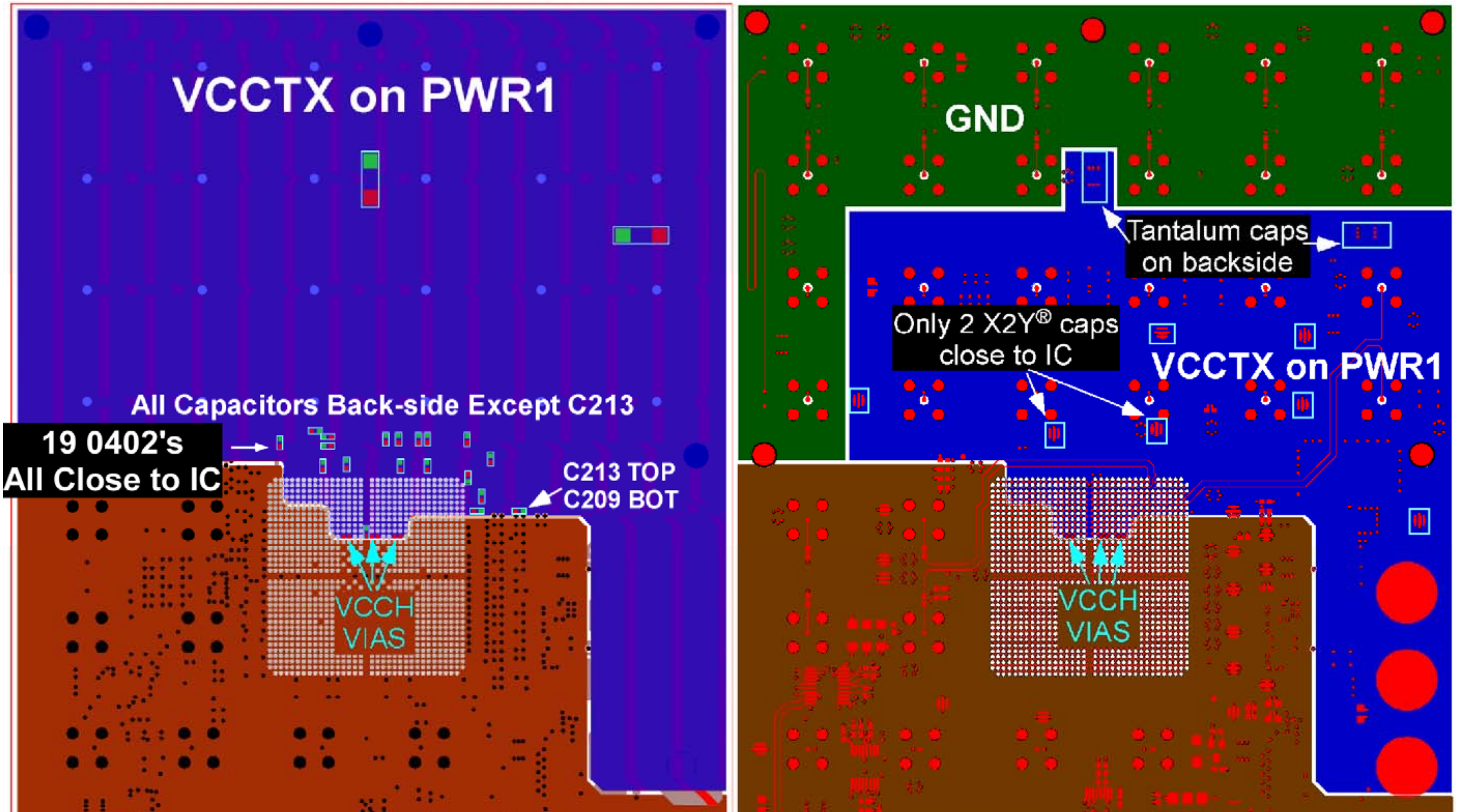
VCCTX Interconnect

Z_{MIN} Simulation Fixturing / Results



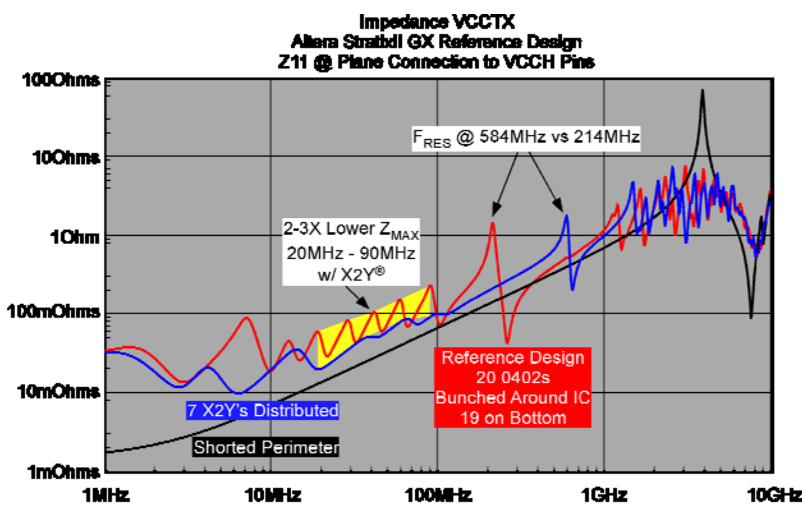


Example Design StratixII GX



StratixII GX VCCH Supply Simulation No IC

- Radically lower mounted L / cap w/ X2Y® top-side solution flattens impedance modulation.
  - Remains much closer to limit of shorted planes
- Higher F_{RES} w/lower Q stabilizes power system much faster after each transient.



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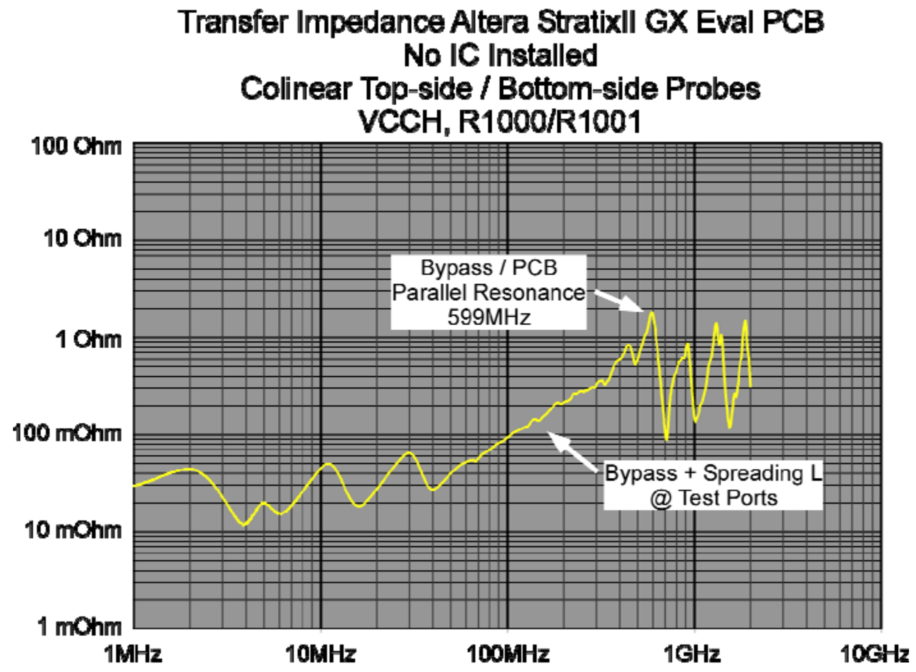
Measured X2Y® Network

- Bypass network measured through PCB @ 2 0805 one top-side / one bottom side, straight through vias
- Measured bypass to plane PRF closely matches simulation
- Detune resonance by changing one cap (next slide)



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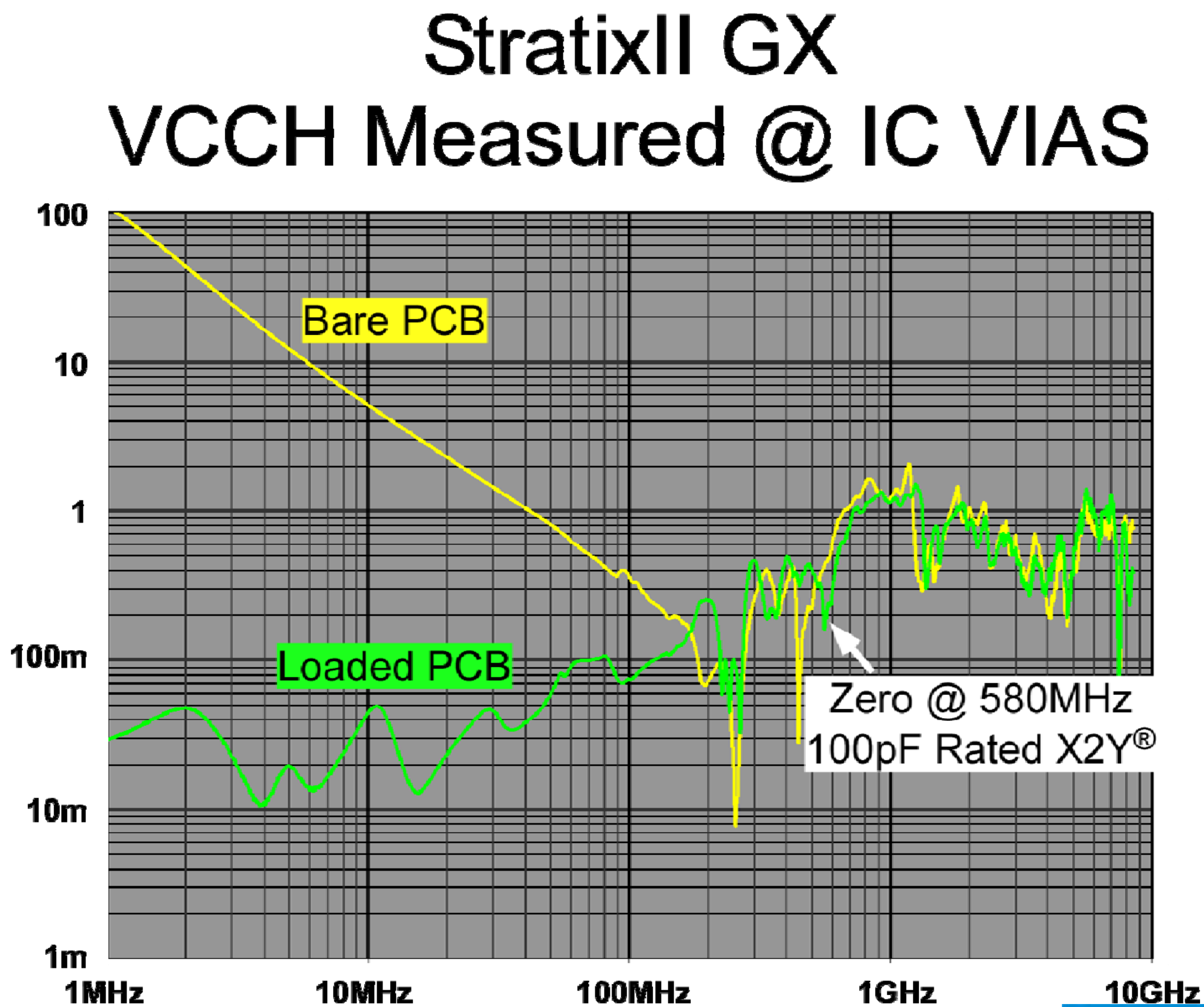
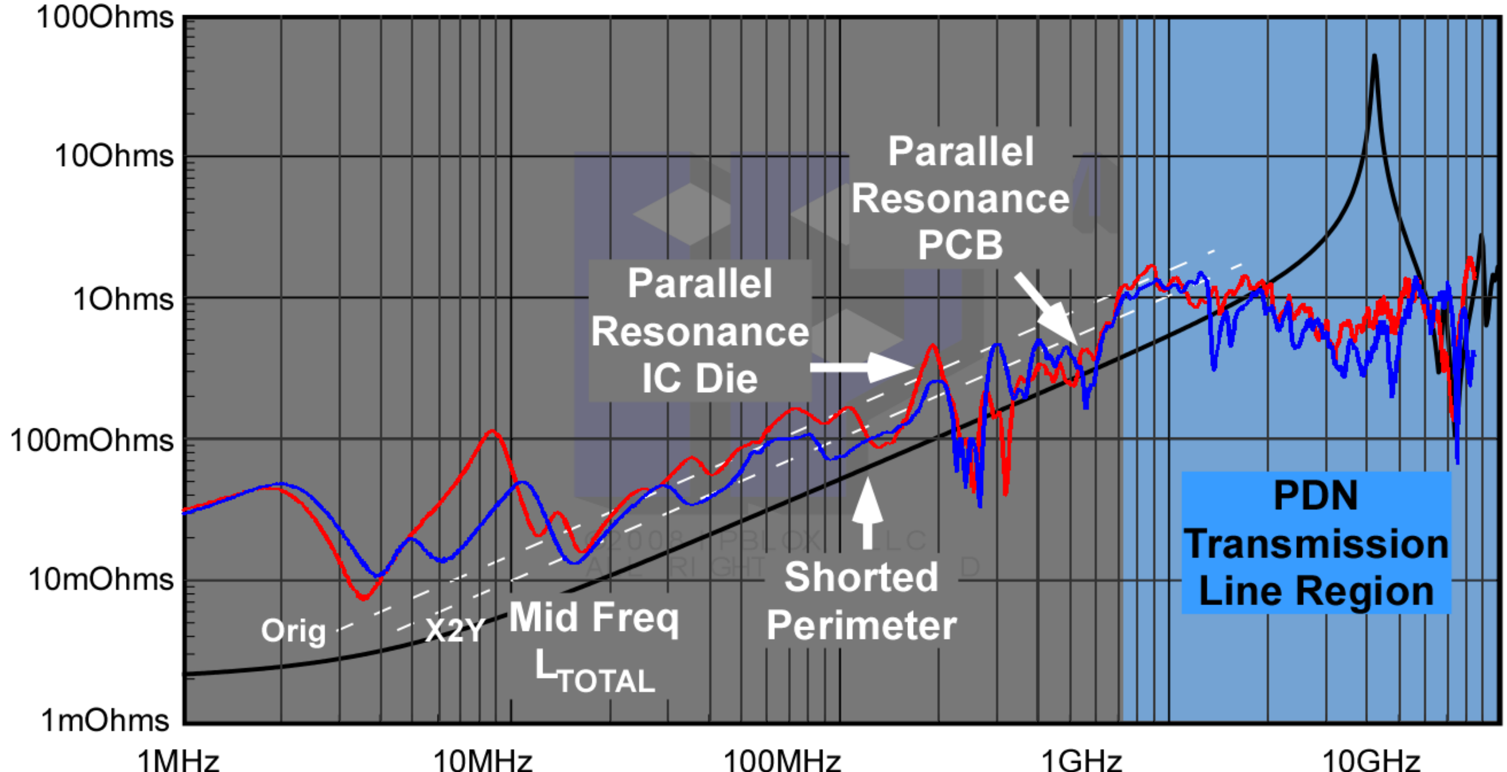
PCB w/ PRF Compensated



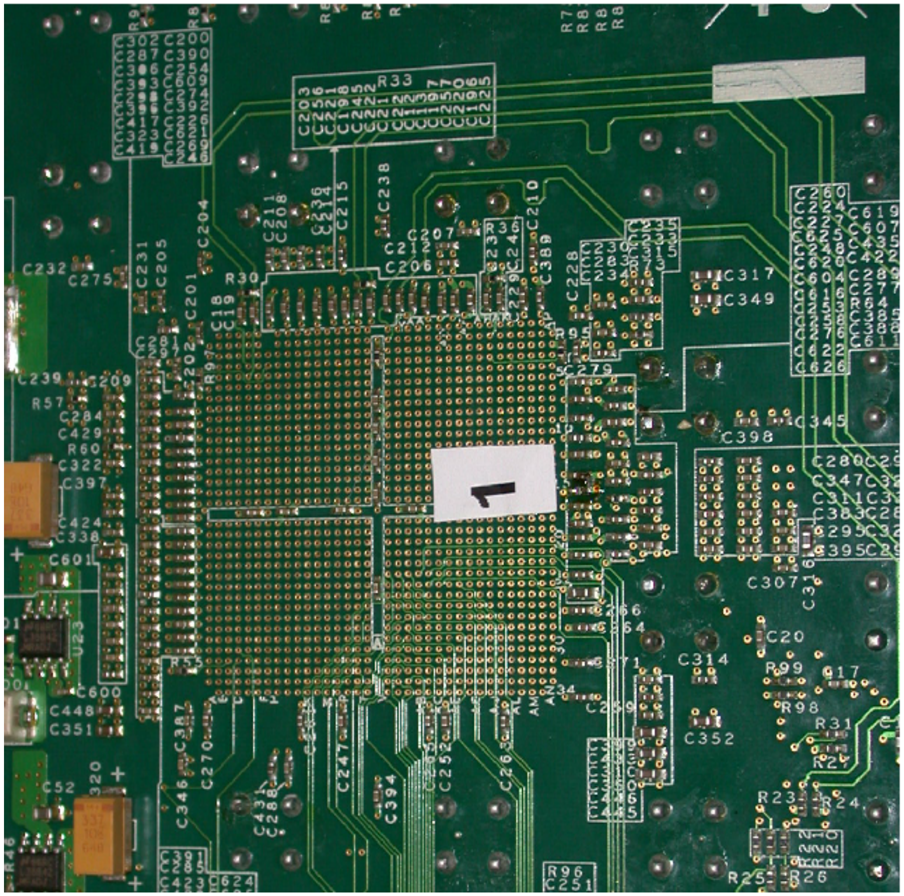
Example StratixII GX

Measured VCCTX Networks vs Simulated Shorted Perimeter

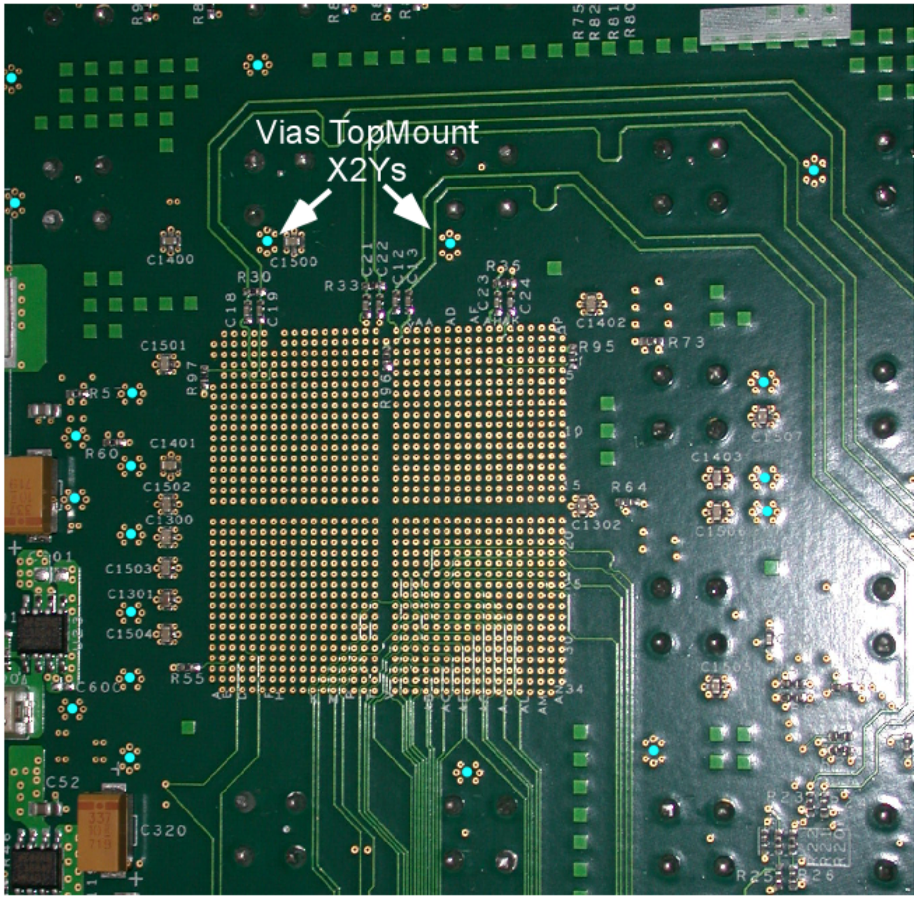


Example Design StratixII GX

Original Design



X2Y® Design



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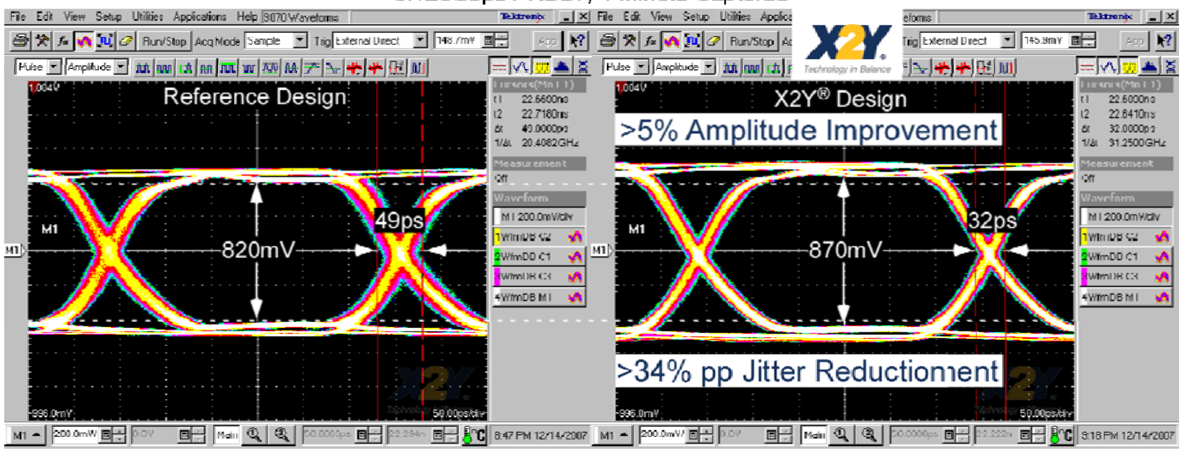
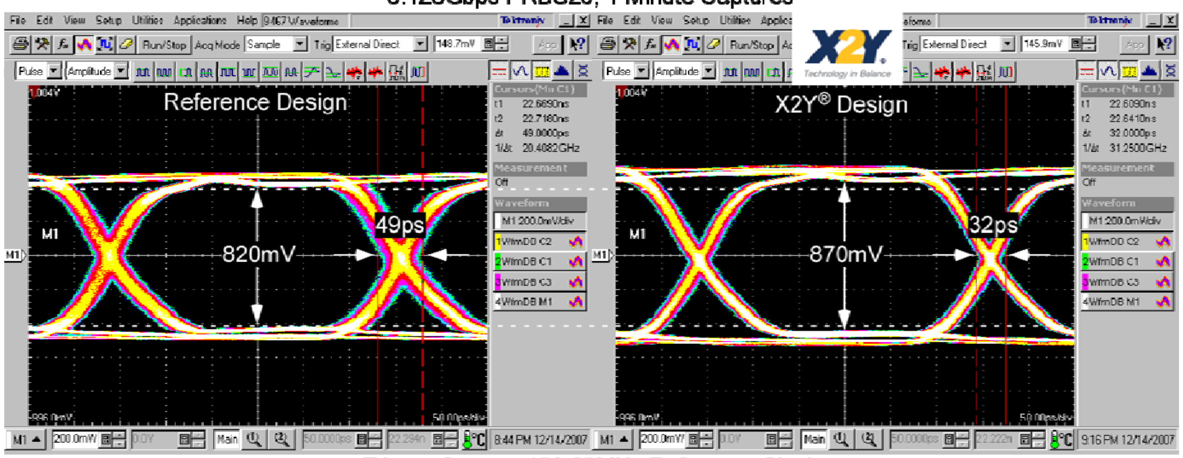
Measured Performance

3.125Gbps PRBS7, 1 Minute Captures



Trigger Source: 156.25MHz Reference Clock

3.125Gbps PRBS23, 1 Minute Captures



Trigger Source: 156.25MHz Reference Clock

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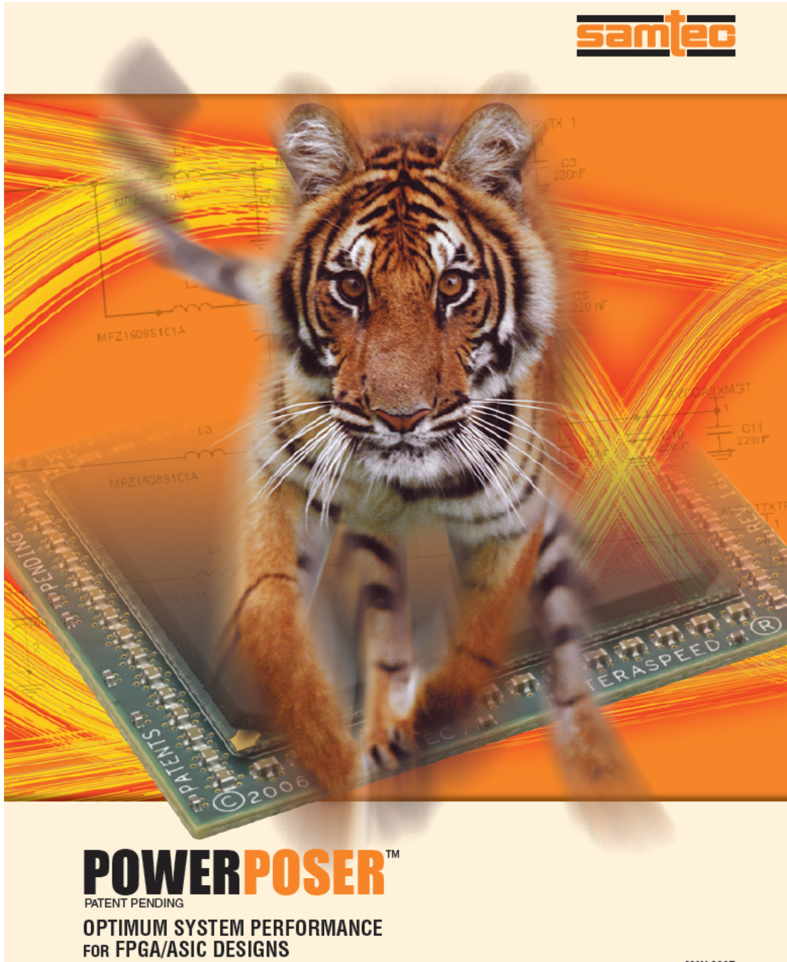
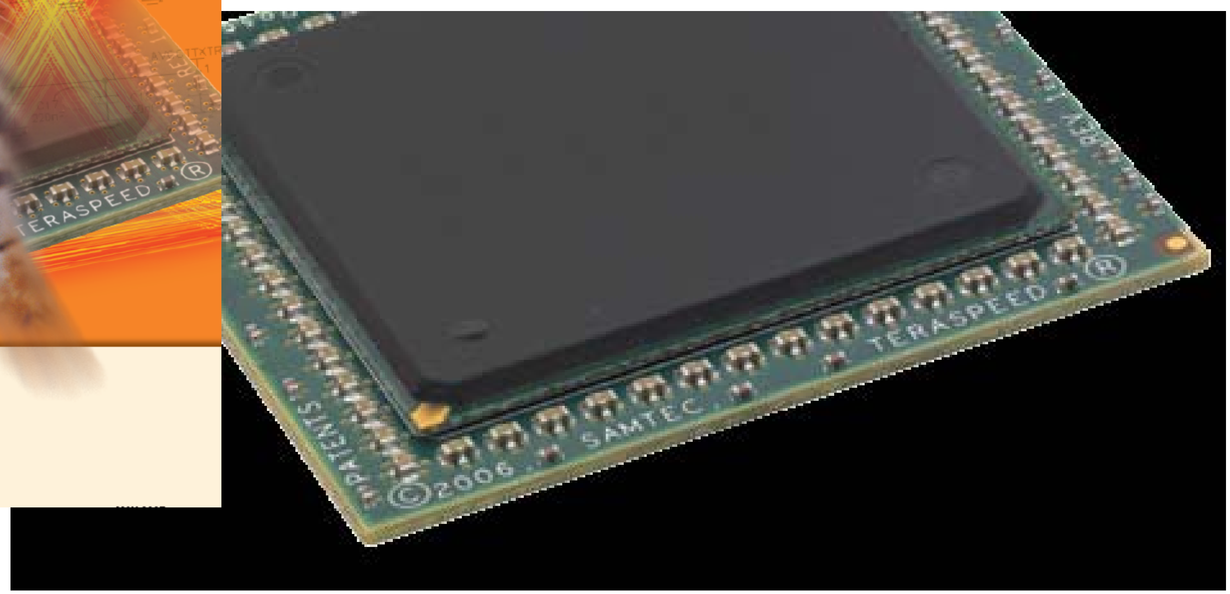
PowerPoser™





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Conclusions

- Understanding spatial behavior of PDNs is critical to proper analysis and design
- Inductance and resonance are the main problems to overcome
- Capacitor mounted inductance determines the number of capacitors needed to meet basic HF impedance requirements
- Detuning resonance provides substantial performance gains, lower L more feasible
- X2Y® capacitors excel at low mounted inductance

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