Fundamentals of Signal and Power Integrity

Christian Schuster

Distinguished Lecturer for the IEEE EMC Society 2012-13

Institute of Electromagnetic Theory
Hamburg University of Technology (TUHH)

Acknowledgements

Renato Rimolo-Donadio, Xiaomin Duan, Sebastian Müller, Miroslav Kotzev, Heinz-Dietrich Brüns

Young Kwark, Xiaoxiong Gu, Mark Ritter, Bruce Archambeault, Dale Becker, Thomas-Michael Winkel, Hubert Harrer

… and many others!

Abstract

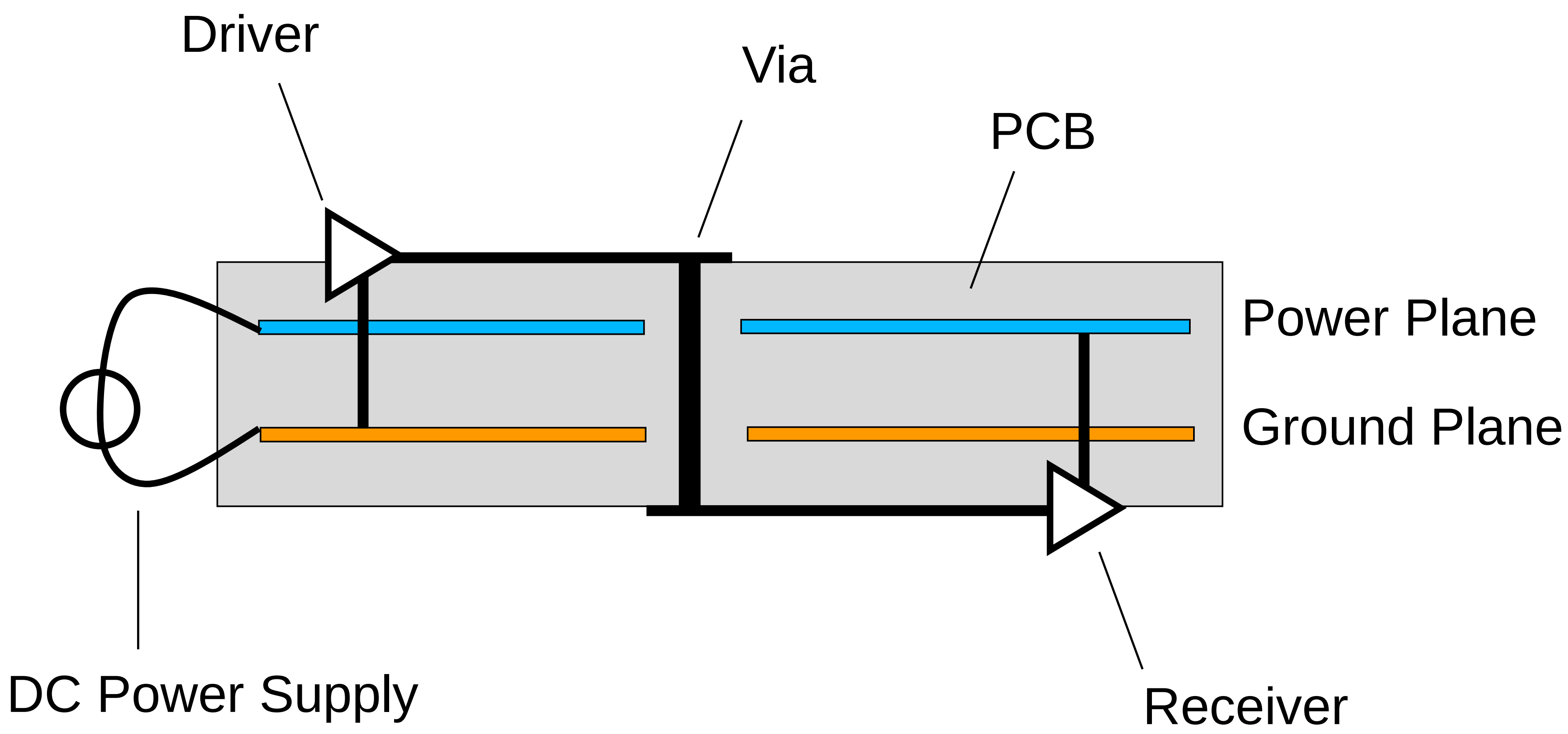
This presentation will give an introduction to the fundamentals of signal and power integrity engineering for high-speed digital systems with a focus on packaging aspects. The presentation is intended for an audience that has little or no formal training in electromagnetic theory and microwave engineering.

Topics that will be addressed include lumped discontinuities, transmission line effects, crosstalk, bypassing and decoupling, via and power plane effects, return current issues, and measurement techniques for Gbps links.

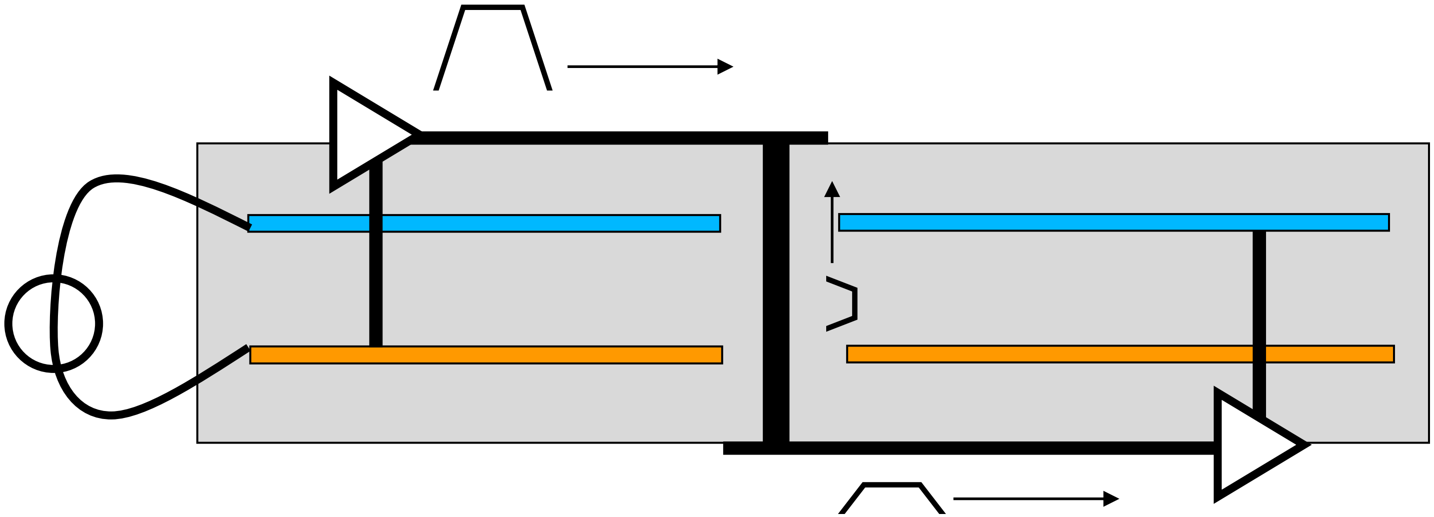
More information on current research projects at the Institute of Electromagnetic Theory can be found at:

http://www.tet.tu-harburg.de/

A Bird‘s Eye View on SI, PI & EMC



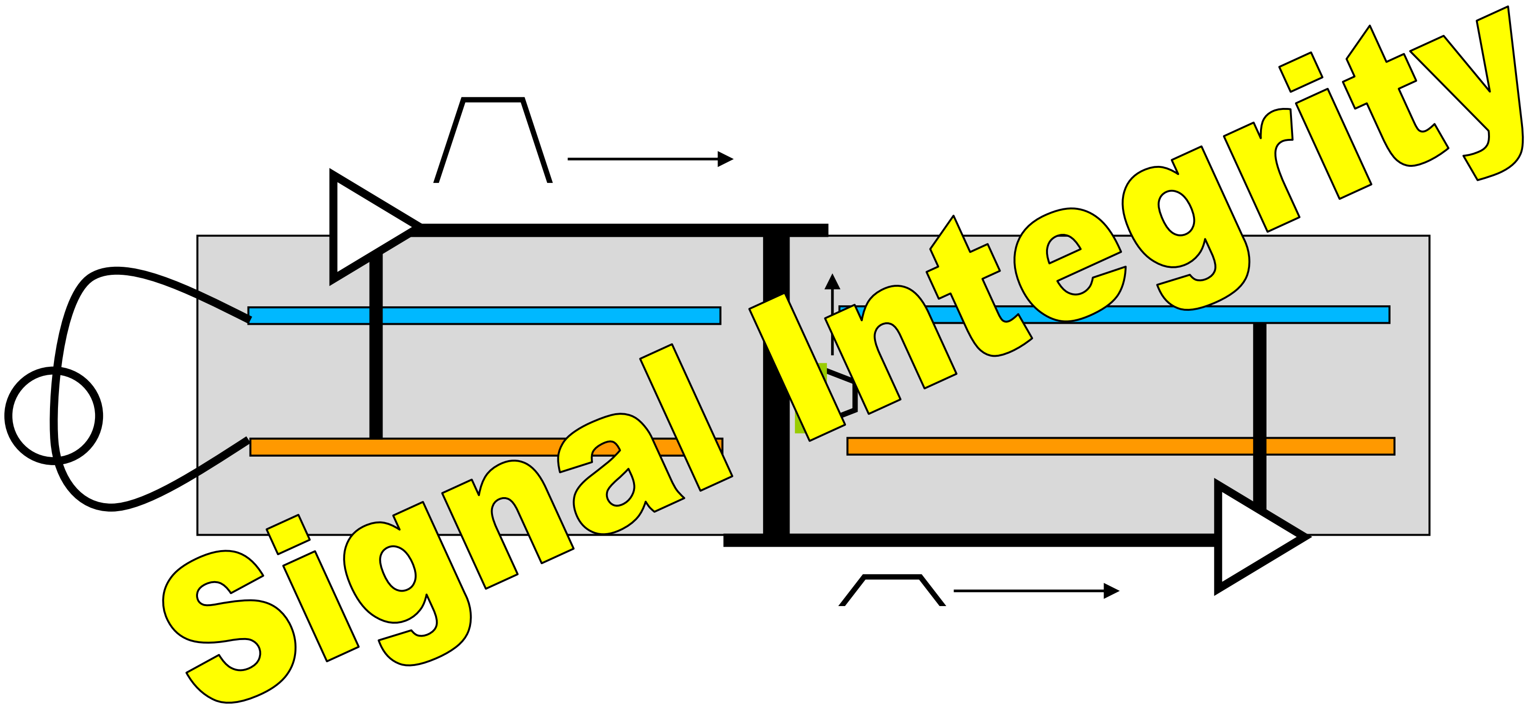
A Bird's Eye View on SI, PI & EMC



Signal Transmission Issues:

Attenuation, Reflection, Dispersion, Interference, Crosstalk

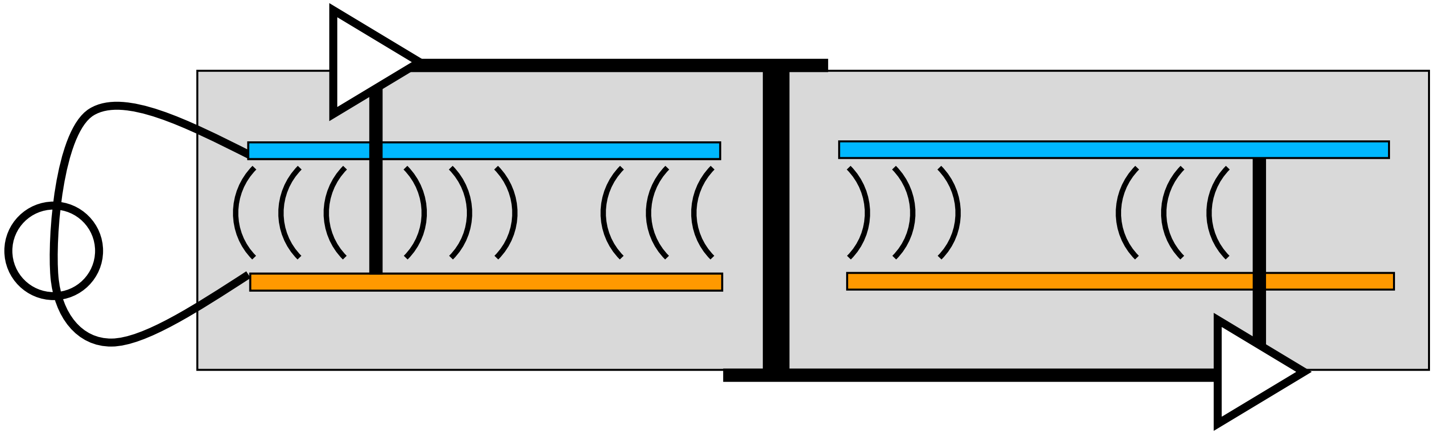
A Bird's Eye View on SI, PI & EMC



Signal Transmission Issues:

Attenuation, Reflection, Dispersion, Interference, Crosstalk

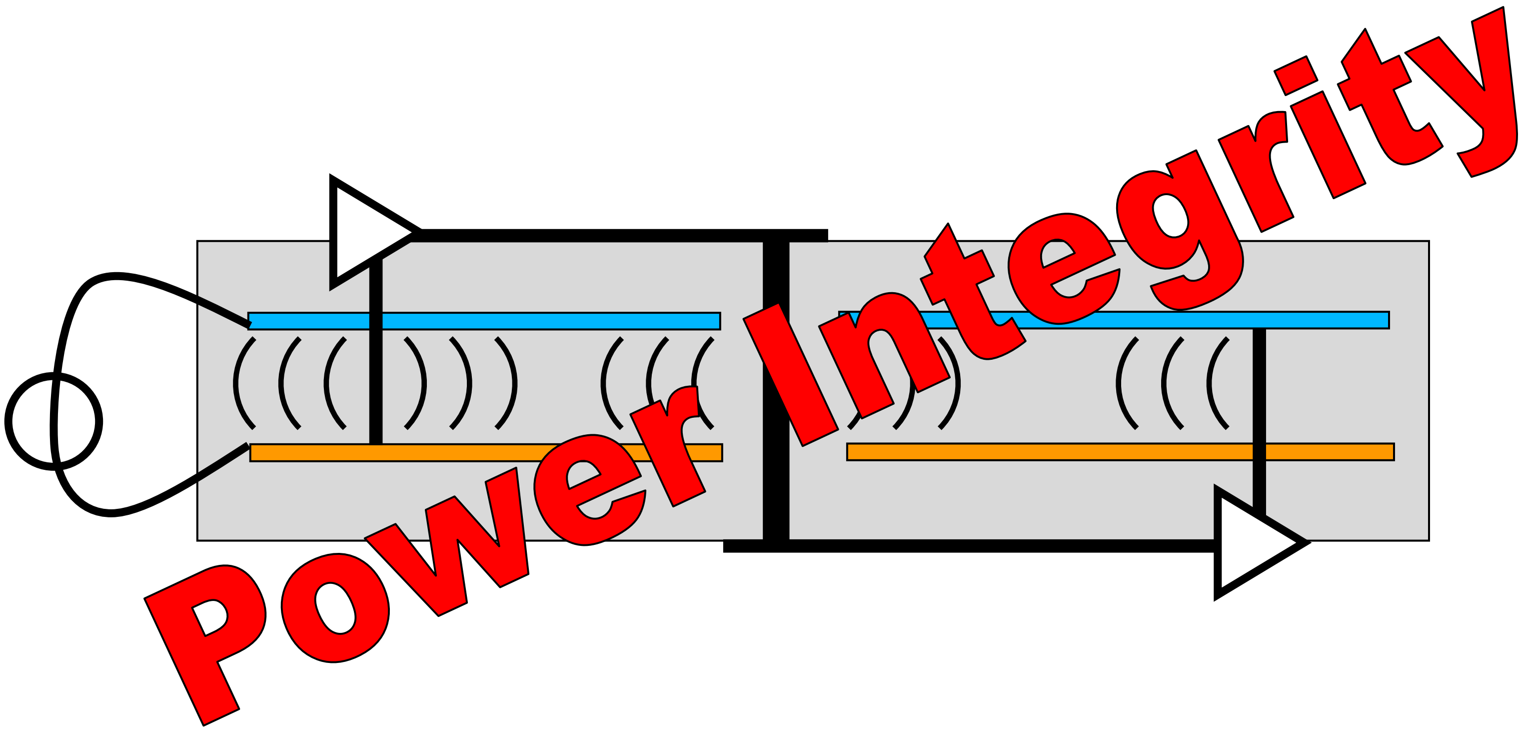
A Bird‘s Eye View on SI, PI & EMC



Power Delivery Issues:

Voltage Drop, Switching Noise, Crosstalk

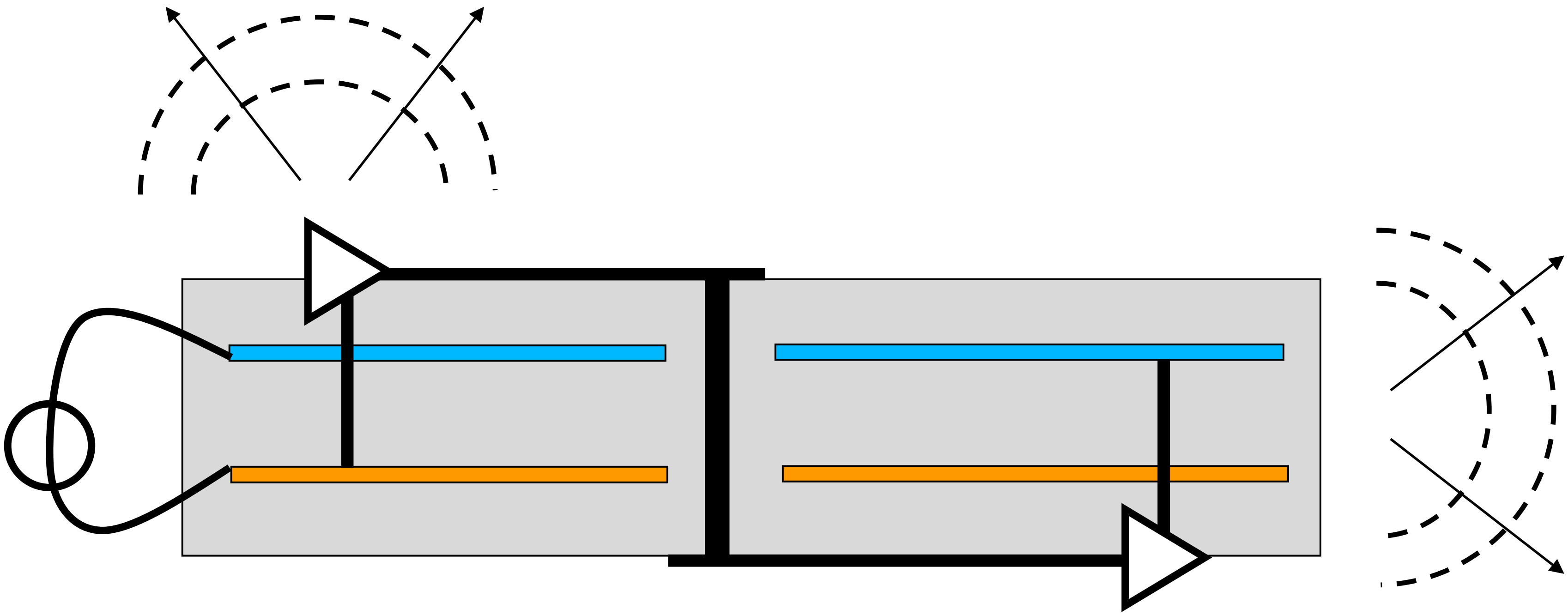
A Bird‘s Eye View on SI, PI & EMC



Power Delivery Issues:

Voltage Drop, Switching Noise, Crosstalk

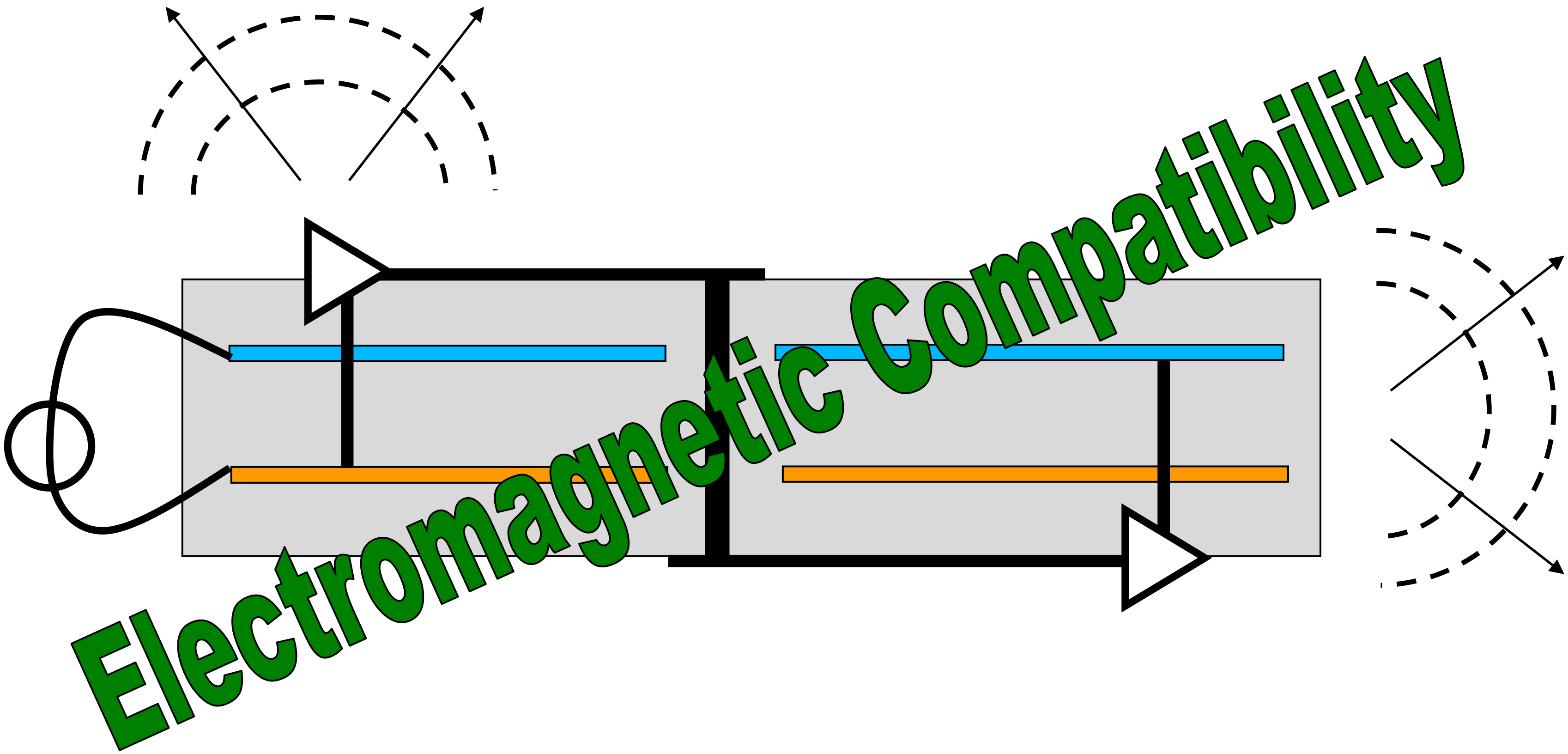
A Bird‘s Eye View on SI, PI & EMC



Electromagnetic Compatibility Issues:

Near Field Coupling, Radiated Emissions

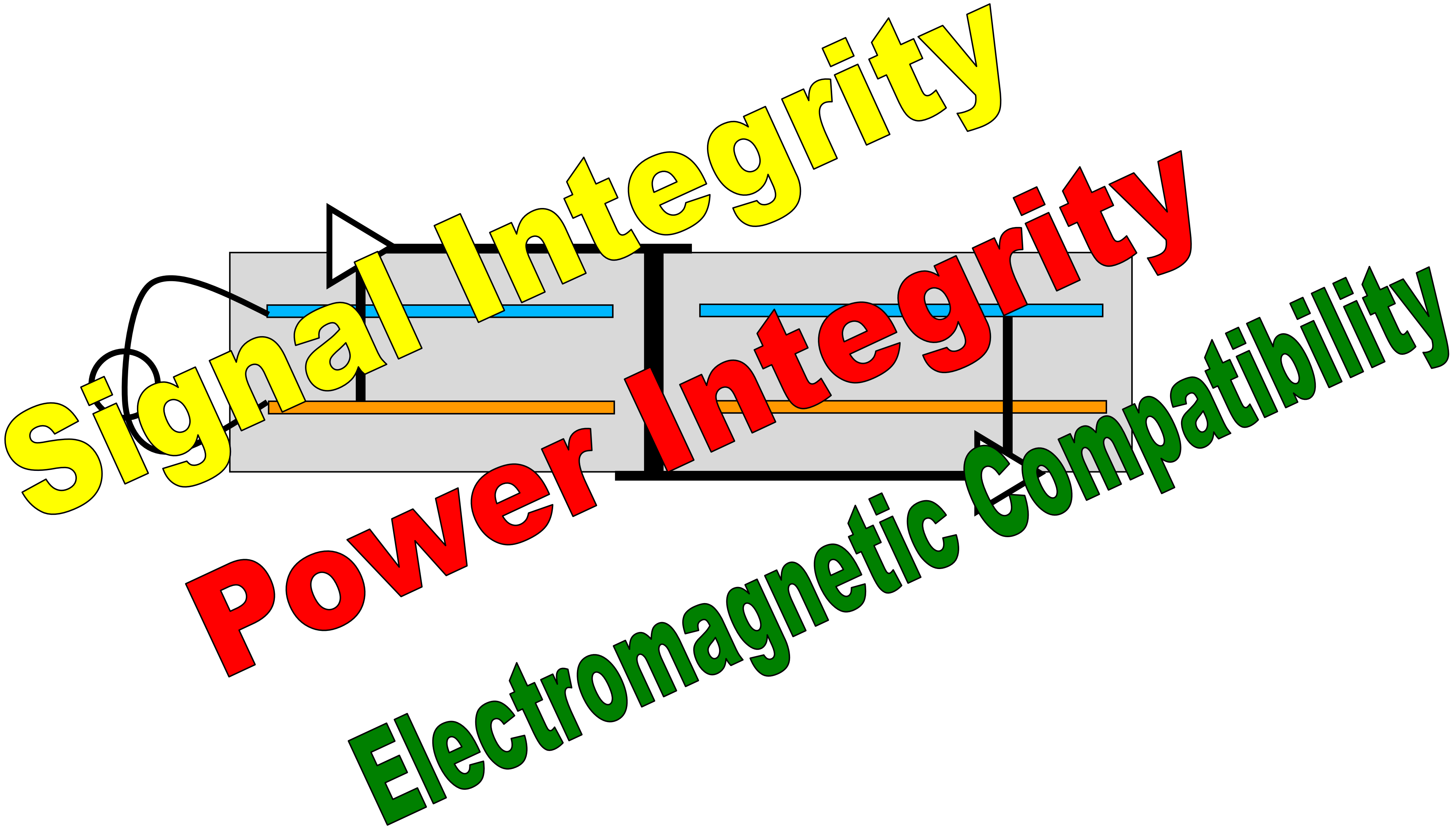
A Bird‘s Eye View on SI, PI & EMC



Electromagnetic Compatibility Issues:

Near Field Coupling, Radiated Emissions

SI + PI + EMC = “Electrical Integrity“



Outline

(1) Hamburg and TUHH

(2) Signal Integrity

(3) Power Integrity

(4) Vias and Return Currents

(5) Measurement Techniques

(6) Wrapping Up

(1)

Hamburg and TUHH

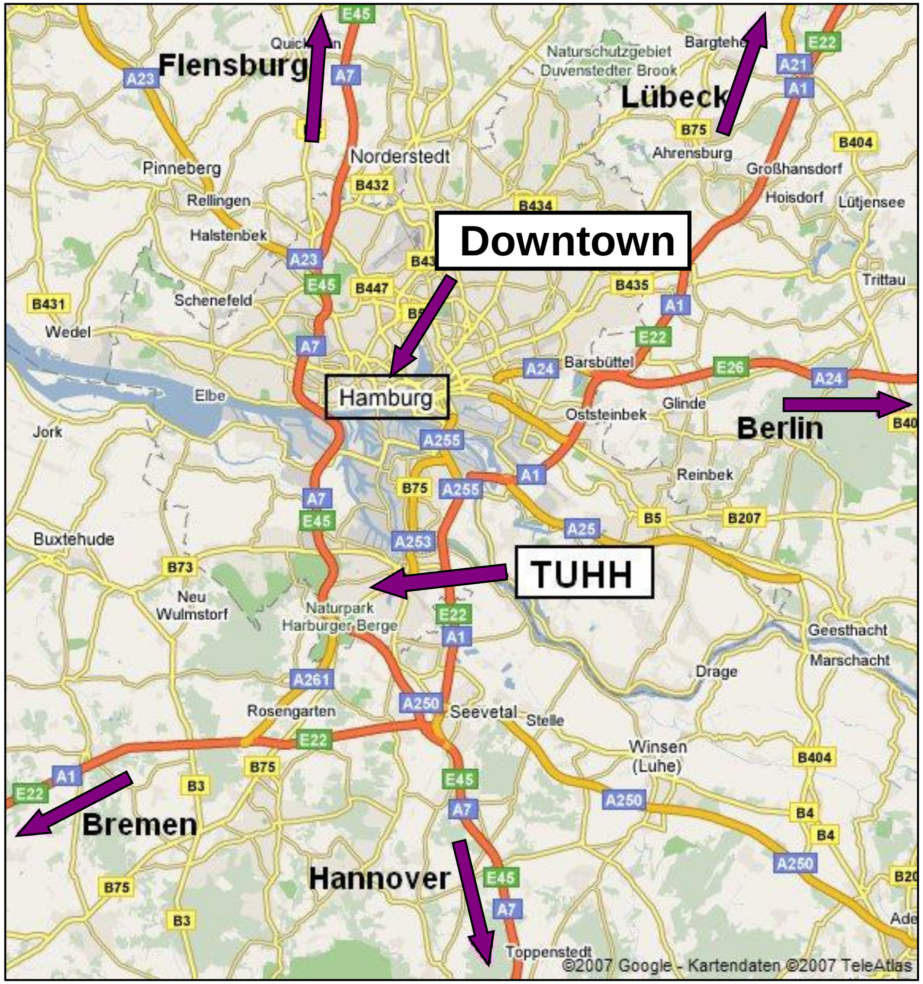

Hamburg
Bremen
Danmark
København
Deutschland
Berlin
Hannover
Amsterdam
Nederland
United Kingdom
London
France
Paris
Italia
Österreich
Schweiz
Suisse
Svizzera
©2007 Google - Kartendaten ©2007 TeleAtlas

Hamburg University of Technology

Founded 1978

Approx. 5000 Students

Approx. 100 Faculty Members



Hamburg University of Technology

What We Do at TUHH

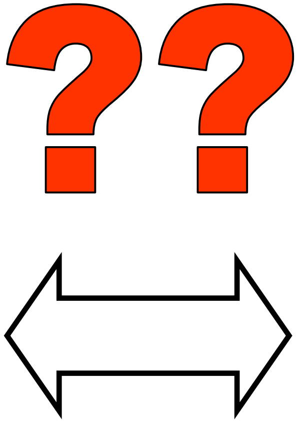
$$\nabla \cdot \vec{D} = \rho$$

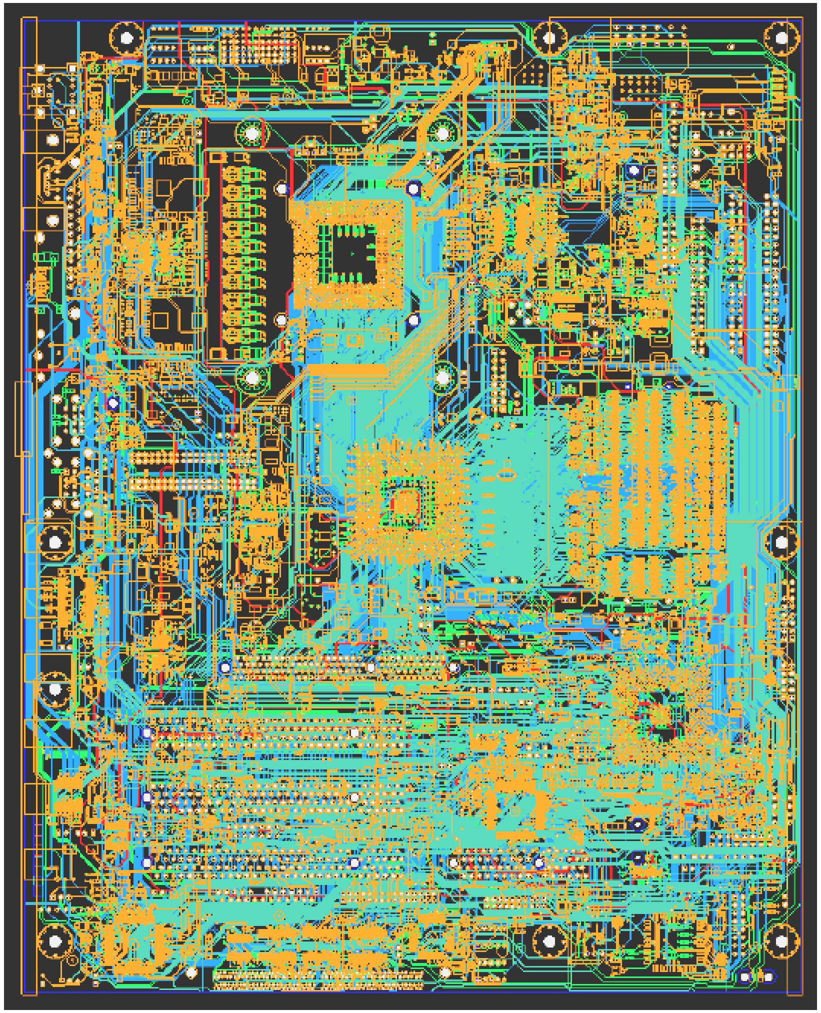
$$\nabla \cdot \vec{B} = 0$$

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$$

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t}$$

Maxwell‘s Equations



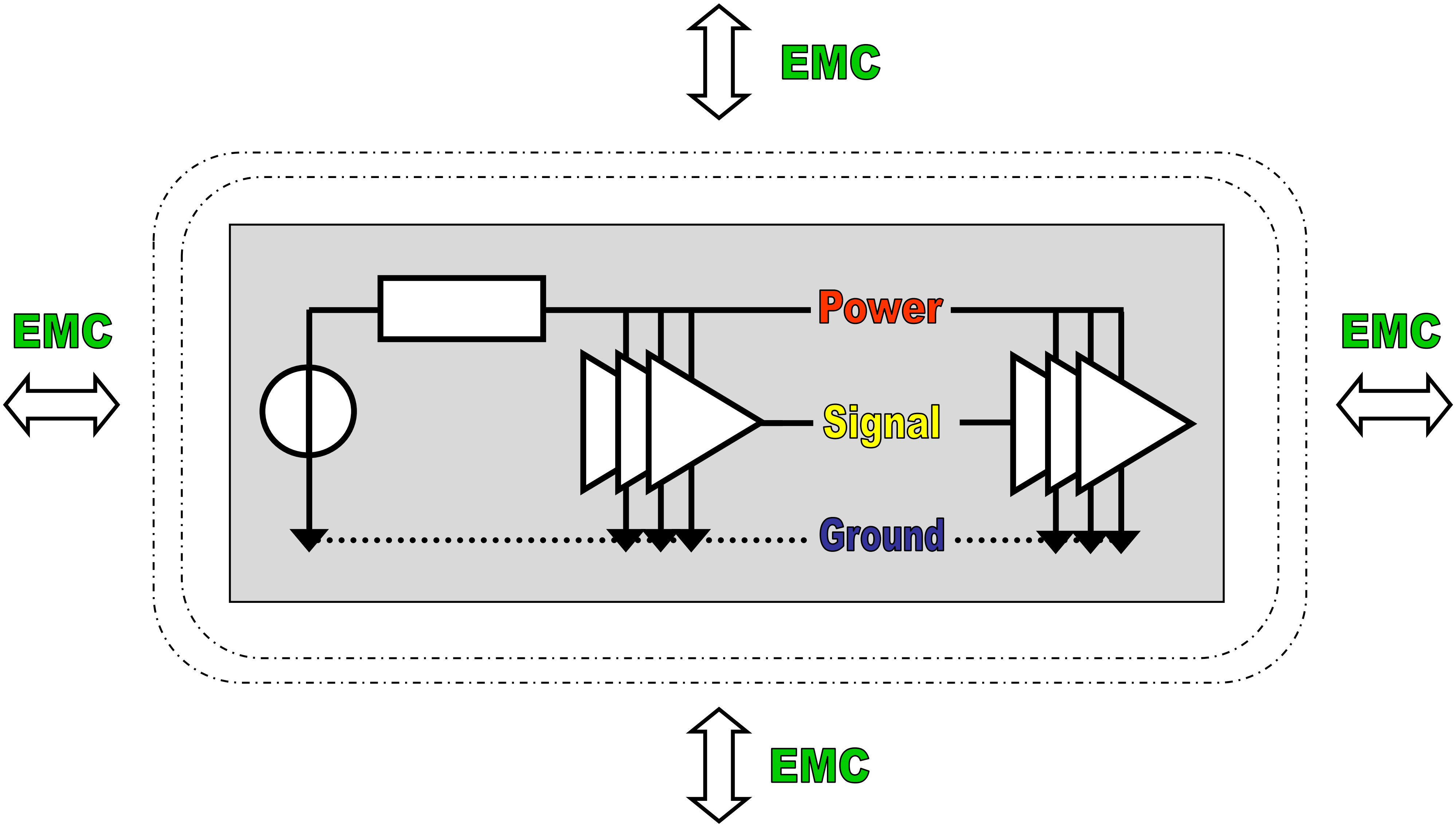


Printed circuit board layout

(2)

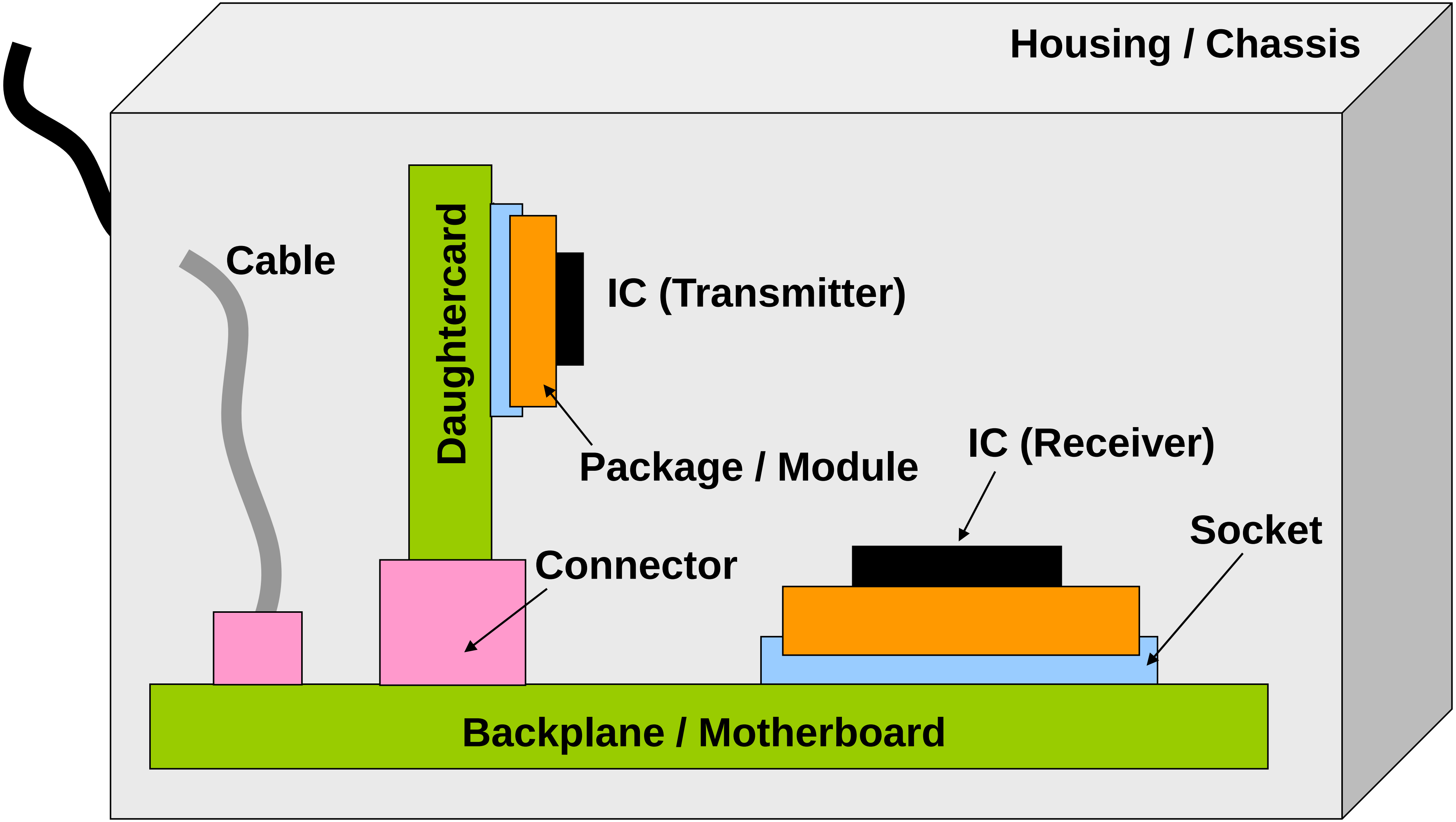
Signal Integrity

Electrical Integrity of Digital Systems

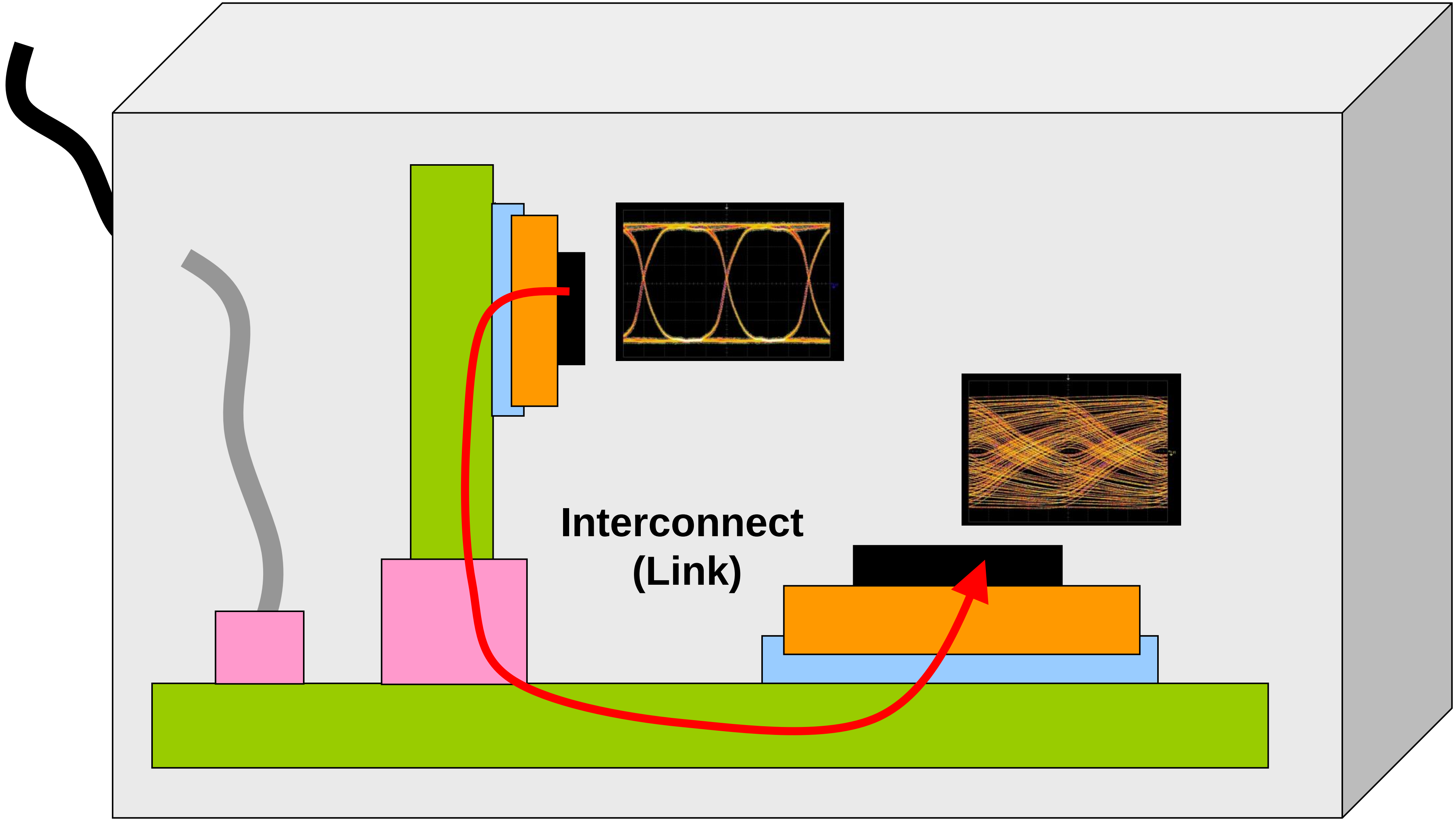


Christian Schuster – 19

Packaging of Digital Systems

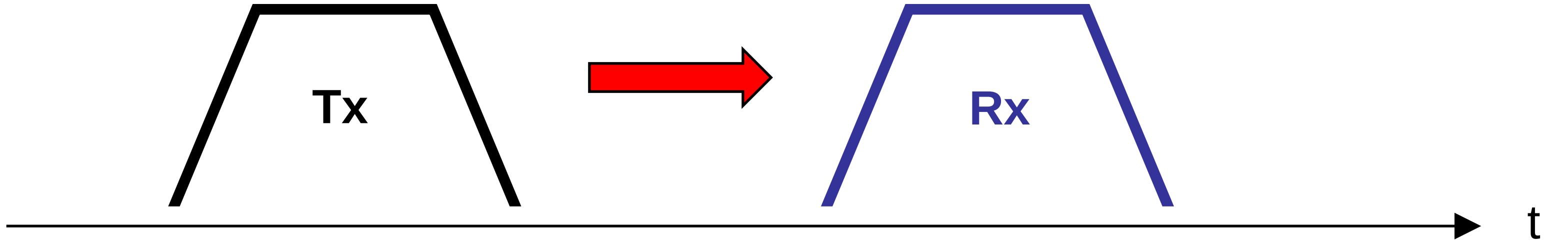


Packaging of Digital Systems

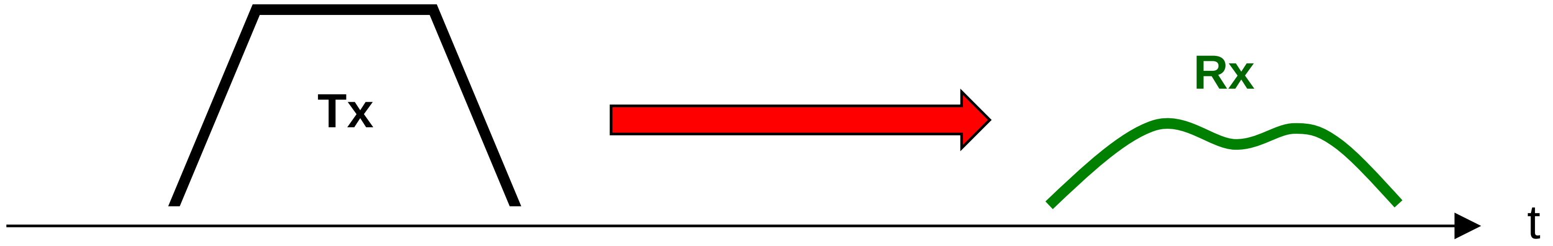


Effect of Interconnects

The ideal interconnect will simply delay the signal:

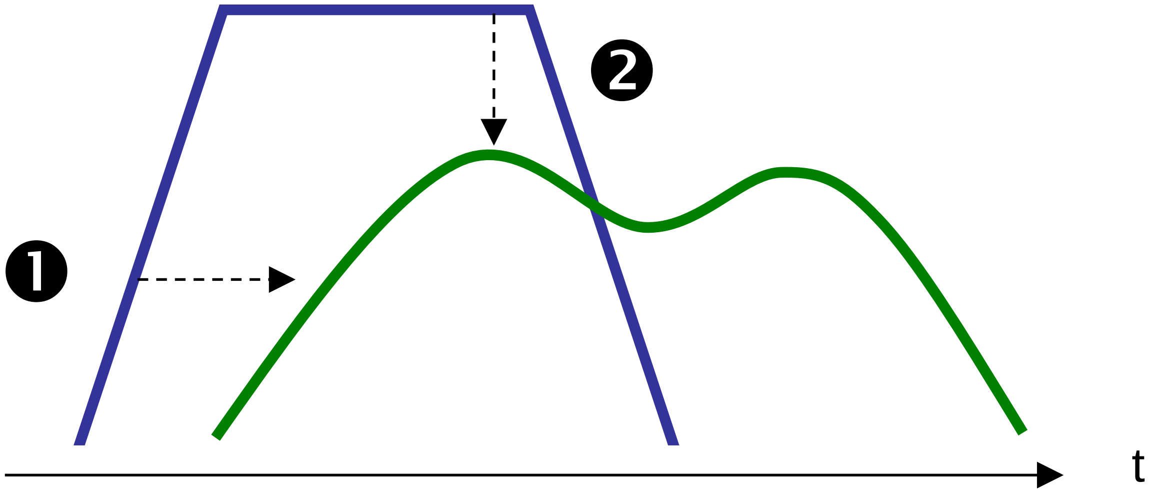


Any real interconnect will additionally change timing and amplitude:



Effect of Interconnects

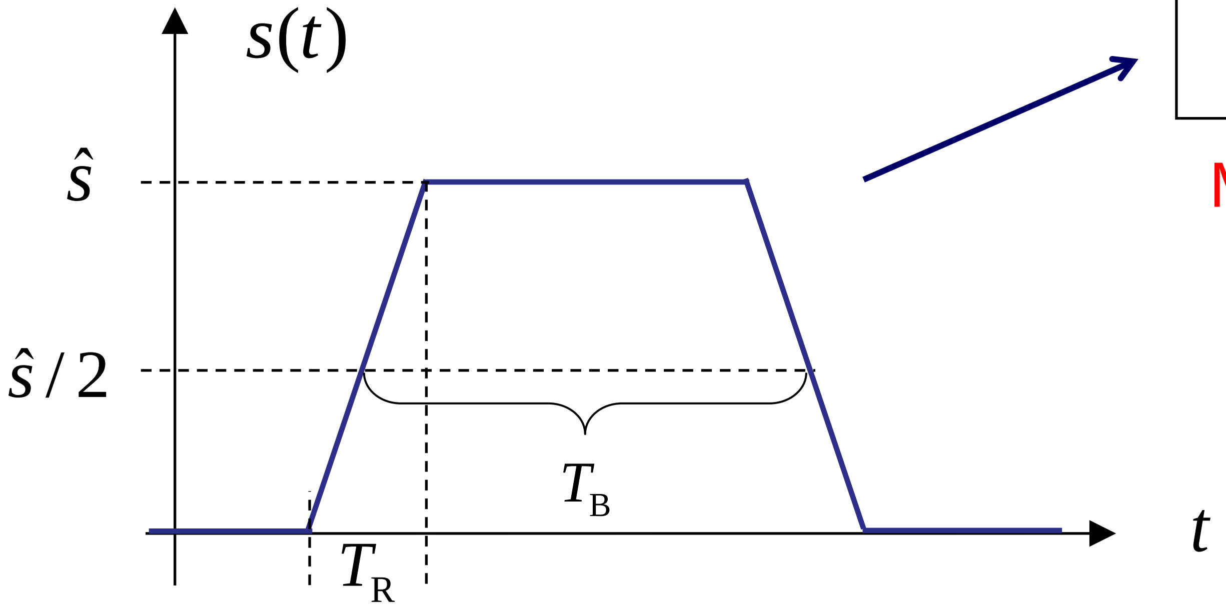
The deviations in timing and amplitude are in general called:



❶ Timing jitter or simply: **JITTER**

❷ Amplitude noise or simply: **NOISE**

Signal Bandwidth



$$f_{max} \approx \frac{1}{\pi T_R} \approx \frac{0.3\,..\,0.5}{\text{rise time}}$$

Maximum Frequency

$$f_0 = \frac{1}{2T_B} = \frac{0.5}{\text{bit period}}$$

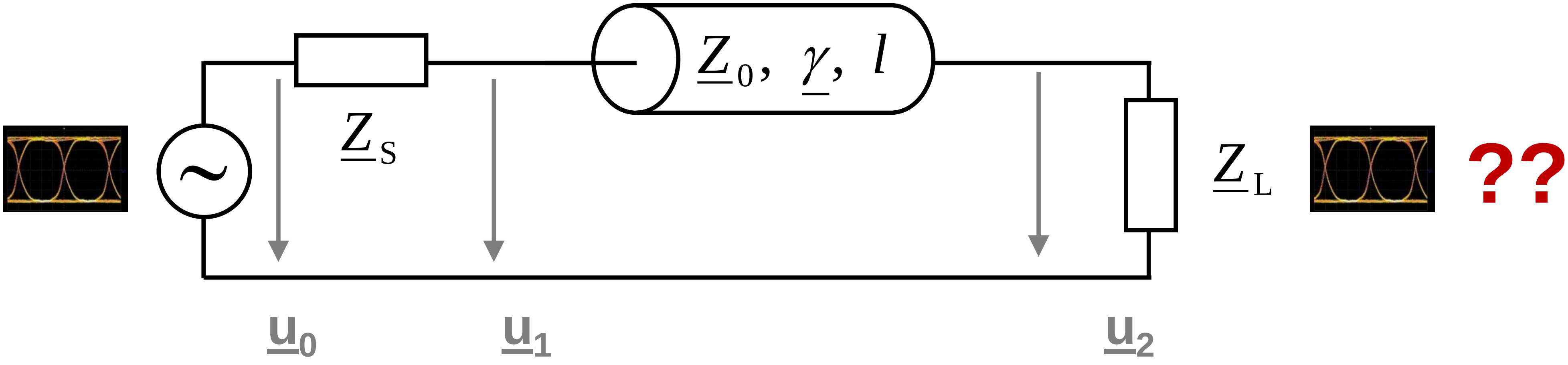
Fundamental Frequency

Maintaining Signal Integrity

1. Match terminations
2. Manage discontinuities
3. Reduce Coupling
4. Limit attenuation
5. Equalize signals

Effect of Terminations

Let‘s use the following interconnect (link) model:



Transmitter **Interconnect** **Receiver**

Transmission Lines in Digital Systems

Microstrip Line

$$Z_0 \approx \frac{87\Omega}{\sqrt{\varepsilon_{\mathrm{r}} + 1.41}} \cdot \ln\left(\frac{5.98 \cdot h}{0.8 \cdot w + t}\right)$$

(h = height of dielectric,
w = conductor width,
t = conductor thickness)

Stripline (symmetric)

$$Z_0 \approx \frac{60\Omega}{\sqrt{\varepsilon_{\mathrm{r}}}} \cdot \ln\left(\frac{1.9 \cdot h}{0.8 \cdot w + t}\right)$$

(h = height of dielectric,
w = conductor width,
t = conductor thickness)

Metal   Dielectric

Transmission Lines in Digital Systems

Typical trace length
≈ 5 – 75 cm

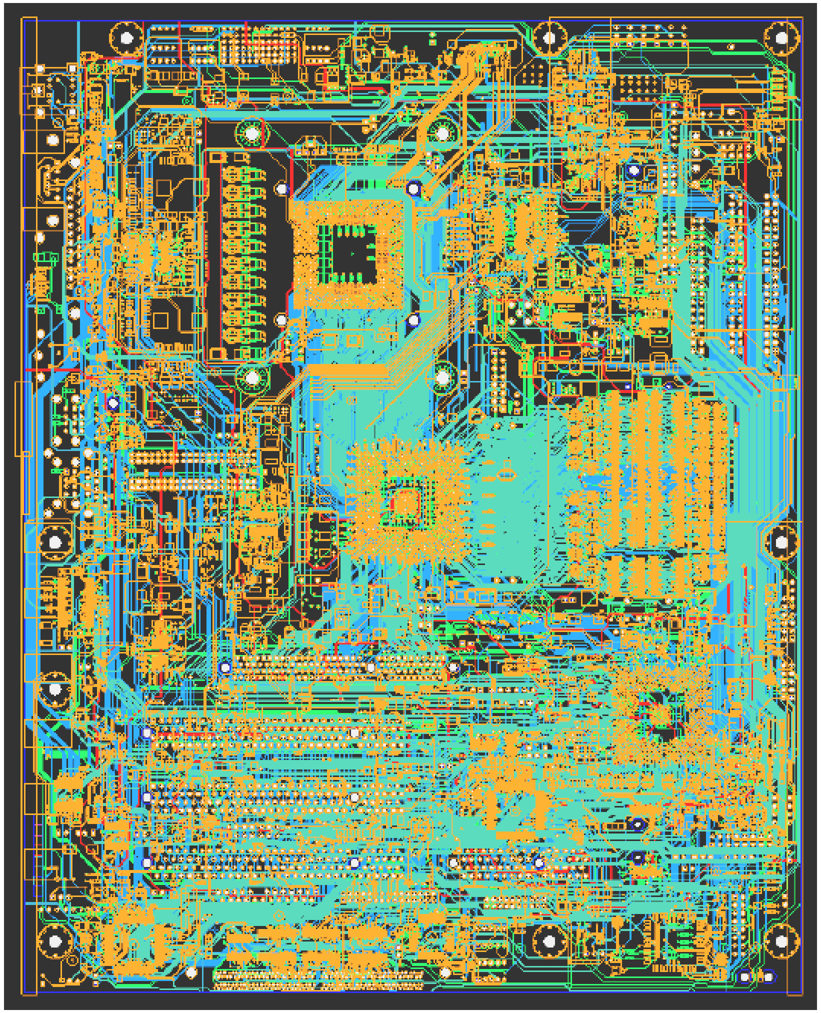
Velocity of propagation
≈ 150 000 km/s

Operating frequency
≈ 5 GHz

Corrsponding wavelength
≈ 3 cm

…

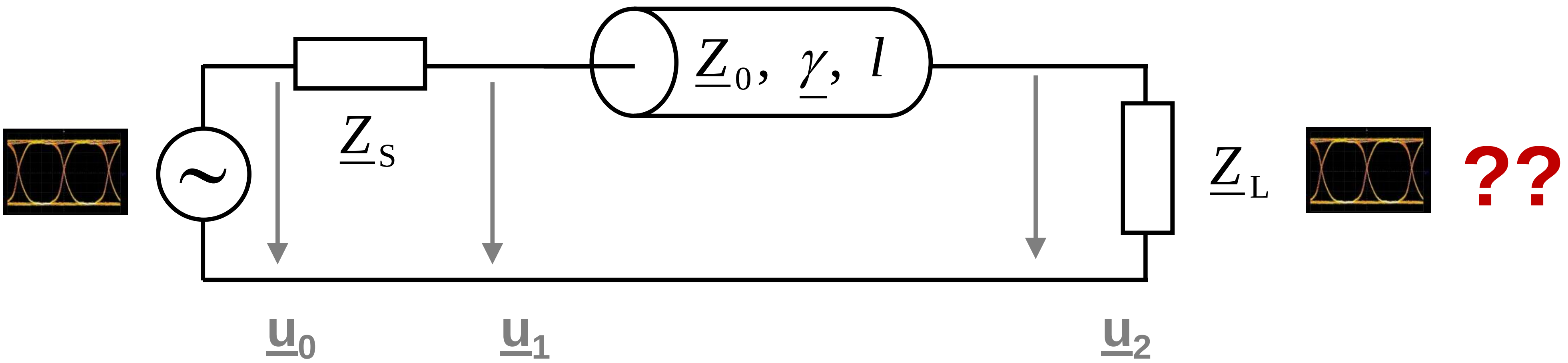
up to 25 wavelengths on a trace!



Printed circuit board layout

Effect of Terminations

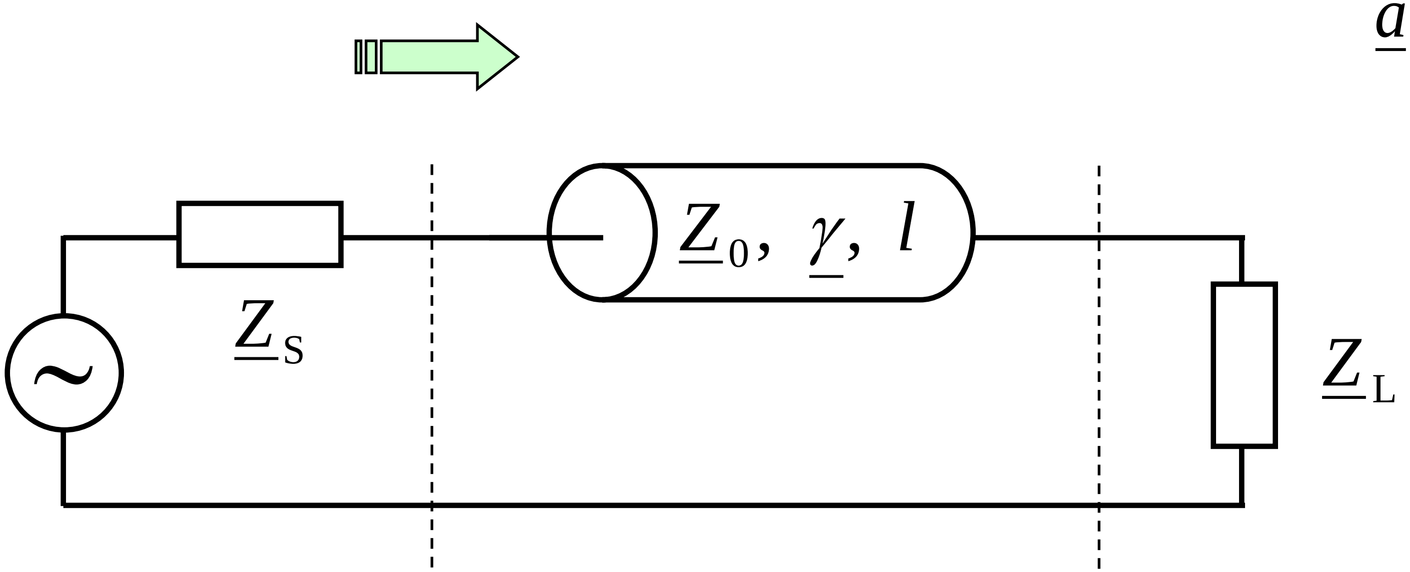
Let‘s use the following interconnect (link) model:



$$\Rightarrow \quad \frac{\underline{u}_2}{\underline{u}_0} = \text{const. and max. !}$$

Effect of Terminations

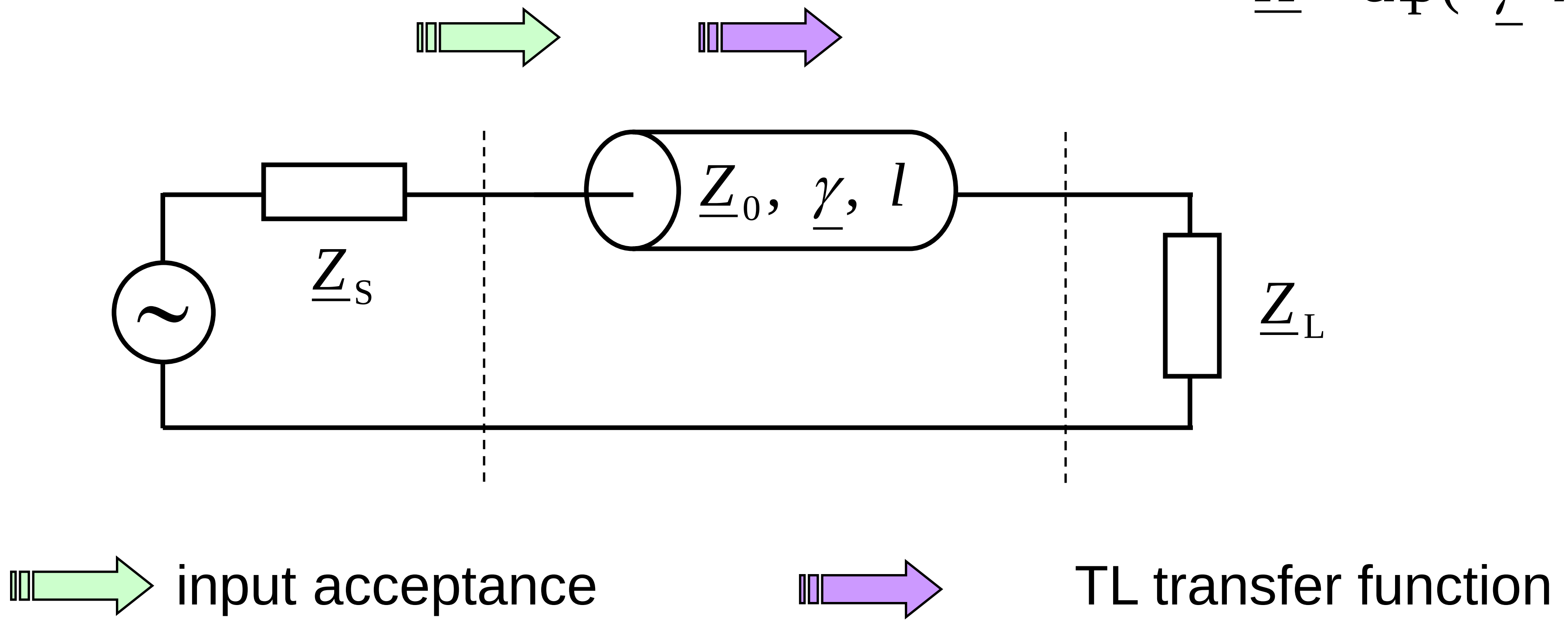
$$\underline{a} = \frac{\underline{Z}_0}{\underline{Z}_S + \underline{Z}_0}$$



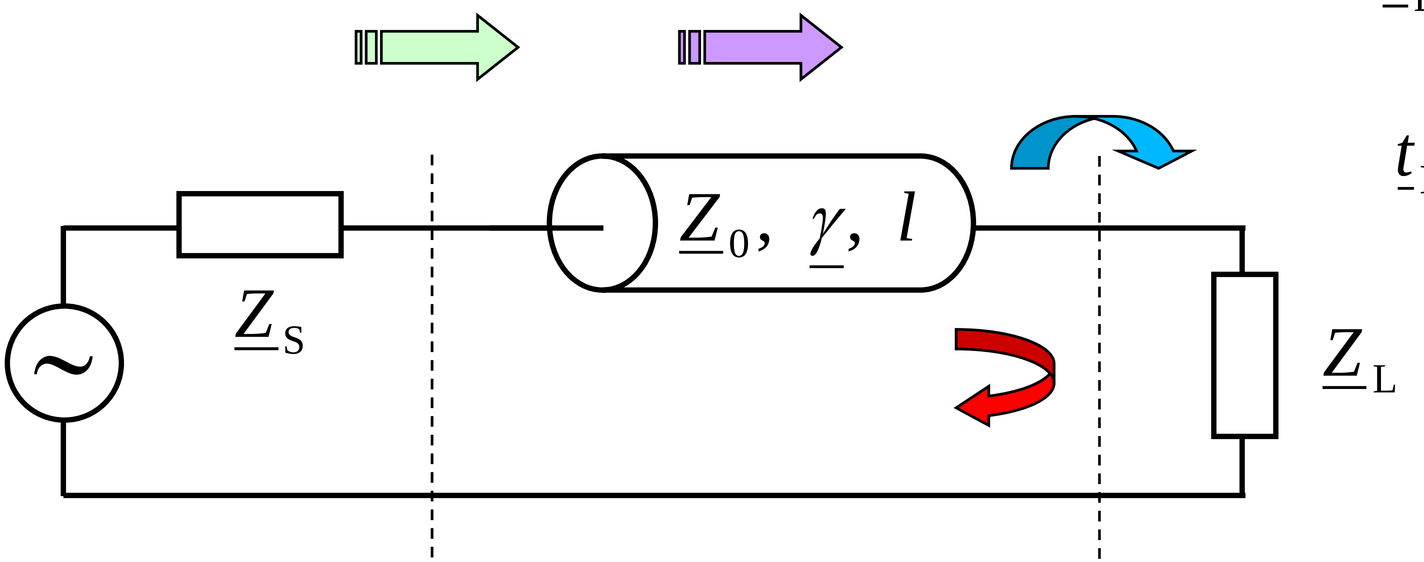
input acceptance

Effect of Terminations

$$\underline{H} = \exp(-\underline{\gamma} \cdot l)$$

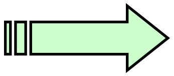


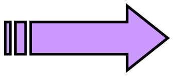
Effect of Terminations

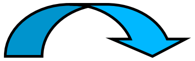


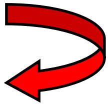
$$\underline{r}_L = \frac{\underline{Z}_L - \underline{Z}_0}{\underline{Z}_L + \underline{Z}_0}$$

$$\underline{t}_L = 1 + \underline{r}_L$$


input acceptance


TL transfer function

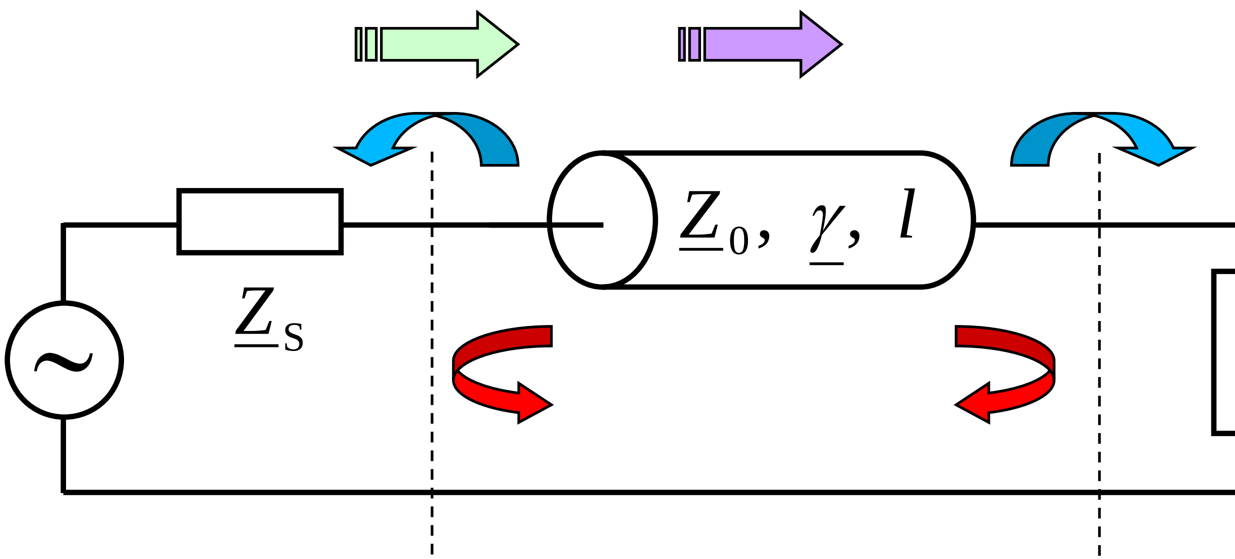

load transmission

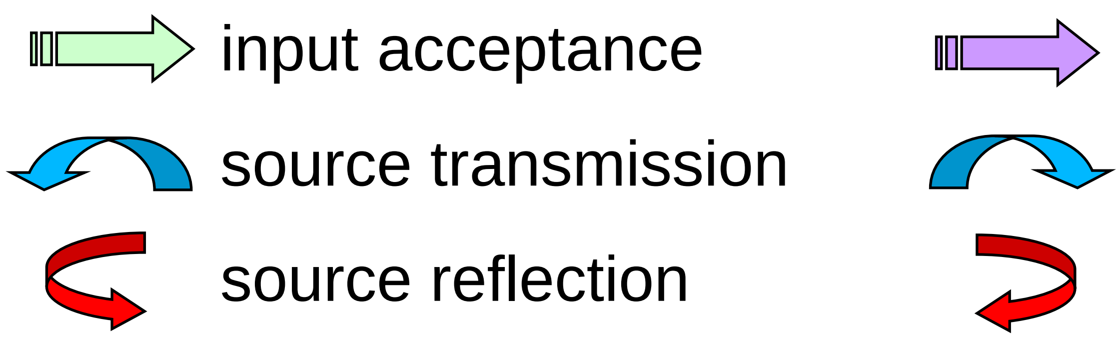

load reflection

Effect of Terminations

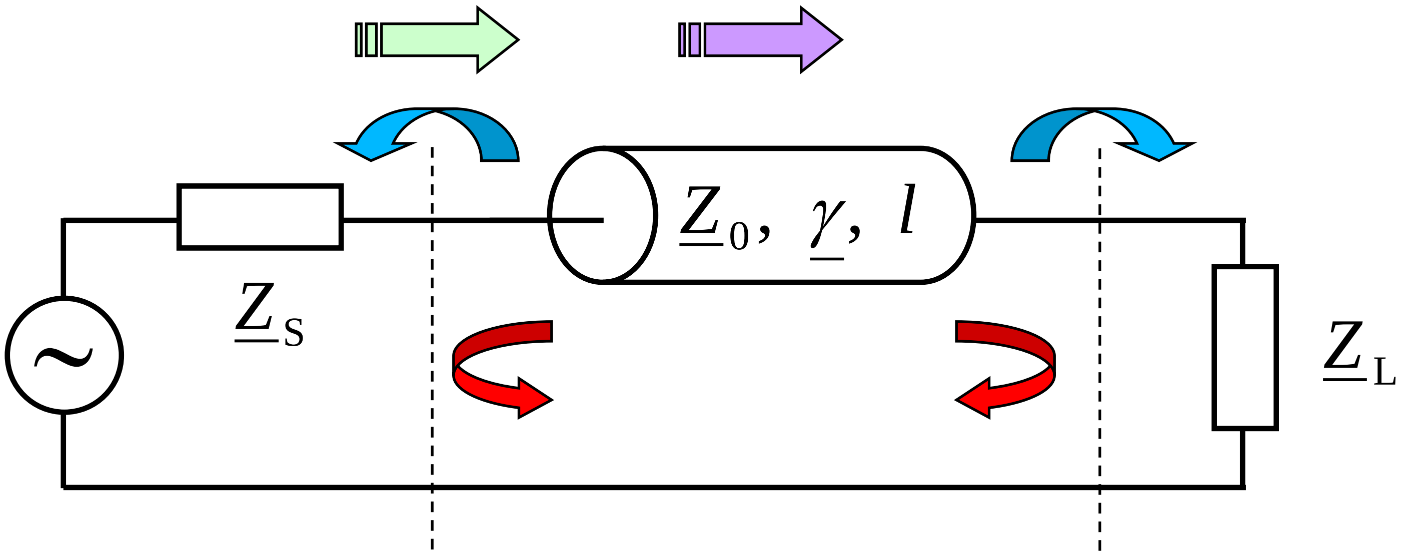
$$\underline{r}_S = \frac{\underline{Z}_S - \underline{Z}_0}{\underline{Z}_S + \underline{Z}_0}$$

$$\underline{t}_S = 1 + \underline{r}_S$$



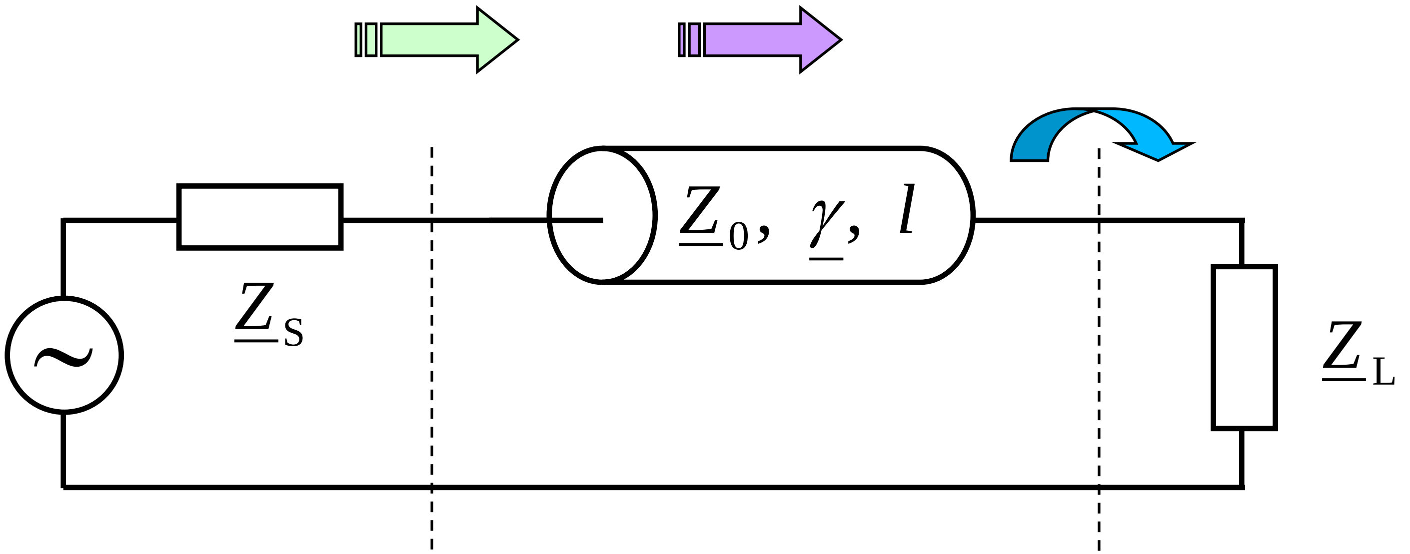


Effect of Terminations



$$\Rightarrow \quad \frac{\underline{u}_2}{\underline{u}_0} = \frac{\underline{a}\cdot\underline{H}\cdot\underline{t}_L}{1-\underline{H}^2\cdot\underline{r}_L\cdot\underline{r}_S} = ??$$

Effect of Terminations

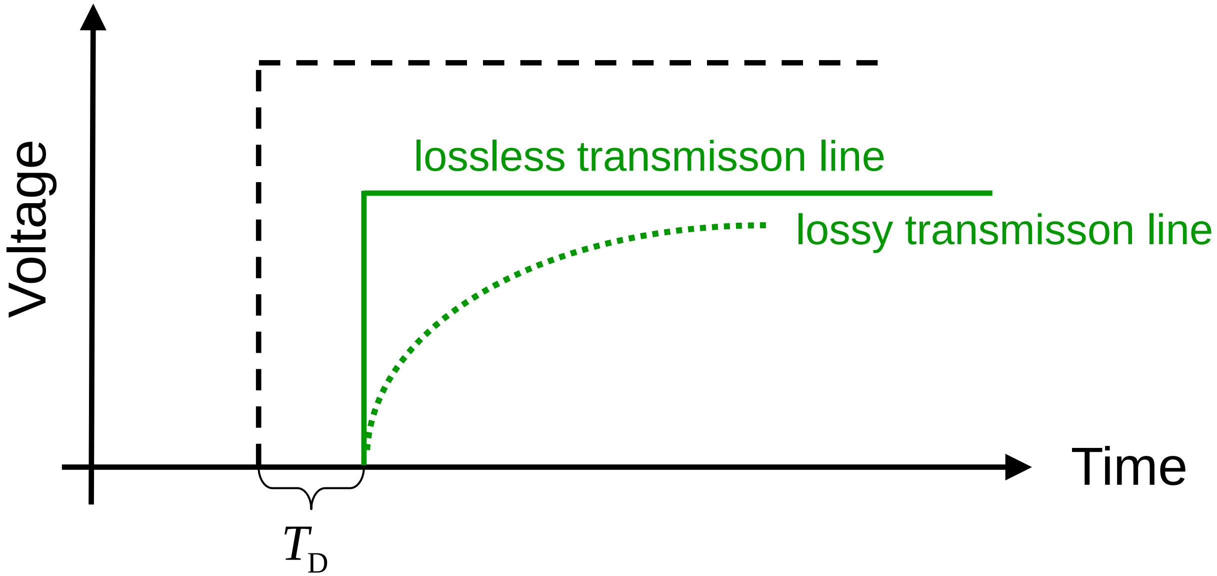


$$\boxed{\underline{Z}_\mathrm{L} = \underline{Z}_0} \rightarrow \frac{\underline{u}_2}{\underline{u}_0} = \underline{a} \cdot \underline{H}$$

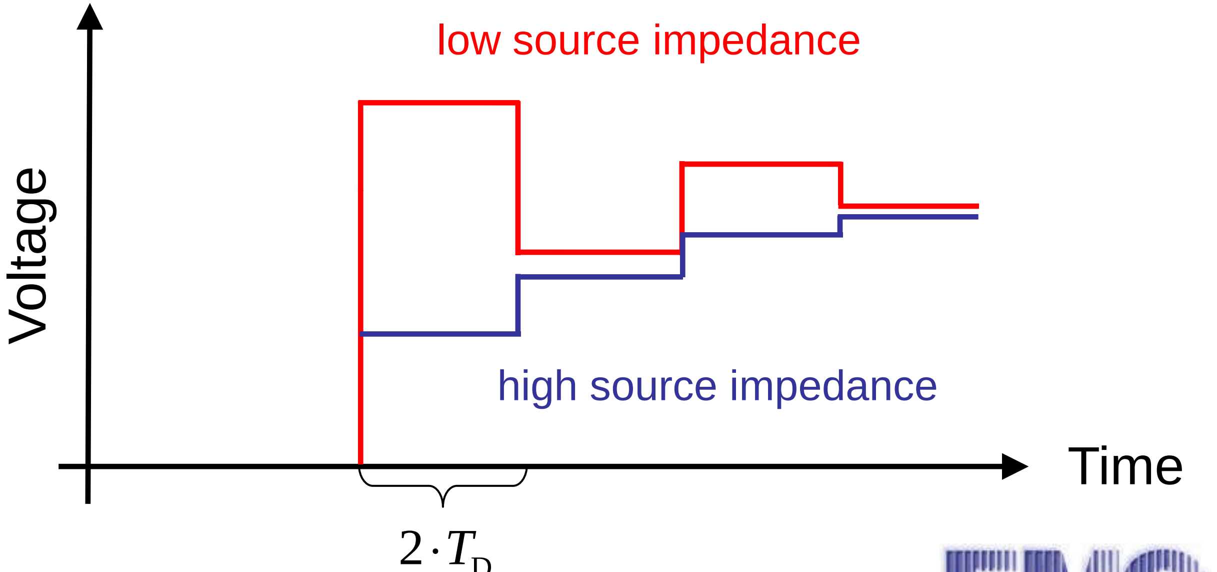
$$\boxed{\underline{Z}_\mathrm{S} = \underline{Z}_\mathrm{L} = \underline{Z}_0} \rightarrow \frac{\underline{u}_2}{\underline{u}_0} = \frac{1}{2} \cdot \underline{H}$$

Effect of Terminations

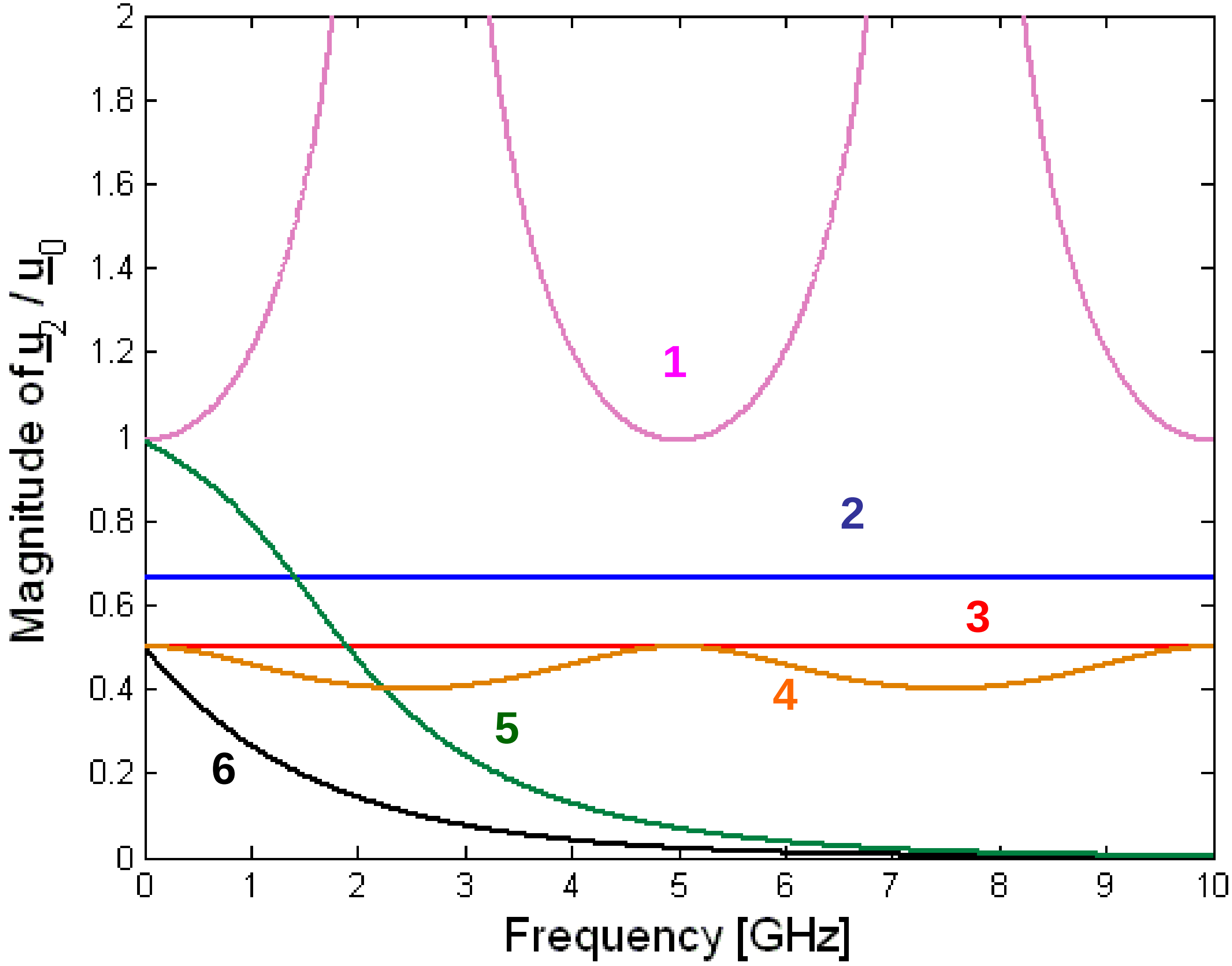
Matched interconnect:



Mismatched Interconnect:



Effect of Terminations



1 $\underline{Z}_S = 10\,\Omega,\ \underline{Z}_0 = 50\,\Omega,\ \underline{Z}_L = 1\,k\Omega$
zero losses

2 $\underline{Z}_S = 50\,\Omega,\ \underline{Z}_0 = 50\,\Omega,\ \underline{Z}_L = 100\,\Omega$
zero losses

3 $\underline{Z}_S = 50\,\Omega,\ \underline{Z}_0 = 50\,\Omega,\ \underline{Z}_L = 50\,\Omega$
zero losses

4 $\underline{Z}_S = 100\,\Omega,\ \underline{Z}_0 = 50\,\Omega,\ \underline{Z}_L = 100\,\Omega$
zero losses

5 $\underline{Z}_S = 10\,\Omega,\ \underline{Z}_0 = 50\,\Omega,\ \underline{Z}_L = 1\,k\Omega$
non-zero losses

6 $\underline{Z}_S = 50\,\Omega,\ \underline{Z}_0 = 50\,\Omega,\ \underline{Z}_L = 50\,\Omega$
non-zero losses

(all lines have a delay of 0.1 ns)

Matching Terminations

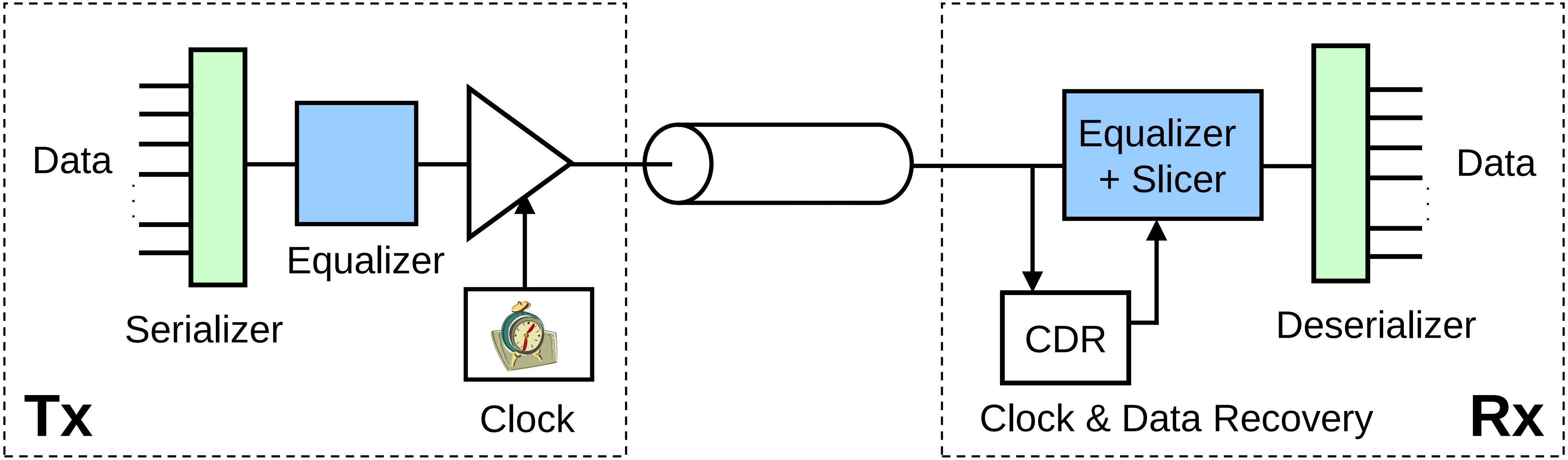
➔ Check your interconnect length $(2 \cdot T_{\mathrm{D}} > T_{\mathrm{R}})$!

➔ Check your interconnect impedance!

➔ Match receiver input impedance!

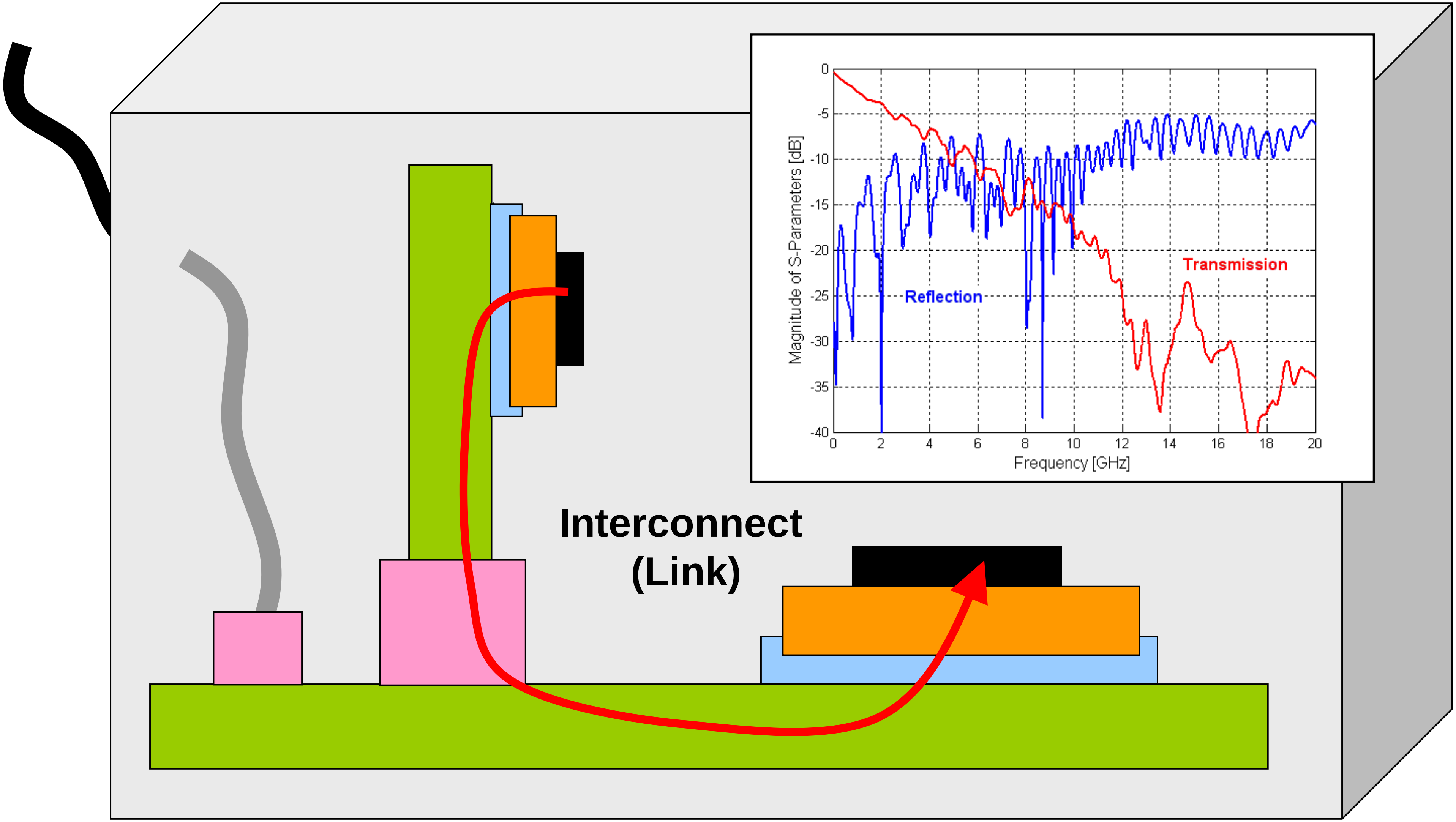
➔ Match transmitter output impedance!

Real World Interconnect (Link)

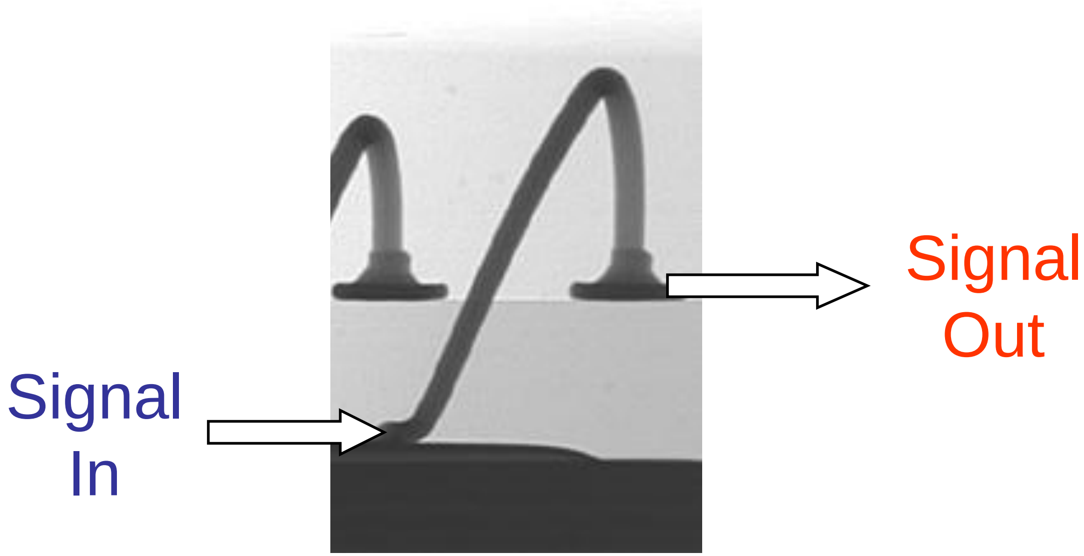


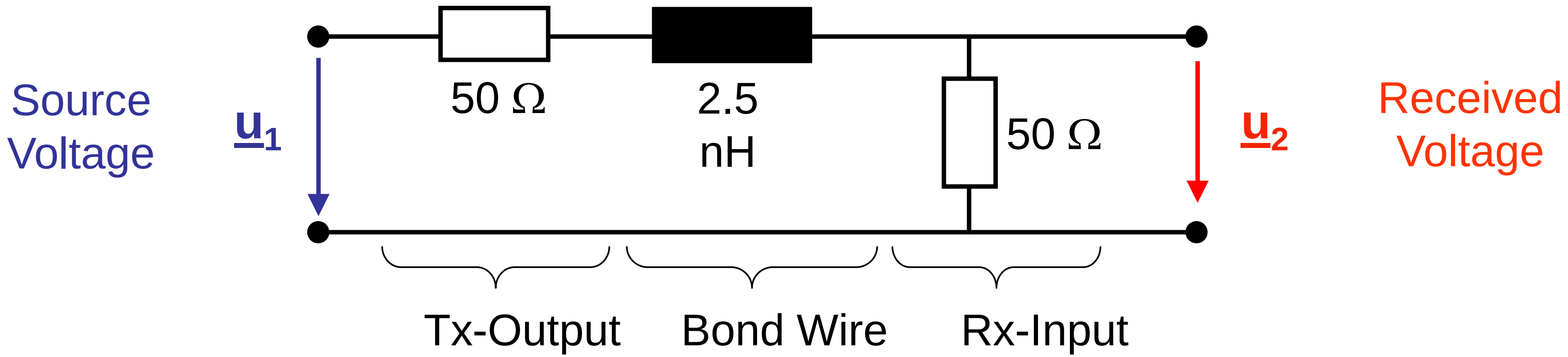
The technology is typically CMOS with the links being voltage mode, unidirectional, serial, point-to-point, and source-synchronous. For improved bandwidth equalization is typically used in the Tx, Rx, or both.

Packaging of Digital Systems



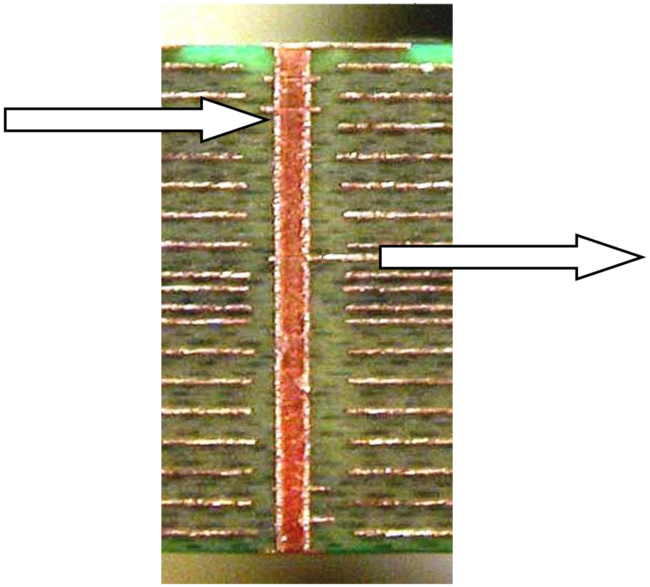
Effect of Lumped Discontinuities



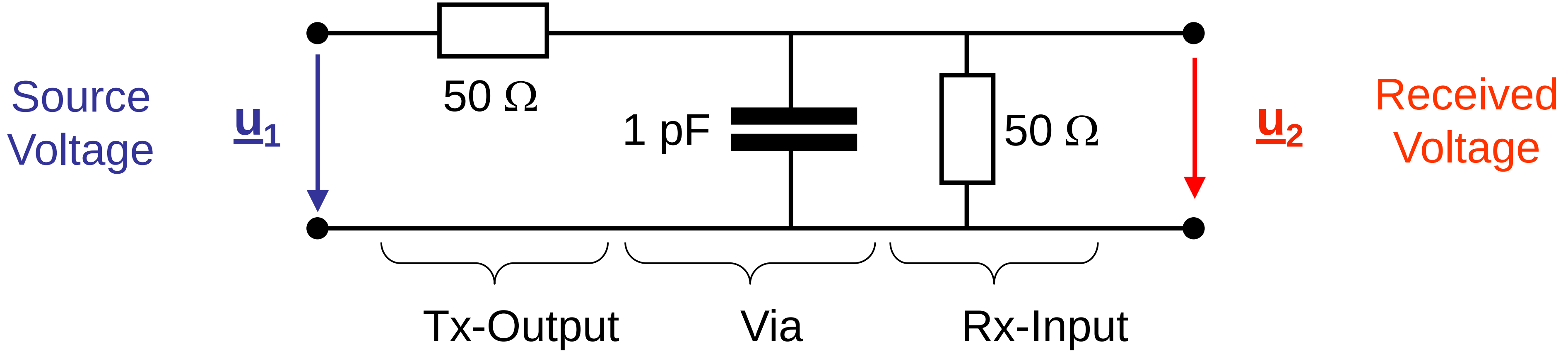


Effect of Lumped Discontinuities

Signal
In

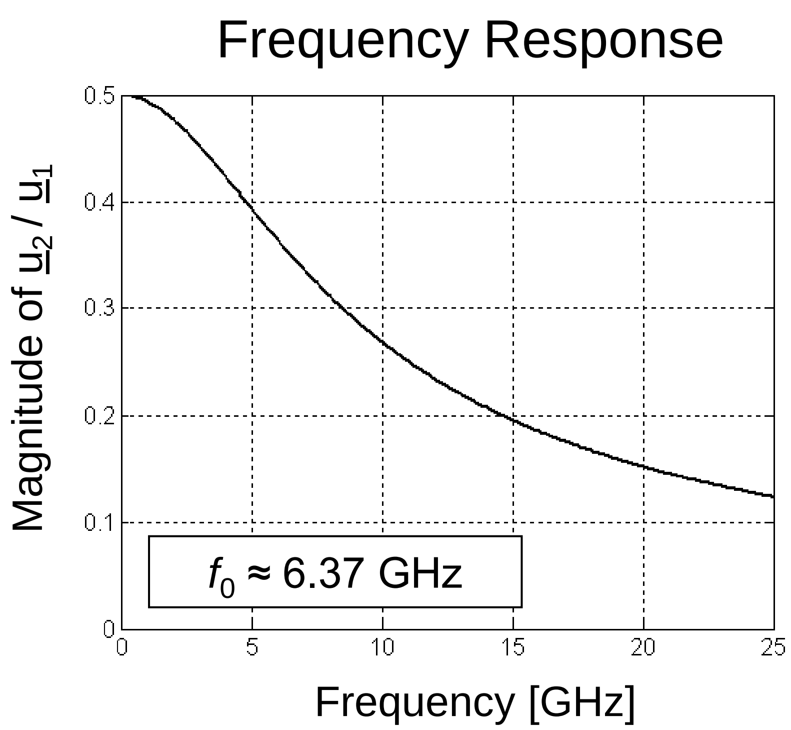


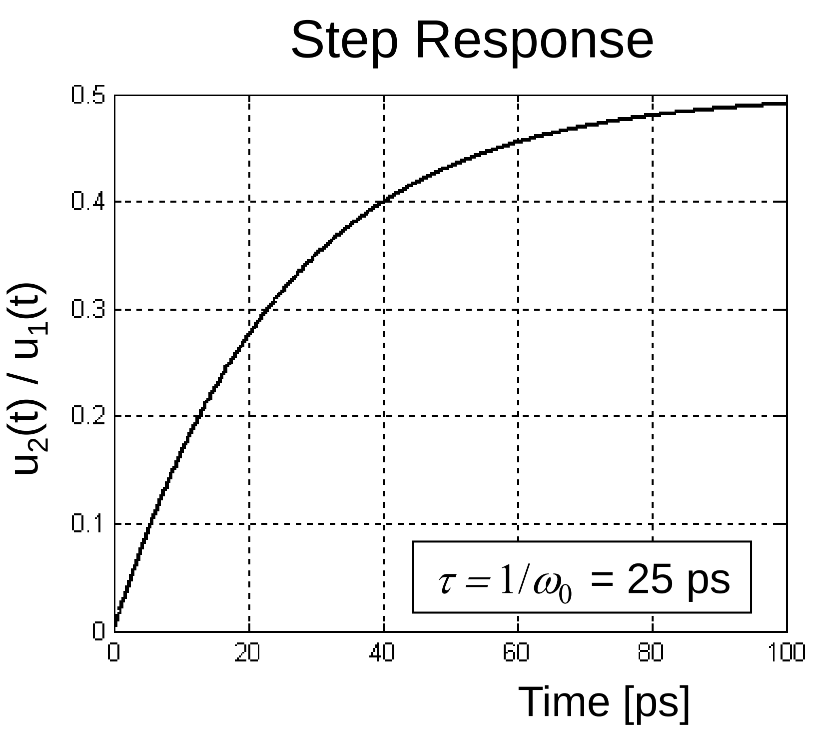
Signal
Out



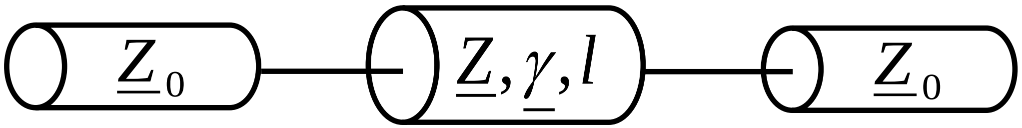
Effect of Lumped Discontinuities

- ➔ Attenuation of high frequency signal components
- ➔ „Slowing down" of the edges of a digital signal

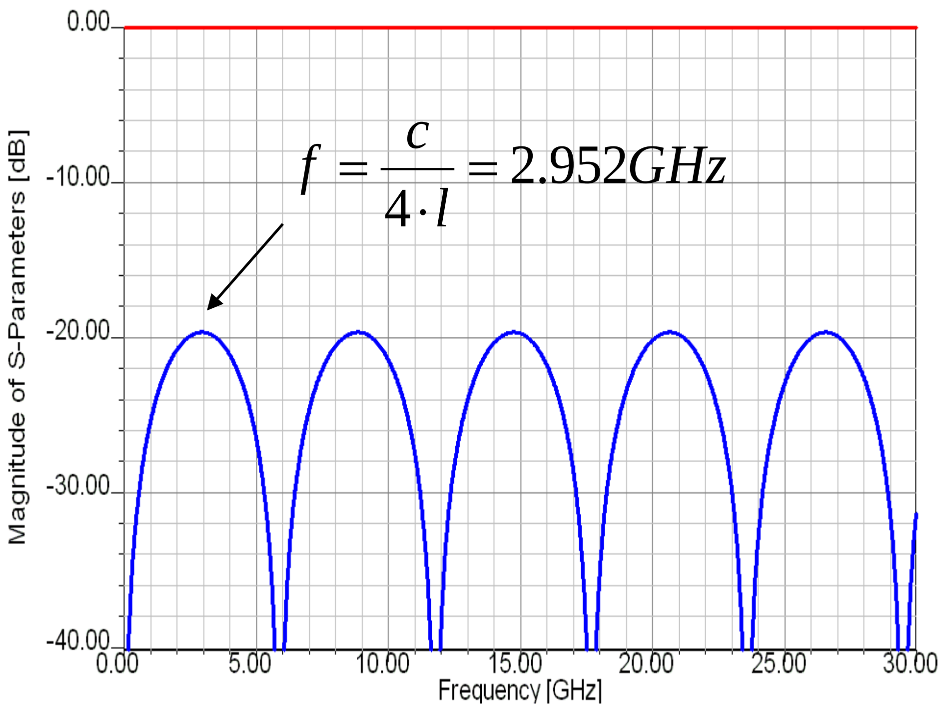




Effect of Distributed Discontinuities



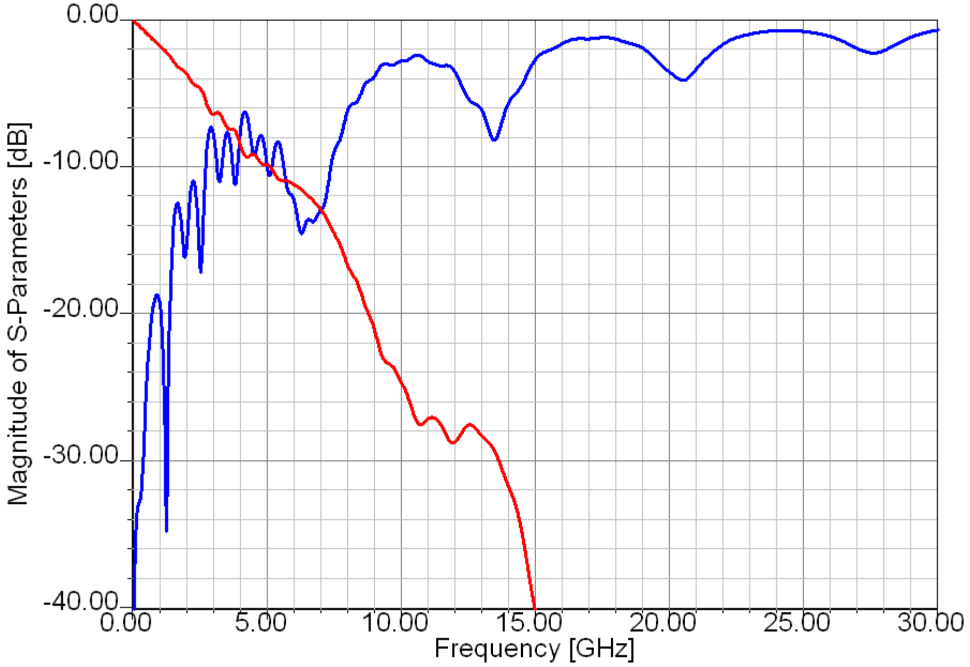
1 inch, 45 Ohm mismatched transmission line at c_0 /2

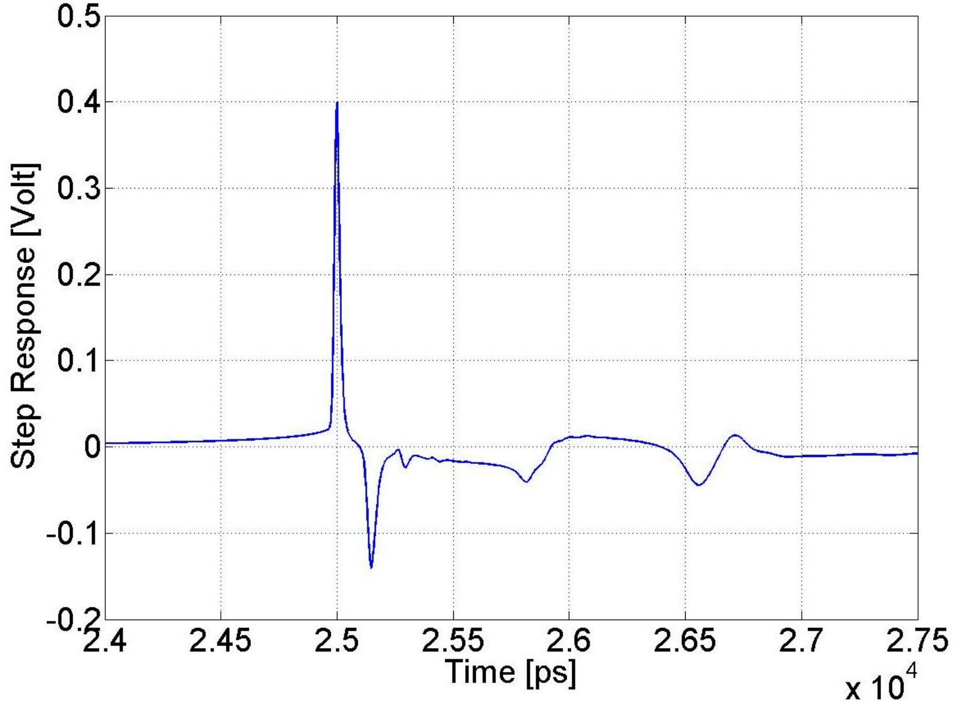


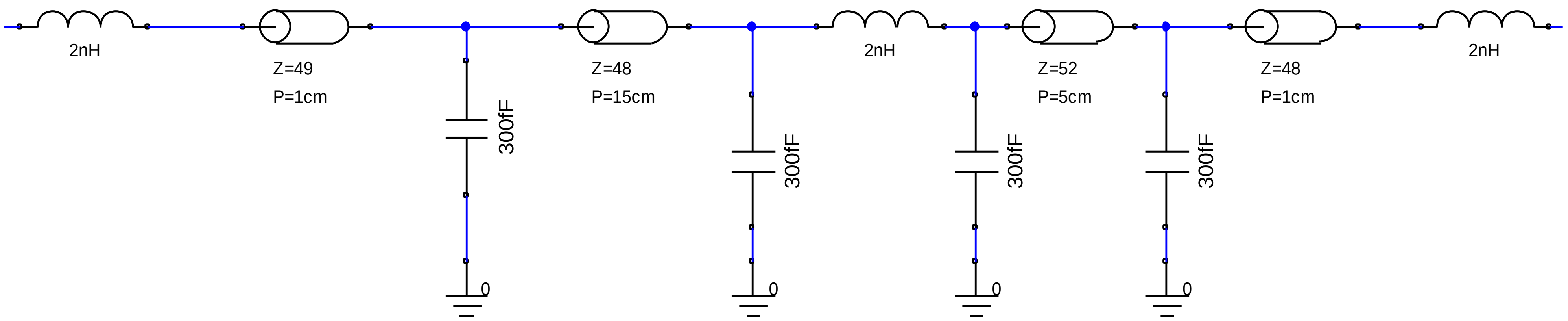
Frequency Response

(Scattering Parameters)

Overall Effect of Discontinuities



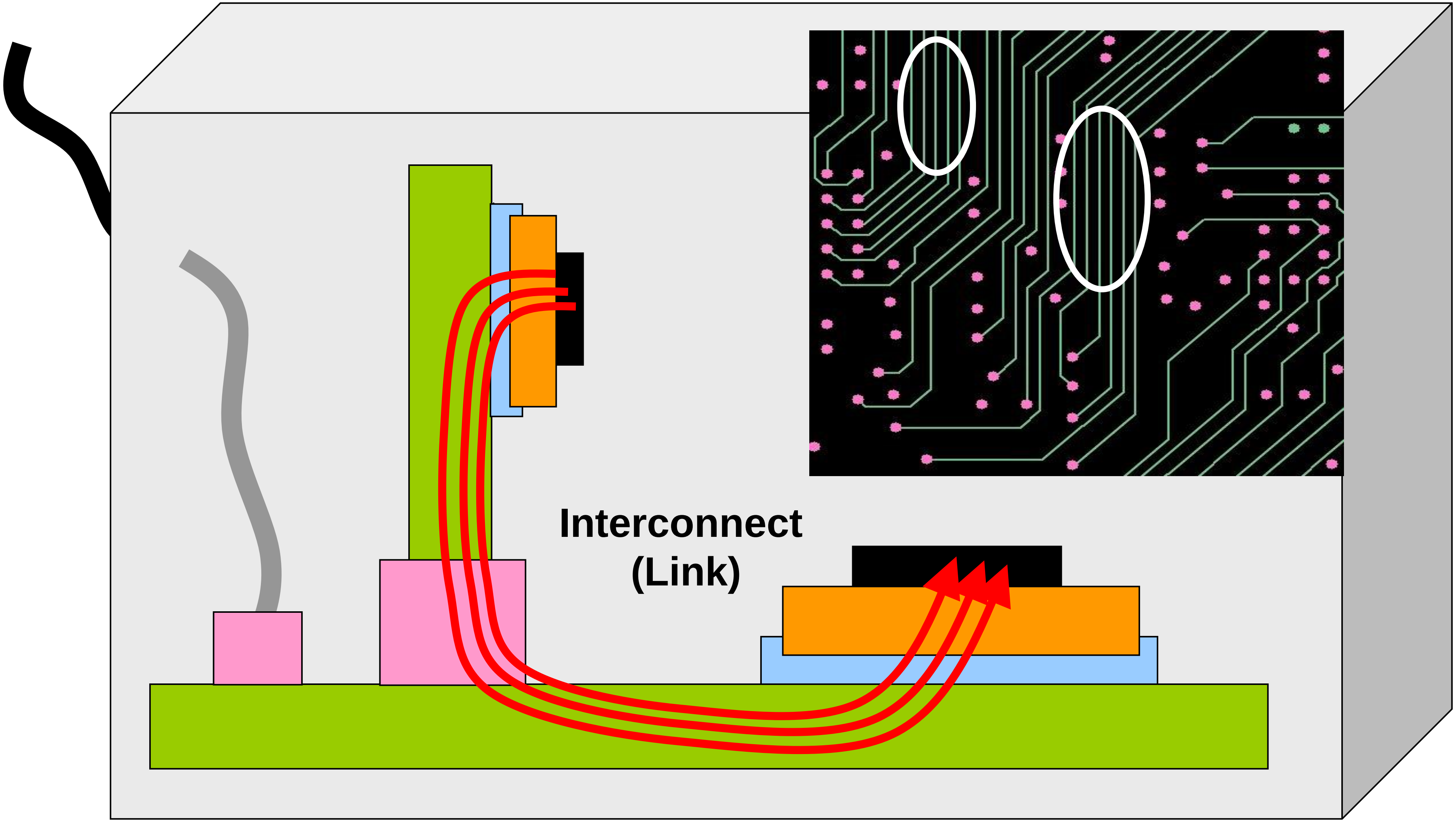




Managing Discontinuities

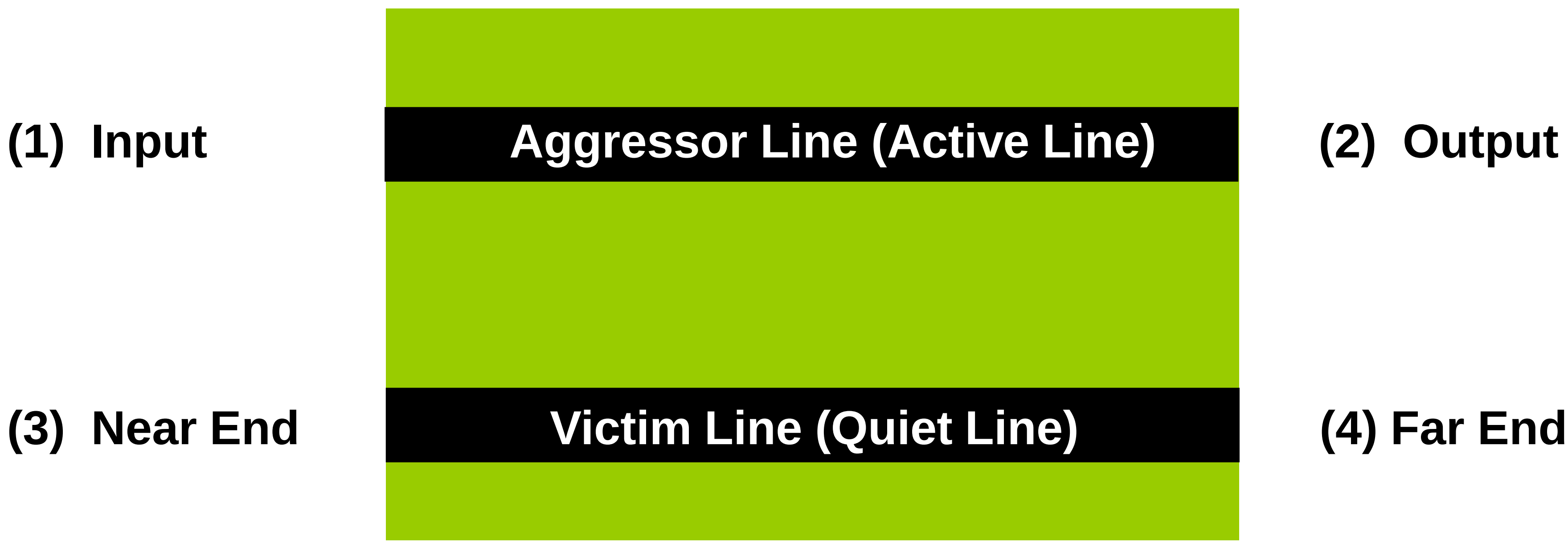
- ➔ Avoid them!
- ➔ Check their impact!
- ➔ Minimize them (± 10 Ohm around 50 Ohm)!
- ➔ Compensate them (difficult)!
- ➔ Concentrate on the “bottleneck!

Packaging of Digital Systems



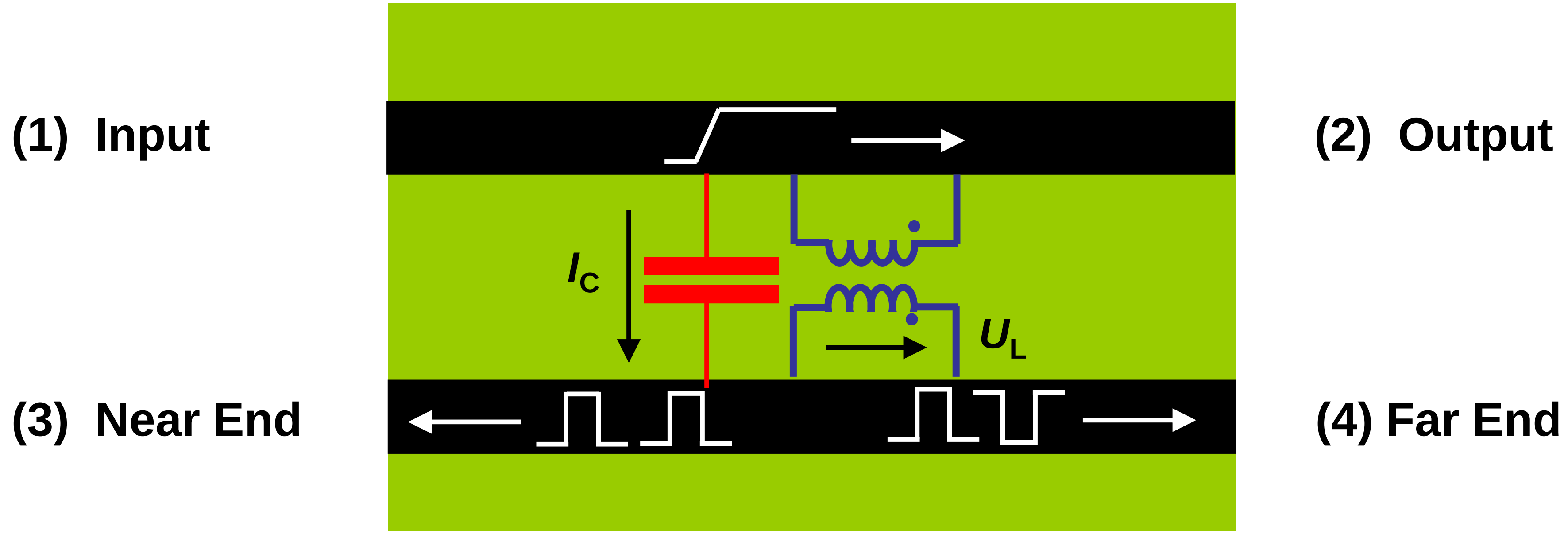
Effect of Coupling

Consider two transmission lines in close proximity:



Effect of Coupling

Consider two transmission lines in close proximity:



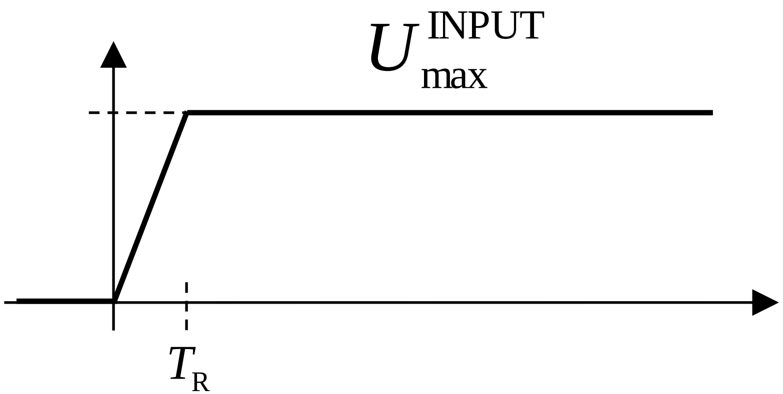
NEXT =
Near End Crosstalk
(sum of ind. and cap. crosstalk)

FEXT =
Far End Crosstalk
(difference of ind. and cap. crosstalk)

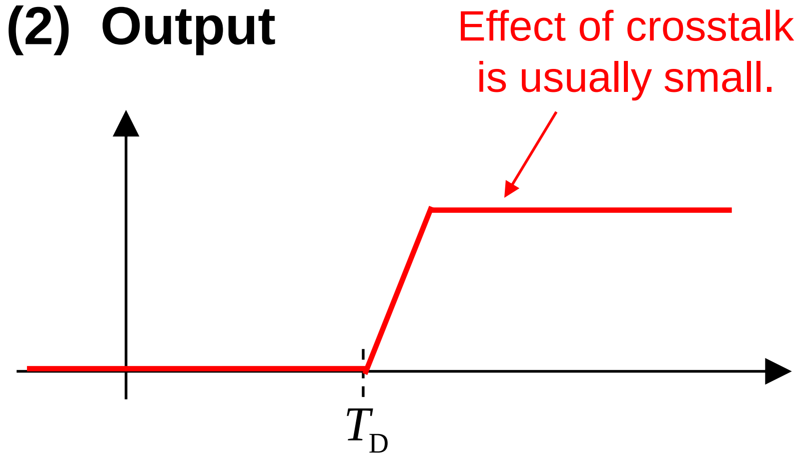
Effect of Coupling

For <u>weak coupling</u> ($k_{L,C} \le 0.25$) it is found approximatively:

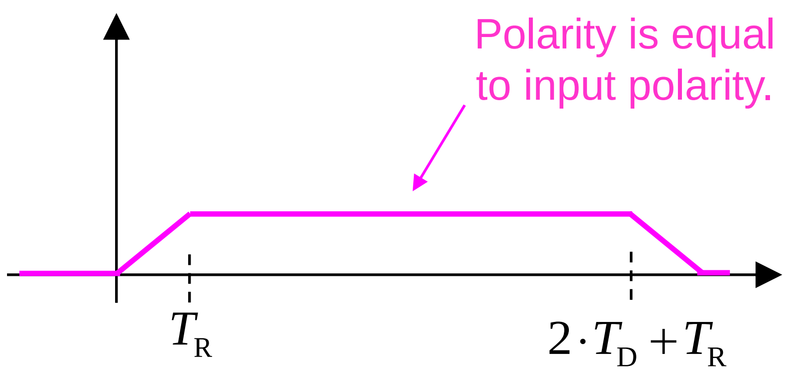
(1) Input



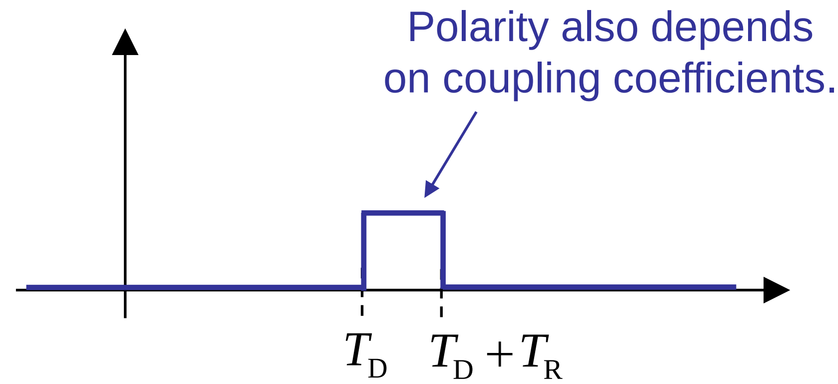
(2) Output



(3) Near End



(4) Far End



Effect of Coupling

For <u>weak coupling</u> ($k_{L,C} \leq 0.25$) it is found approximatively:

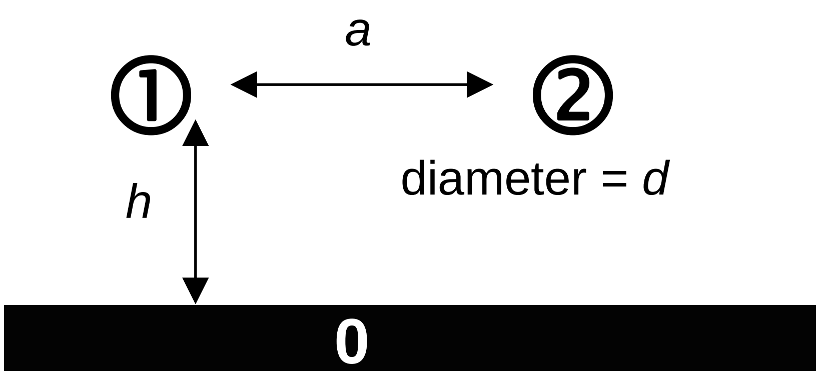
$$U_{\max}^{\text{NEXT}} = \begin{cases} \dfrac{k_C + k_L}{2} \cdot \dfrac{T_D}{T_R} \cdot U_{\max}^{\text{INPUT}} & (T_D < 0.5 \cdot T_R) \\ \dfrac{k_C + k_L}{4} \cdot U_{\max}^{\text{INPUT}} & (T_D > 0.5 \cdot T_R) \end{cases}$$

$$U_{\max}^{\text{FEXT}} = \frac{k_C - k_L}{2} \cdot \frac{T_D}{T_R} \cdot U_{\max}^{\text{INPUT}}$$

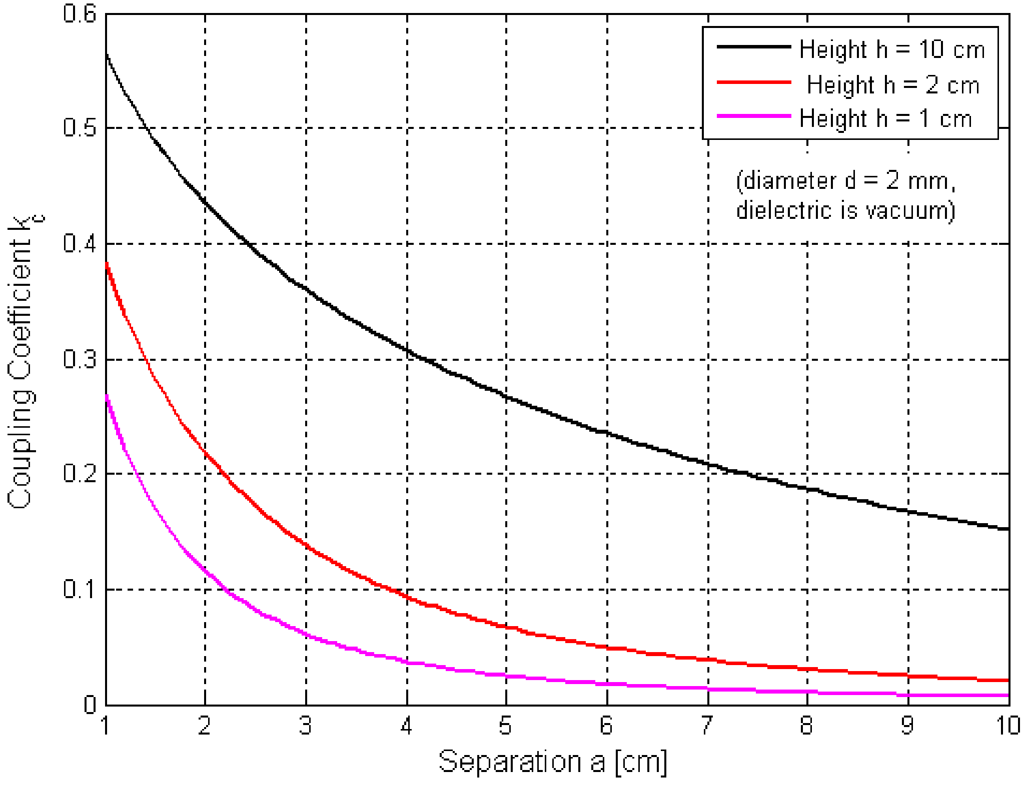
It should be noted that these formulas do not take into account losses on the lines or reflections from load mismatches.

Example for Coupling Coefficients

For two thin wires above infinite ground one can find:



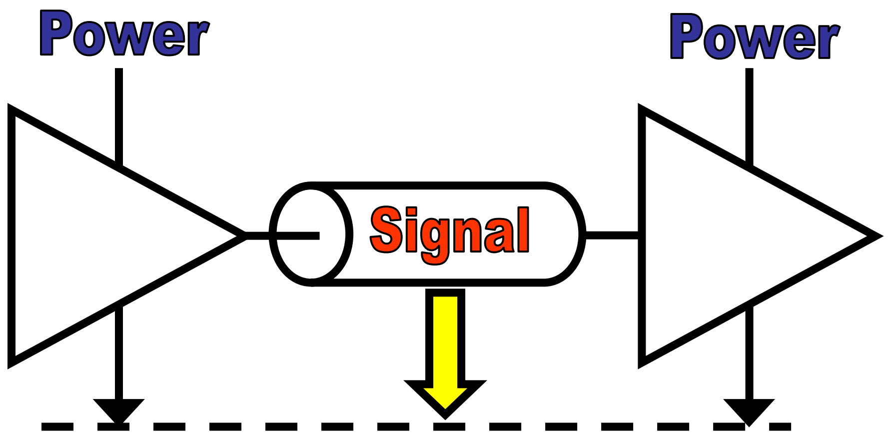
$$k_C = \frac{C'_{12}}{C'_{11} + C'_{12}} \approx \frac{\ln(1+(2h/a)^2)}{2 \cdot \ln(4h/d)}$$



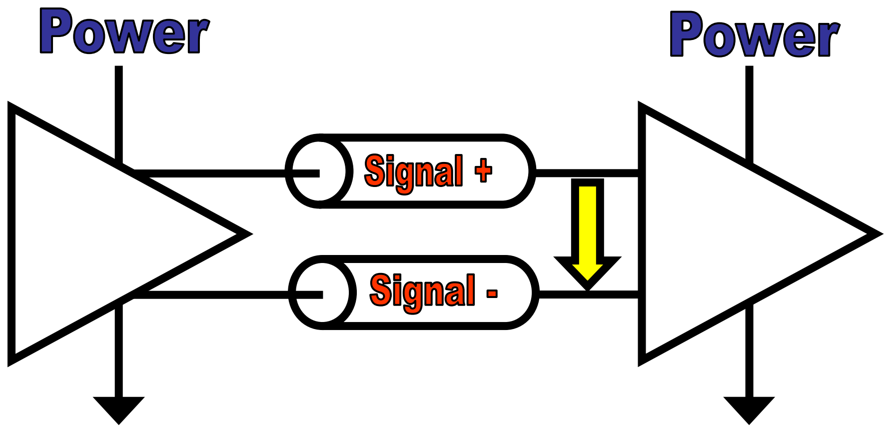
Reducing Coupling

- ➔ Increase line separation!
- ➔ Decrease distance to ground!
- ➔ Balance capacitive and inductive coupling!
- ➔ Increase rise time!
- ➔ Reduce coupling length!
- ➔ Use differential signaling!

Differential Signaling



In a **SINGLE-ENDED** link there is a common (global) reference against which the signal is measured ("ground").

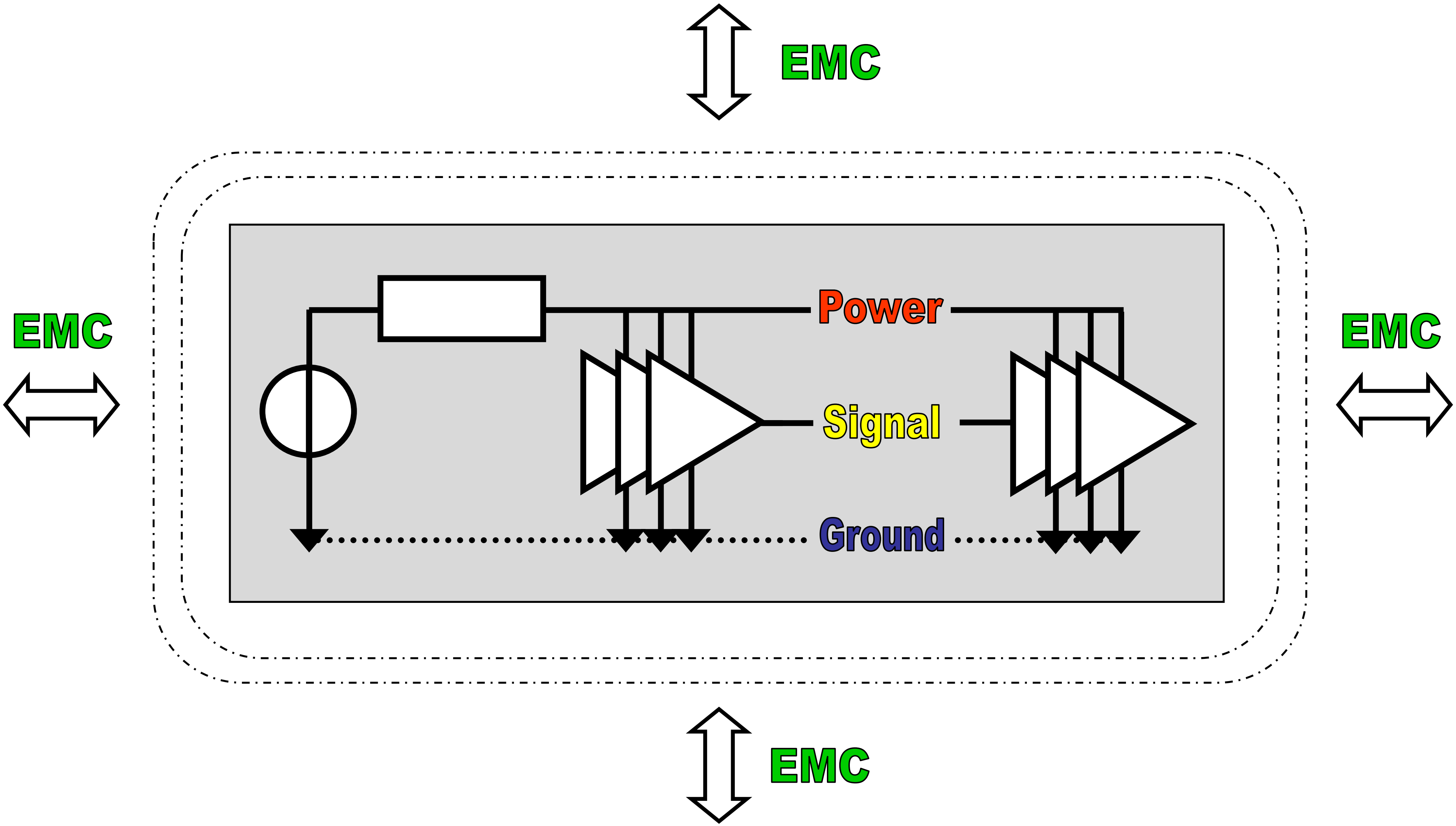


In a **DIFFERENTIAL** link the reference is the negative of the signal itself (which has to be transmitted as well).

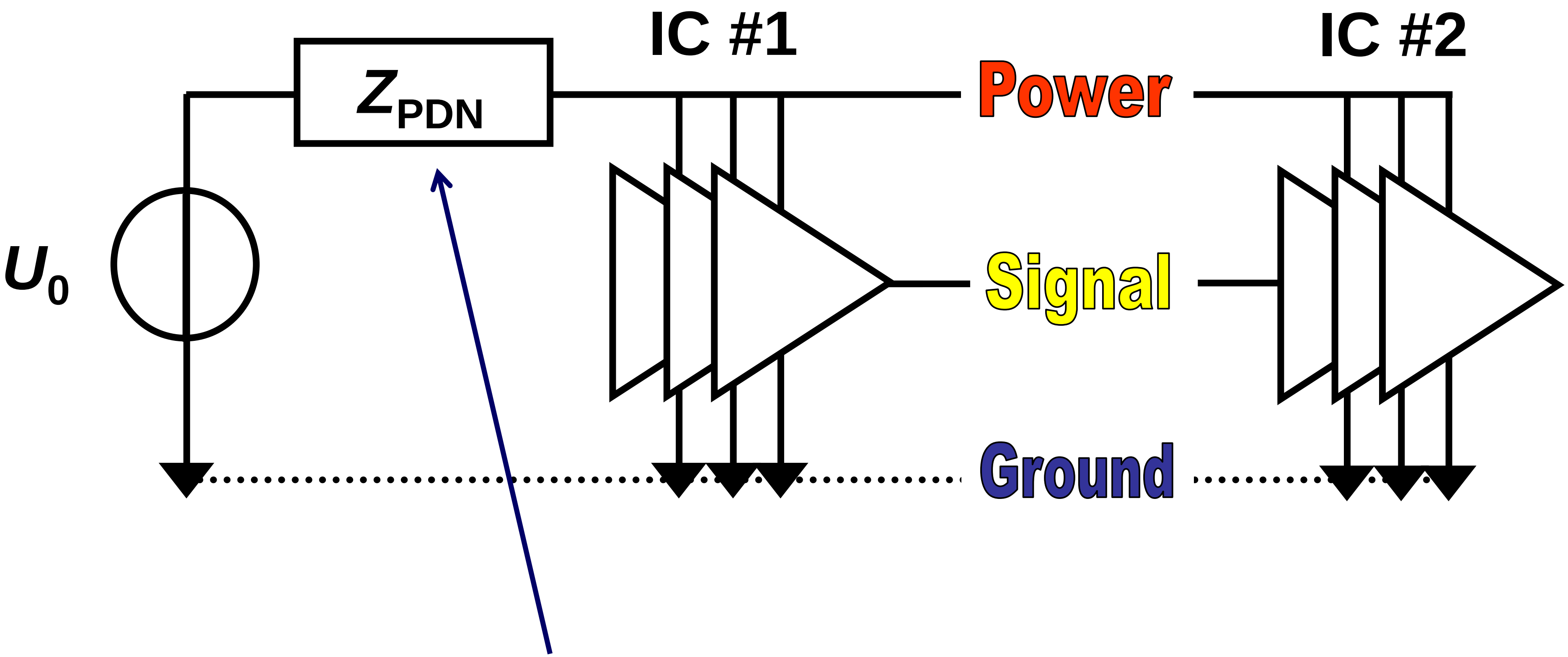
(3)

Power Integrity

Electrical Integrity of Digital Systems

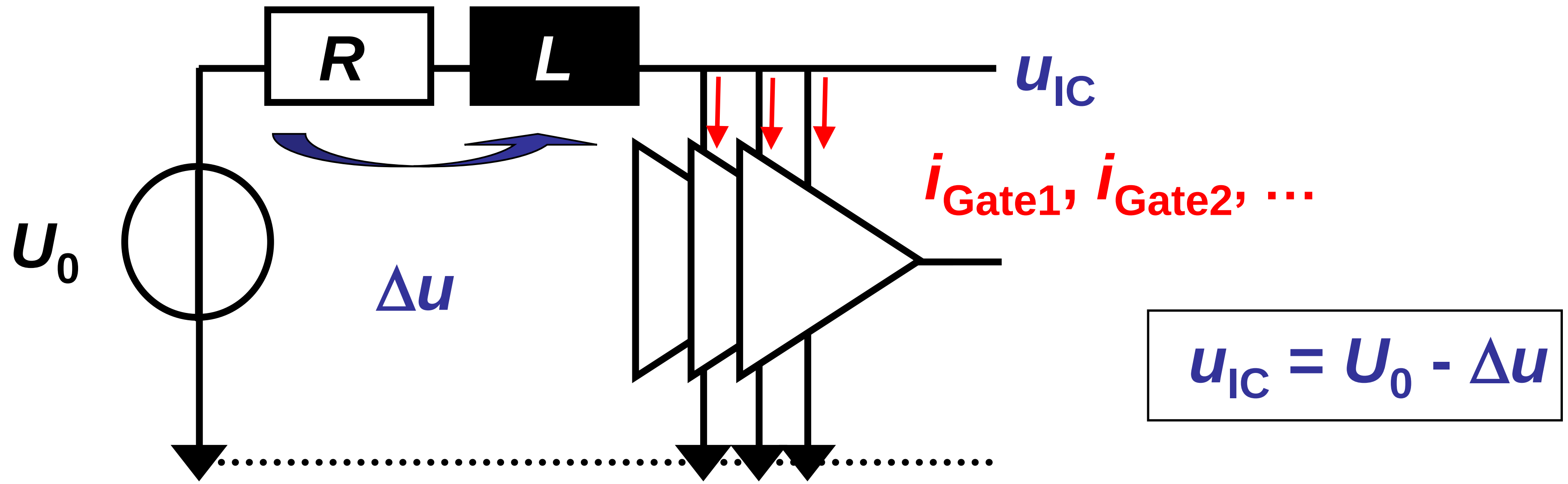


Effect of Common Power Delivery



PDN = Power Delivery Network

Effect of Common Power Delivery

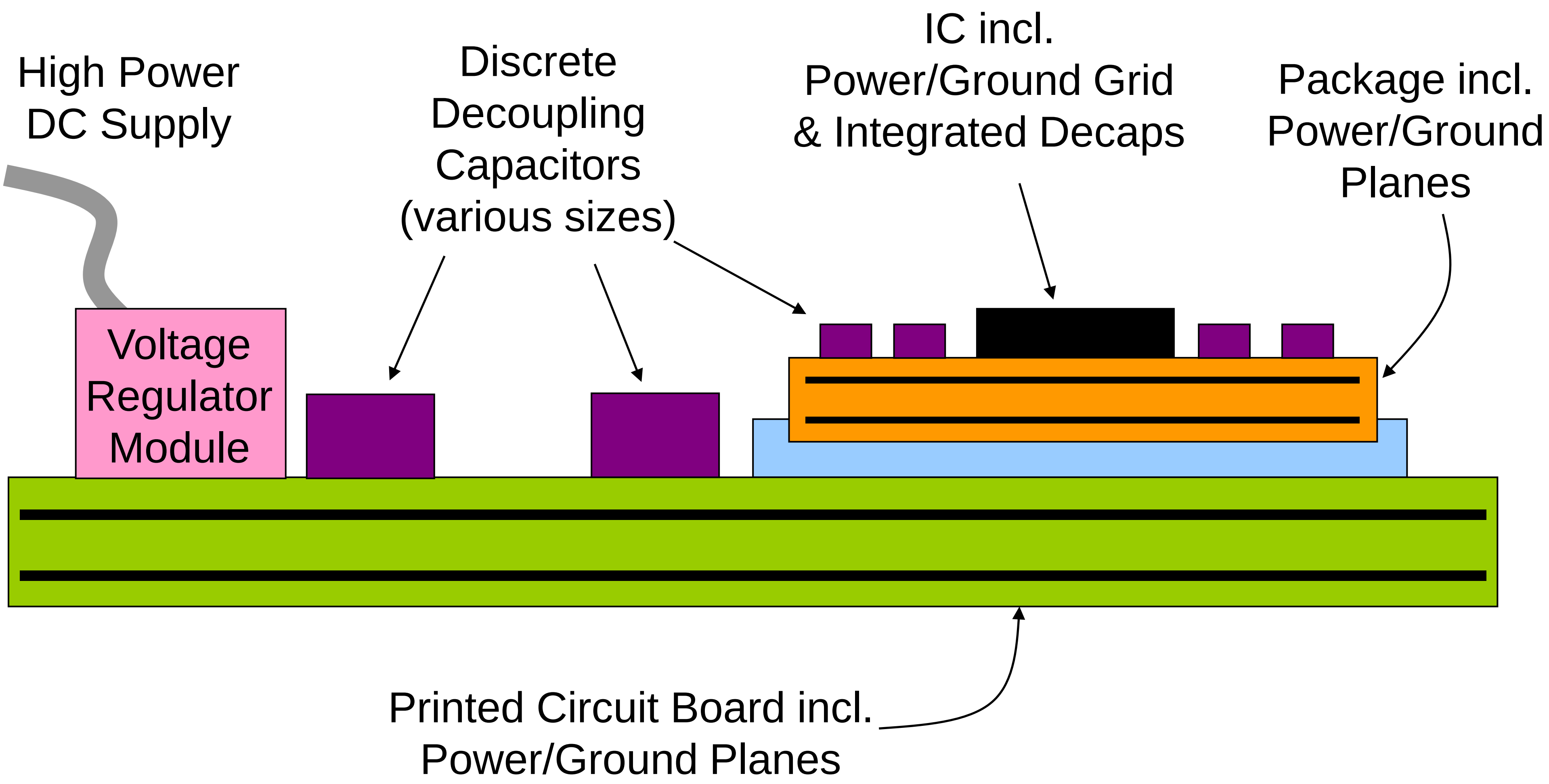


$$\Delta u(t) = \underbrace{R \cdot \left[i_{\text{Gate1}}(t) + i_{\text{Gate1}}(t) + \ldots \right]}_{\text{"DC-drop or IR-drop"}} + \underbrace{L \cdot \frac{d}{dt} \left[i_{\text{Gate1}}(t) + i_{\text{Gate1}}(t) + \ldots \right]}_{\text{"}\Delta\text{I-drop or }\Delta\text{I-noise"}}$$

Maintaining Power Integrity

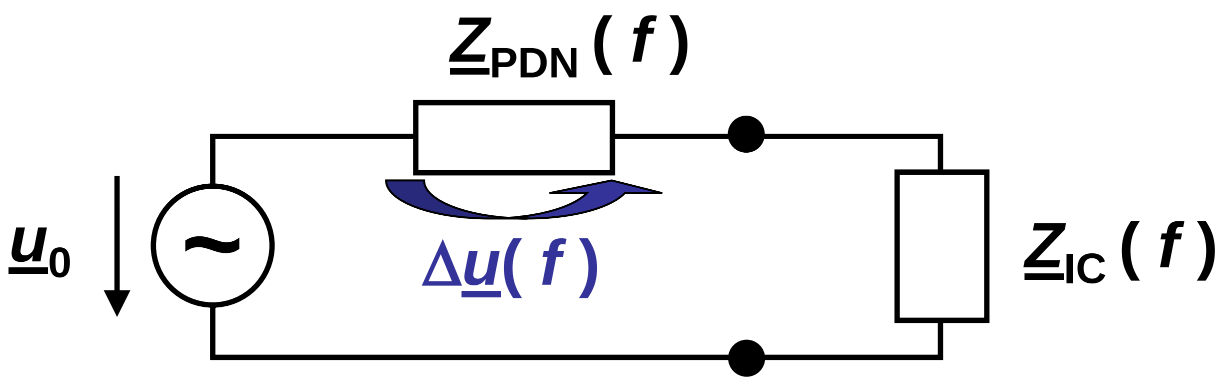
1. Decrease PDN impedance
2. Add decoupling
3. Add even more decoupling
4. Use several power supplies
5. Use on-chip VRMs

PDN Elements



PDN Impedance

In frequency domain the standard PDN model looks like this:



$$\left.\begin{aligned} \left|\Delta\underline{u}(f)\right| &\leq \Delta u_{max} \\ \left|\underline{Z}_{PDN}(f)\right| &\leq Z_{Target} \end{aligned}\right\} \quad f \in \text{"operating frequency range"}$$

PDN Impedance

A typical maximum ripple for ditigal systems is:

$$\frac{\Delta u_{\max}}{u_0} = \text{maximum ripple} \leq 5\% \text{ to } 10\%$$

With a 10% value the following numbers can be obtained for applications … of the early 1990'ies: … of 2000 and on:

… of the early 1990'ies	… of 2000 and on
$u_0 = 5.0 \text{ V}$	$u_0 = 1.2 \text{ V}$
$i_{\text{avg}} = 1 \text{A}$	$i_{\text{avg}} = 120 \text{A}$
$u_0 / i_{\text{avg}} = 5.0\ \Omega$	$u_0 / i_{\text{avg}} = 0.01\ \Omega$
$P_{\text{avg}} = 5 \text{W}$	$P_{\text{avg}} = 144 \text{W}$
➡ $Z_{\text{Target}} = 0.5 \Omega$	➡ $Z_{\text{Target}} = 0.001 \Omega$ **= 1 mΩ !**

PDN Impedance

Is **1 mΩ** hard to achieve? How about **10 mΩ**? Let's see …

Example:

The PDN consists of a simple copper wire of 2 mm radius in theform of a flat rectangle with side lengths of 5 cm and 1 cm, respectively.

$$\rightarrow \qquad \left|\underline{Z}_{\text{PDN}}\right| = \sqrt{R^2 + (\omega L)^2}$$

$$\text{with} \qquad R \approx 0.7\ \text{m}\Omega \qquad L \approx 40\ \text{nH}$$

It turns out that 10 mΩ cannot be maintained beyond **40 kHz**!

Decreasing PDN Impedance

➔ Use adequate copper cross sections!

➔ Avoid big current loops!

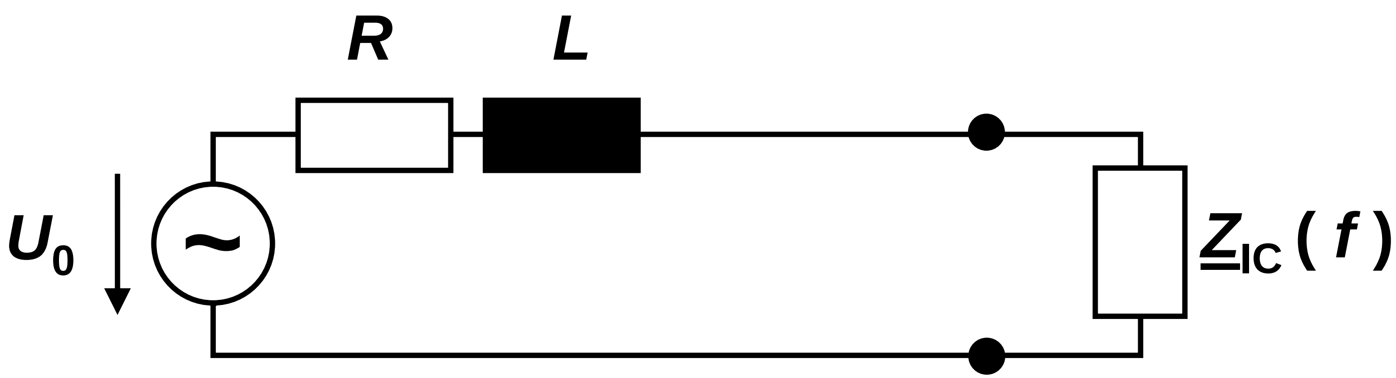
➔ Use power/ground planes!

➔ Provide enough power/ground pins!

➔ Decouple!

Decoupling

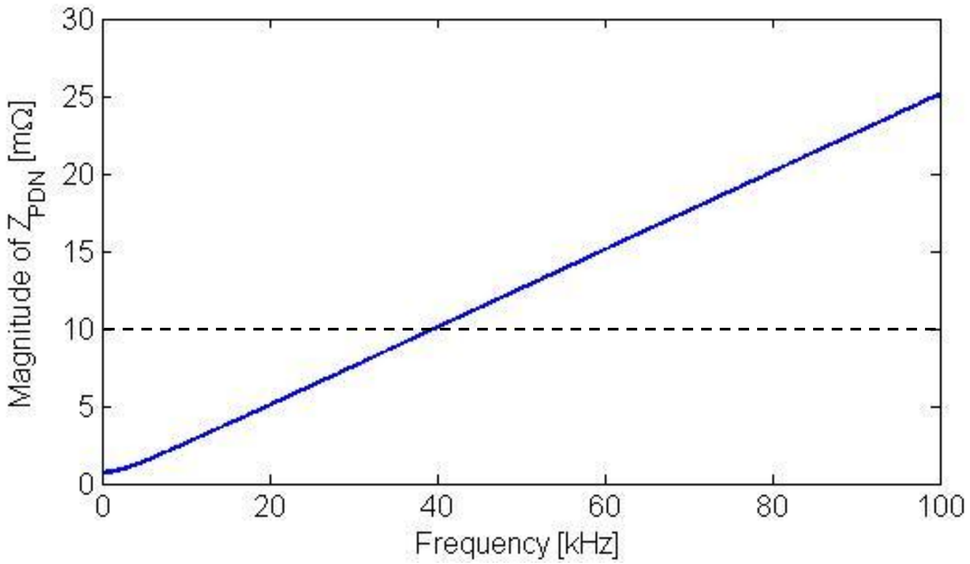
Based on the simple example from before:



$$\underline{Z}_{\text{PDN}} = R + j\omega L$$

$$\approx j\omega L$$

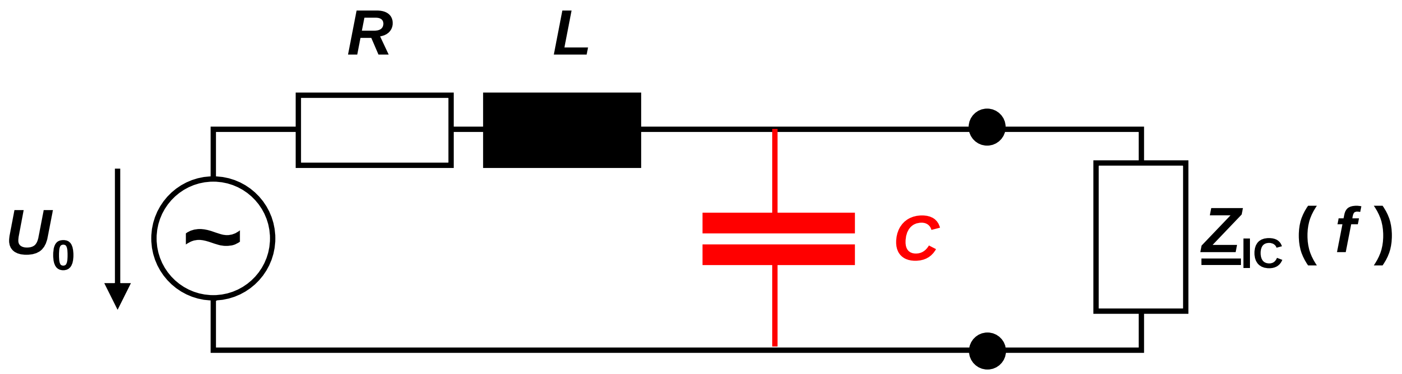
$$\text{(for large } \omega\text{)}$$



(R = 0.7 mΩ, L = 40 nH)

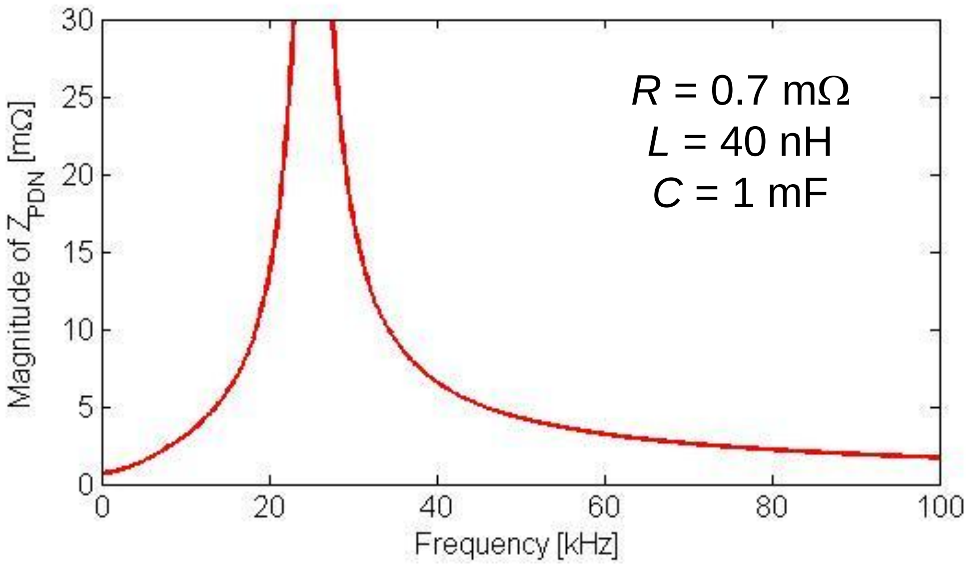
Decoupling

… we ask what a so called "decoupling" or "bypass" capacitor does:



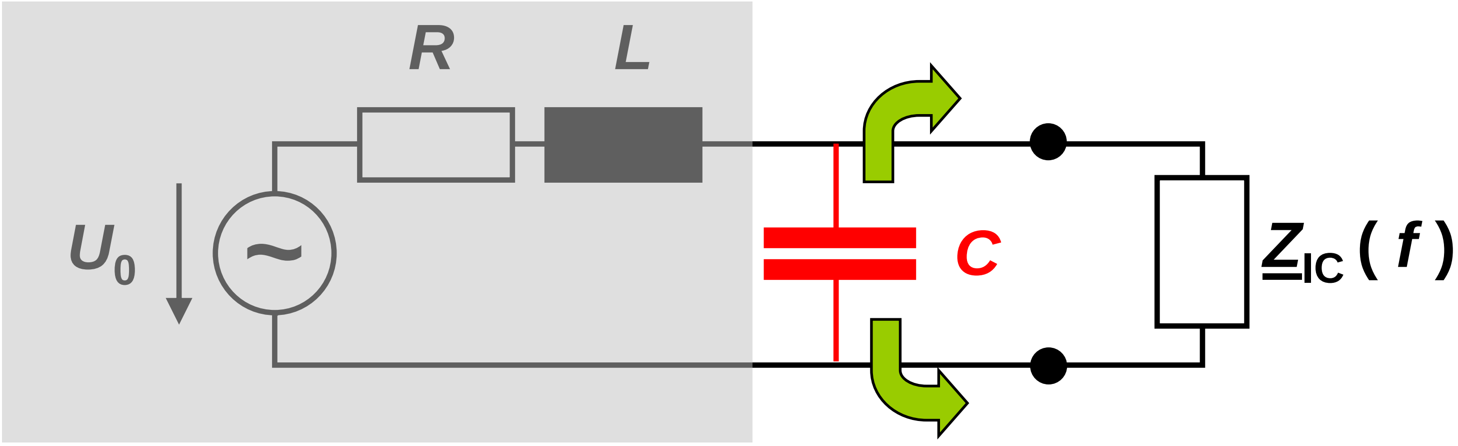
$$\underline{Z}_{\mathrm{PDN}} = \frac{R + j\omega L}{1 + j\omega RC - \omega^2 LC}$$

$$\approx \frac{1}{j\omega C} \quad \text{(for large } \omega\text{)}$$



Decoupling

Heuristic explanation:



Frequency domain: Beyond the resonance frequency the capacitor decouples the part of the PDN that lies "left" of him, i.e. the IC sees only the impedance of the capacitor.

Time domain: The capacitor stores charges close to the IC that can become currents needed for fast switching. It is like a "small battery".

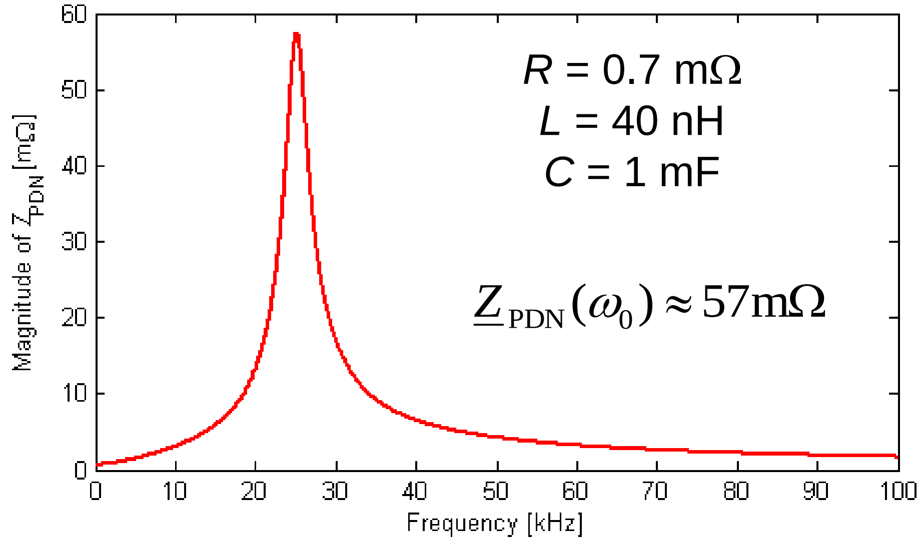
Decoupling

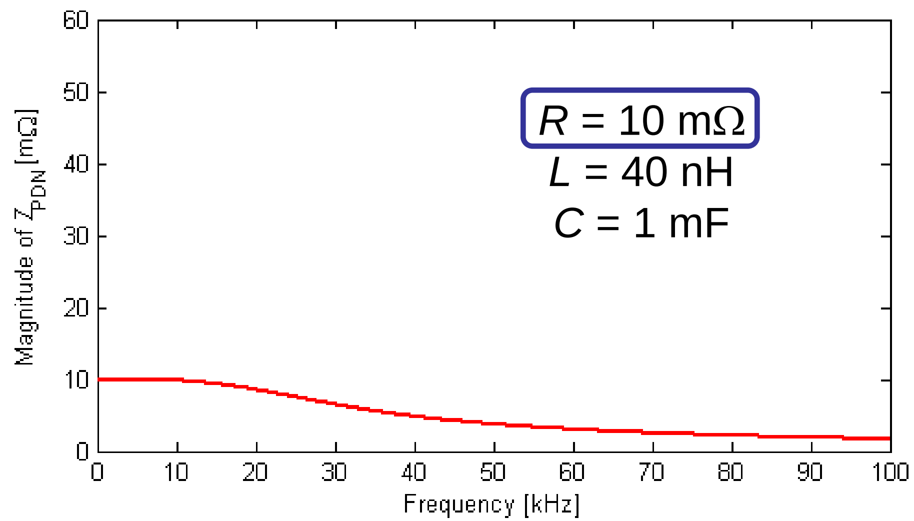
While being beneficial at higher frequencies decoupling increases the PDN impedance in the vicinity of the resonance frequency:

$$\omega_0 = \frac{1}{L} \cdot \sqrt{\frac{L}{C} - R^2} \qquad (L/C \geq R^2)^*$$

$$\rightarrow \qquad \underline{Z}_{\mathrm{PDN}}(\omega_0) = \frac{1}{R} \cdot \frac{L}{C} \geq R$$

Hence, increasing the "damping" (by increasing *R* and/or reducing *L*/*C*) can be helpful:



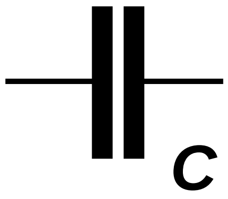


(with $Q = 1/R \cdot \sqrt{L/C}$ the condition becomes $Q \geq 1)^*$

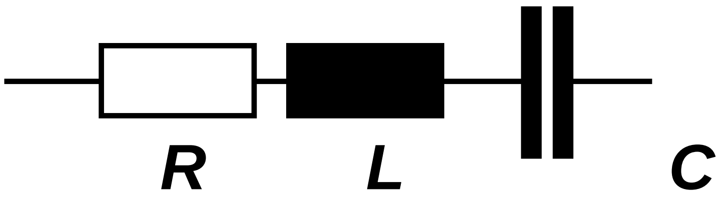
Real Word Decoupling Capacitors

Unfortunately, there is no ideal capacitor available in the real world!

Ideal world:



… and real world:

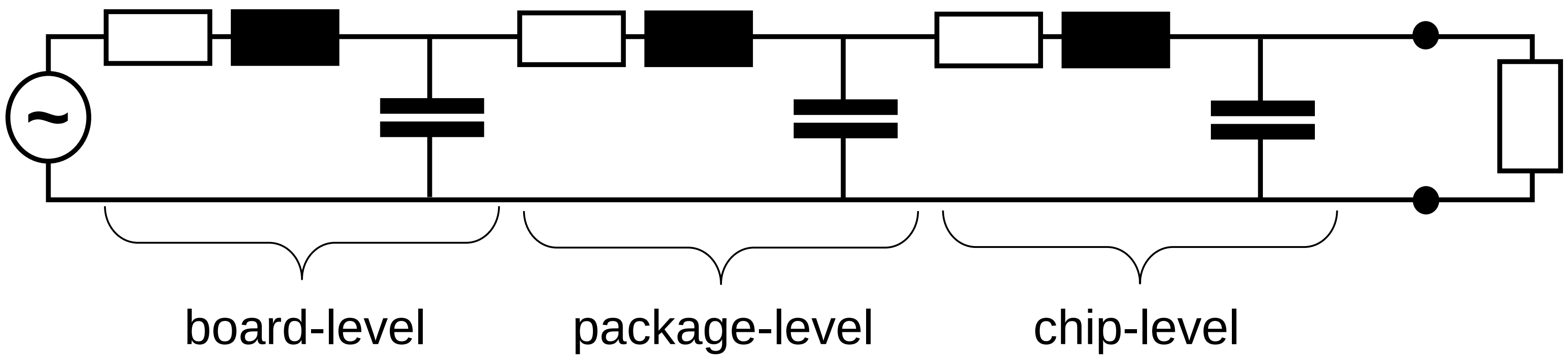


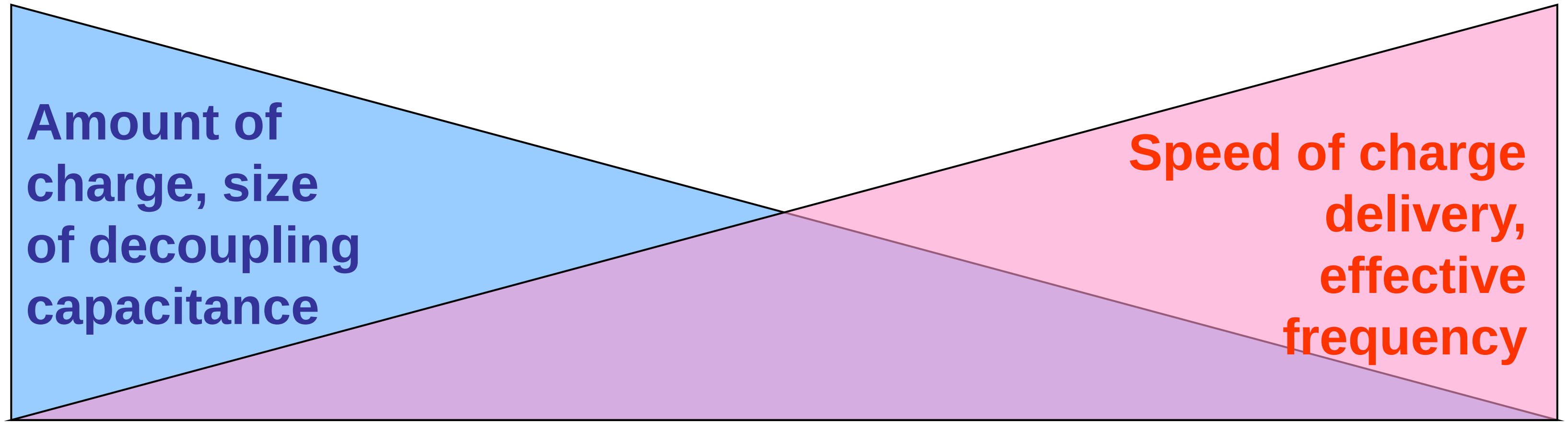
R is also is called the **EQUIVALENT SERIES RESISTANCE (ESR)** and *L* the **EQUIVALENT SERIES INDUCTANCE (ESL)**.

As a consequence any real world capacitor behaves approximately like an inductor beyond its resonance frequency:

$$\omega_0 = 1/\sqrt{LC}$$

More Decoupling





Power/Ground Planes

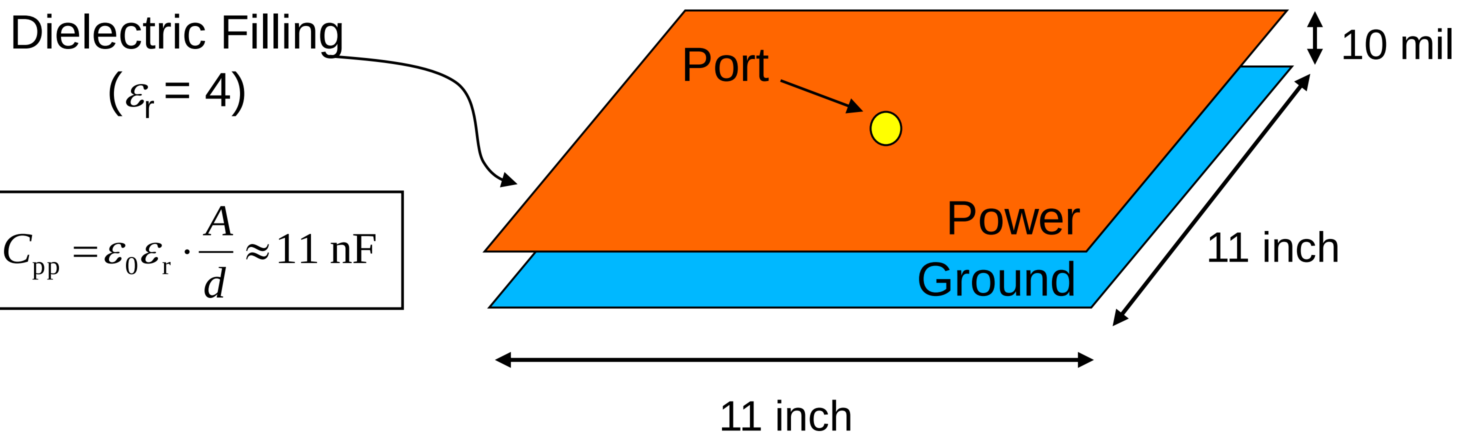
Power/ground planes serve multiple purposes at the same time:

- ➔ easy access to power and ground domains for mounted components
- ➔ a "natural" decoupling capacitor for PDN improvement
- ➔ return current paths, i.e. they serve as reference conductors
- ➔ shielding between different signal layers, i.e. they reduce crosstalk
- ➔ containment for internal EM fields, i.e. reduce EM emission

… HOWEVER …

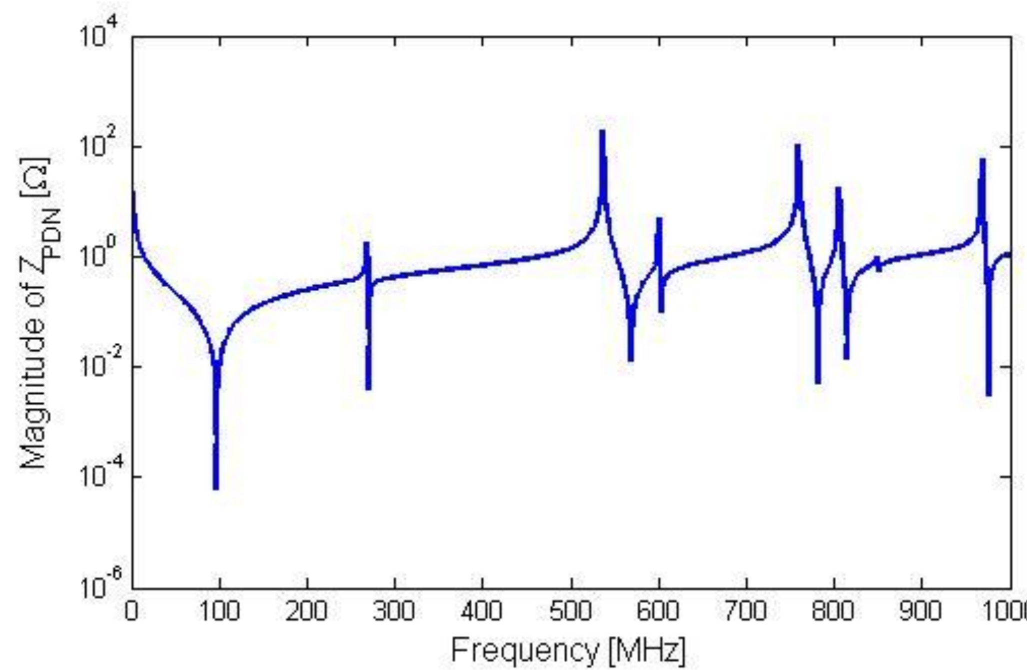
Power/Ground Planes

… they do show a resonant behavior:



$$C_{pp} = \varepsilon_0 \varepsilon_r \cdot \frac{A}{d} \approx 11\ \text{nF}$$

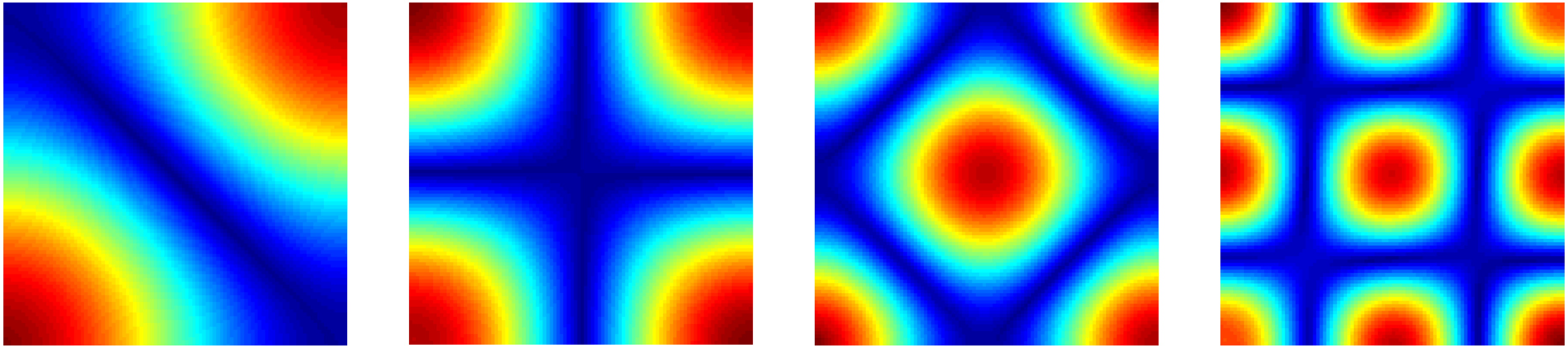
(1 inch = 2.54 cm,
1 mil = 0.001 inch)



Power/Ground Planes

The resonance frequencies are given by:

$$f_{mn} = \frac{c_0}{\sqrt{\mu_r \varepsilon_r}} \sqrt{\left(\frac{m}{2a}\right)^2 + \left(\frac{n}{2b}\right)^2} \qquad (m, n = 0, 1, 2, \ldots)$$



Examples of standing wave patterns on a rectangular power/ground plane pair.

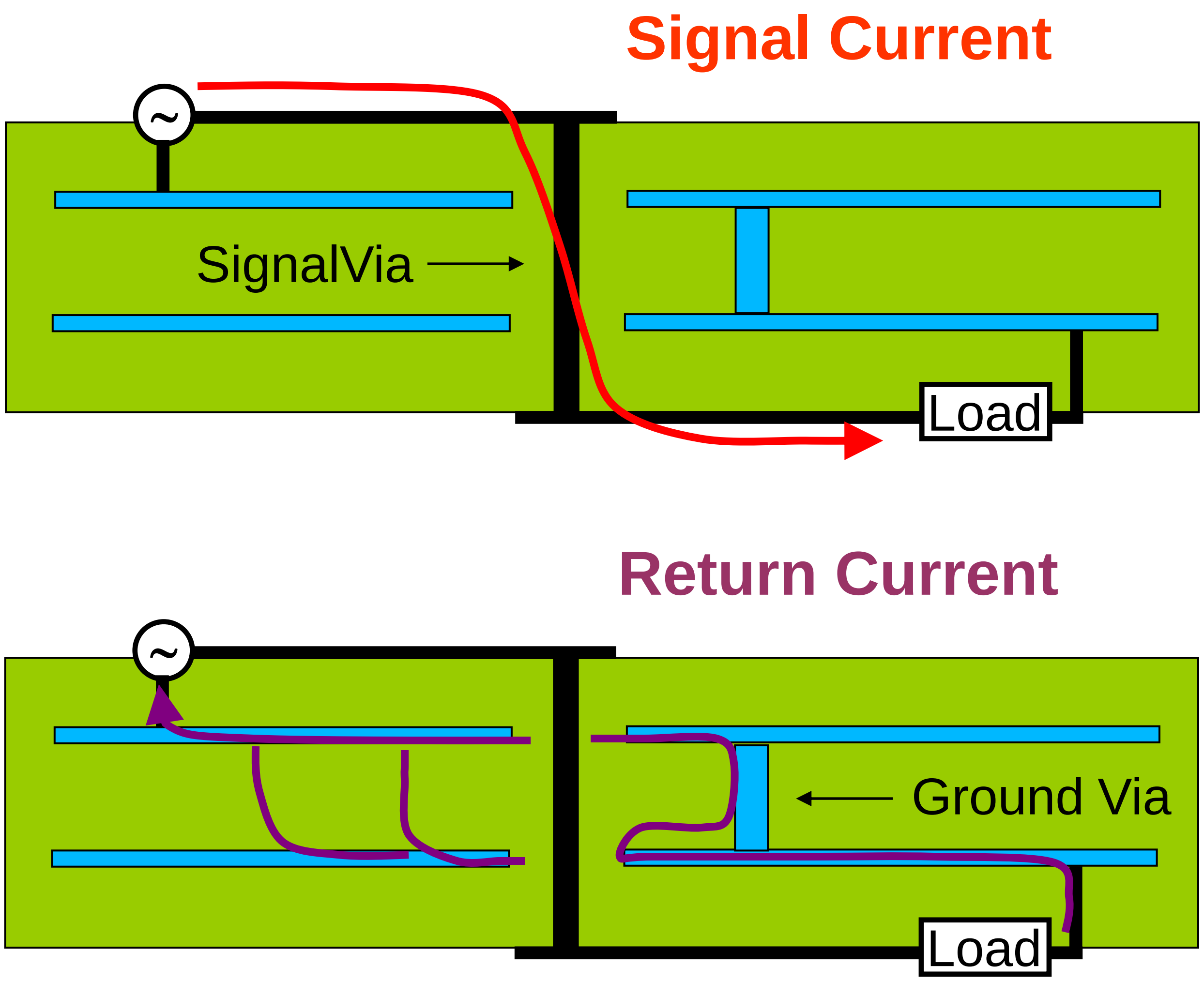
Adding Decoupling

- ➔ Determine your target impedance!
- ➔ Determine your operating frequency range!
- ➔ Provide decoupling at all levels/frequencies!
- ➔ Use parallel decoupling to reduce ESR/ESL!
- ➔ Be wary of resonances!

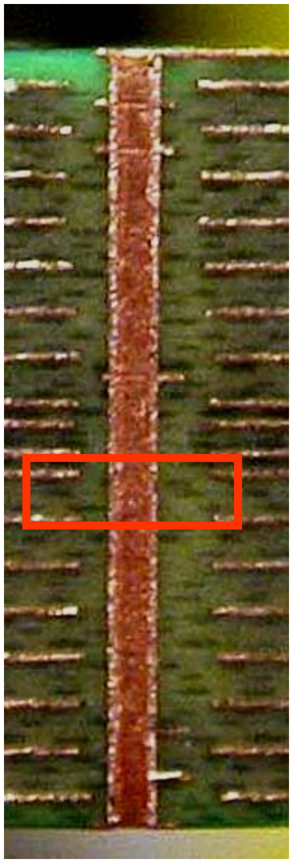
(4)

Vias and Return Currents

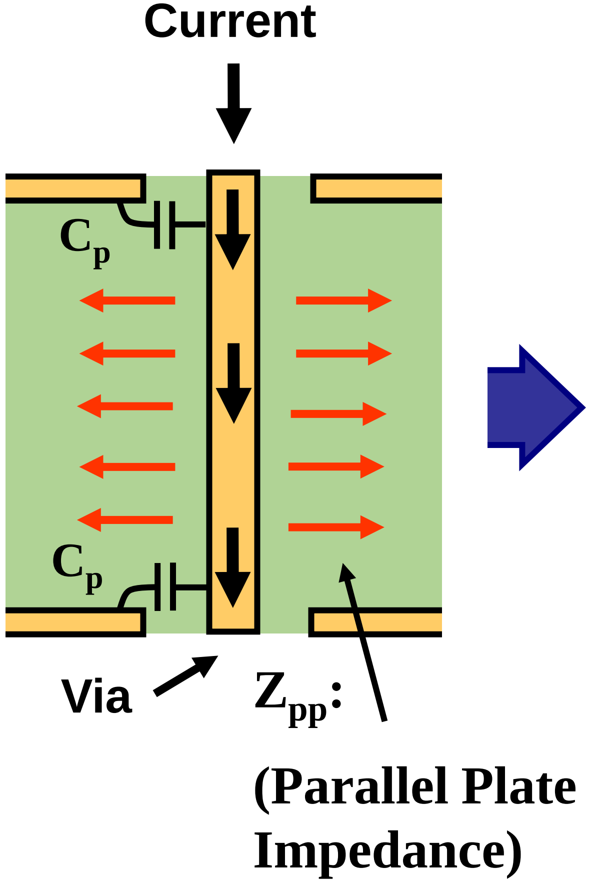
The Problem With Vias

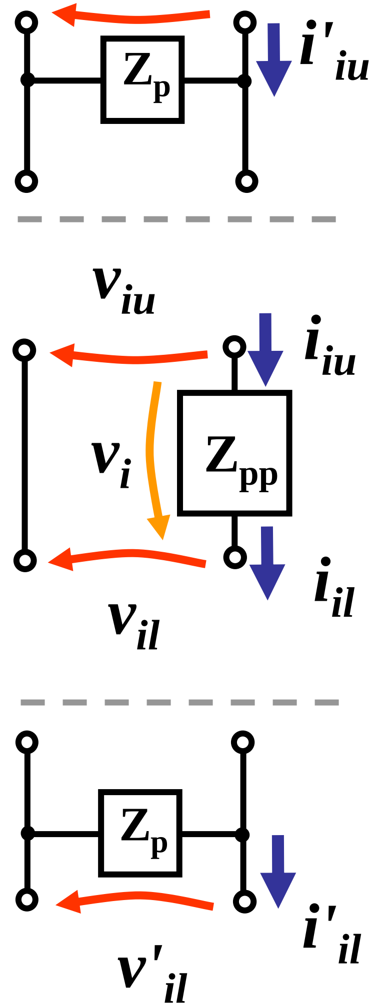


A “Physcis-Based” Model for Vias



Via Cross Section



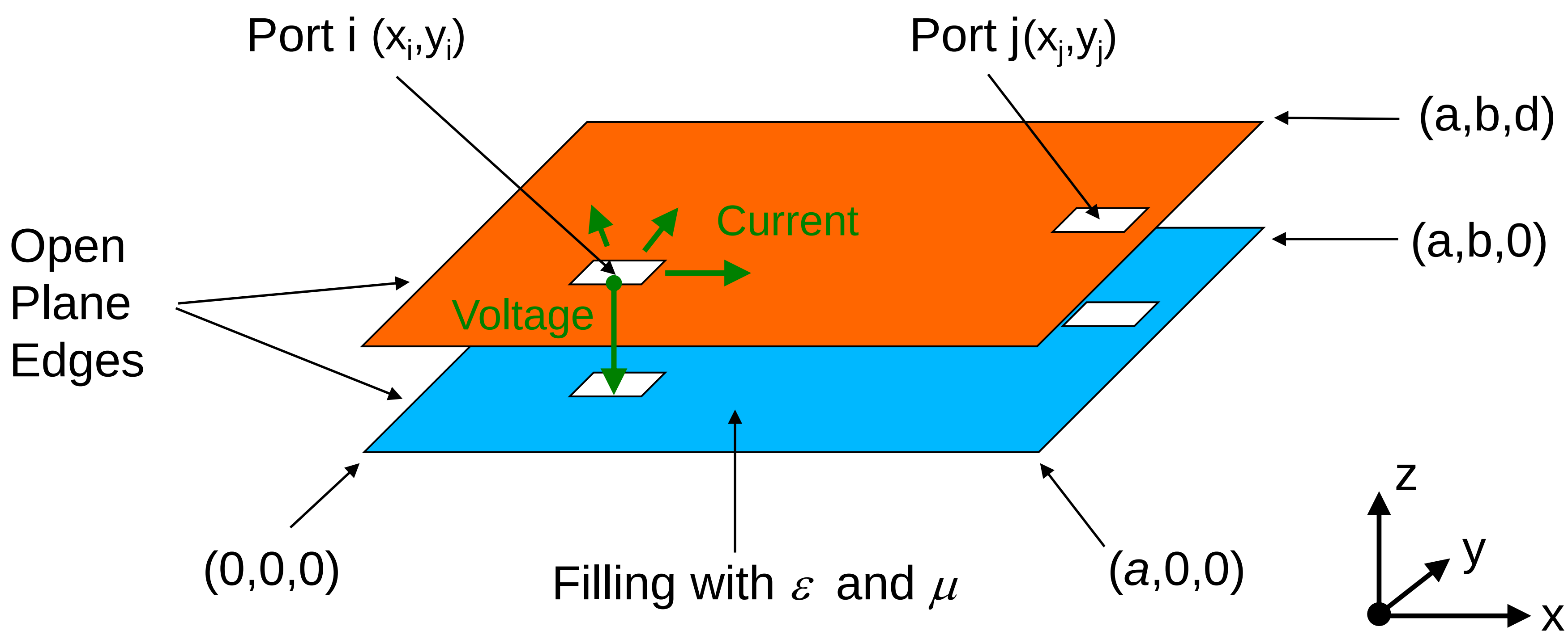


$$\begin{bmatrix} v'_{i_u} \\ i'_{i_u} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/Z_{p_u} & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{i_u} \\ i_{i_u} \end{bmatrix}$$

$$\begin{bmatrix} v_{i_u} \\ i_{i_u} \end{bmatrix} = \begin{bmatrix} 1 & Z_{pp} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{i_l} \\ i_{i_l} \end{bmatrix}$$

$$\begin{bmatrix} v_{i_l} \\ i_{i_l} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/Z_{p_l} & 1 \end{bmatrix} \cdot \begin{bmatrix} v'_{i_l} \\ i'_{i_l} \end{bmatrix}$$

Where Do We Zpp Get From?

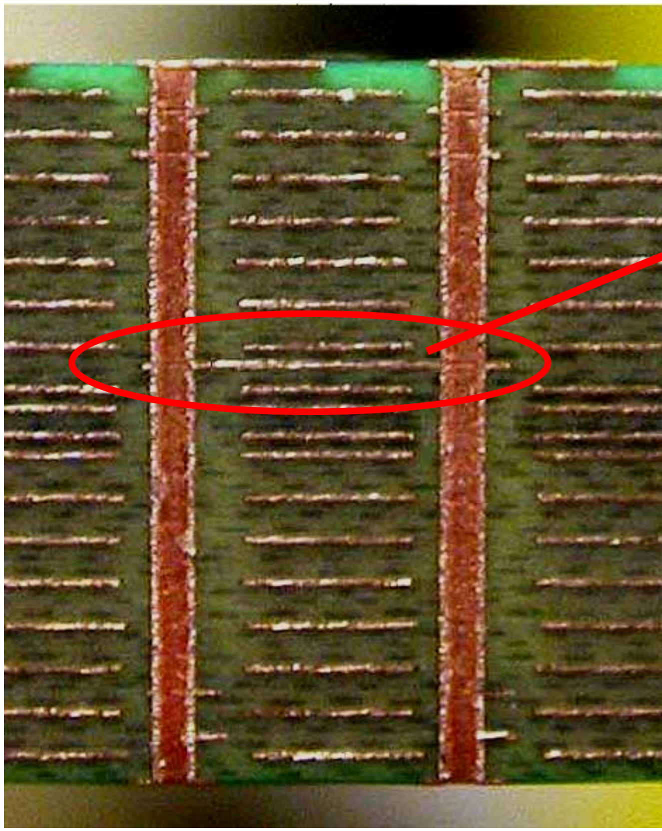


$$\underline{Z}_{ij}(\omega) = \frac{j\omega\mu d}{ab} \cdot \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[C_m^2 C_n^2 \cdot \frac{\cos(k_{xm}x_i)\cdot\cos(k_{yn}y_i)\cdot\cos(k_{xm}x_j)\cdot\cos(k_{yn}y_j)}{k_{xm}^2 + k_{yn}^2 - k^2} \right]$$

$$k_{xm} = \frac{m\pi}{a} \qquad k_{yn} = \frac{n\pi}{b} \qquad k = \omega\cdot\sqrt{\mu\varepsilon}$$

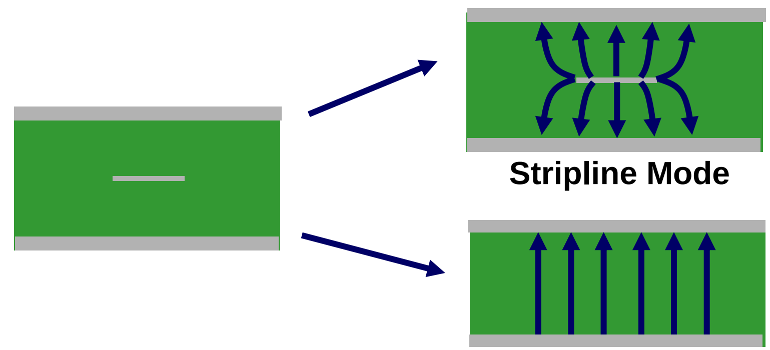
$$C_m, C_n = 1 \text{ for } m,n = 0 \text{ and } \sqrt{2} \text{ otherwise}$$

Including Striplines



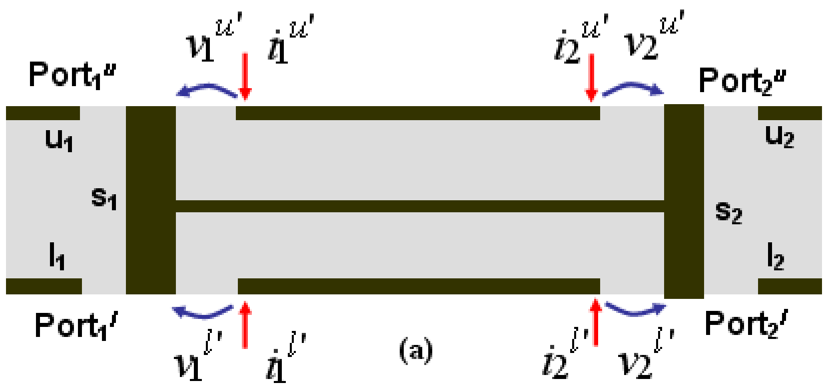
Trace between planes:

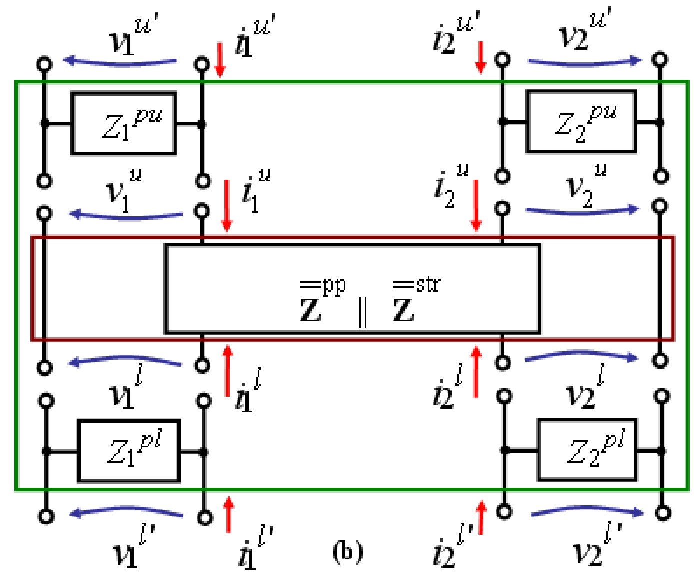
2 Modes: Stripline + Parallel Plate

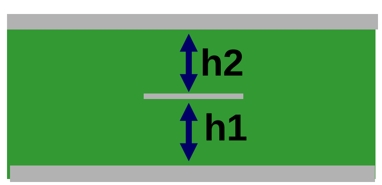


Modal decomposition: find suitable transformation matrices to diagonalize MTL equations

Including Striplines





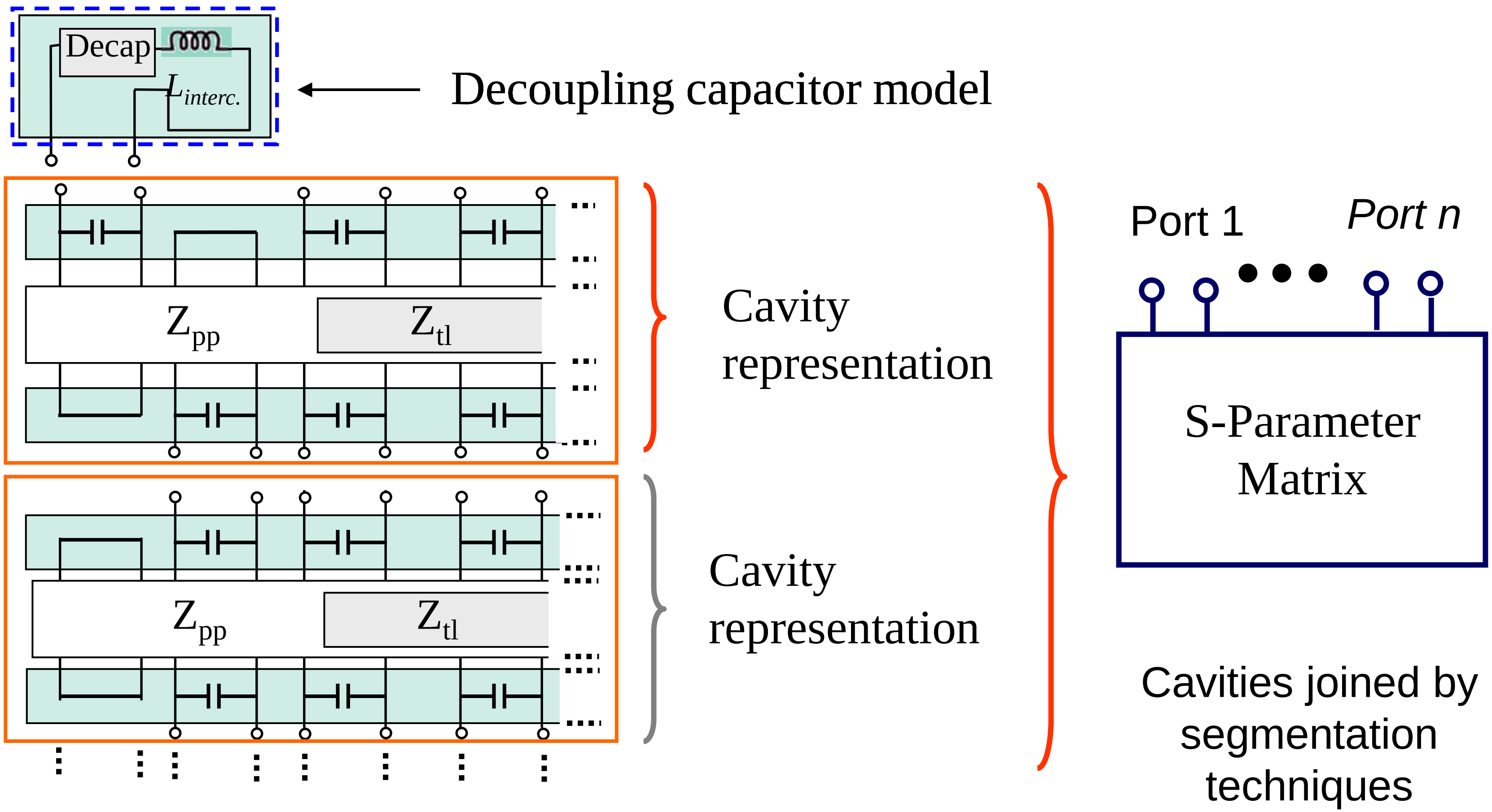


$$k \approx -\frac{h_1}{h_1 + h_2}$$

$$\begin{pmatrix} I_{ps1} \\ I_{ps2} \\ I_{gs1} \\ I_{gs2} \end{pmatrix} = \begin{pmatrix} k^2 \overline{\overline{Y}}_{stripline} + \overline{\overline{Y}}_{pp} & (-k^2 - k)\overline{\overline{Y}}_{stripline} - \overline{\overline{Y}}_{pp} \\ (-k^2 - k)\overline{\overline{Y}}_{stripline} - \overline{\overline{Y}}_{pp} & (k^2 + 2k + 1)\overline{\overline{Y}}_{stripline} + \overline{\overline{Y}}_{pp} \end{pmatrix} \cdot \begin{pmatrix} V_{ps1} \\ V_{ps2} \\ V_{gs1} \\ V_{gs2} \end{pmatrix}$$

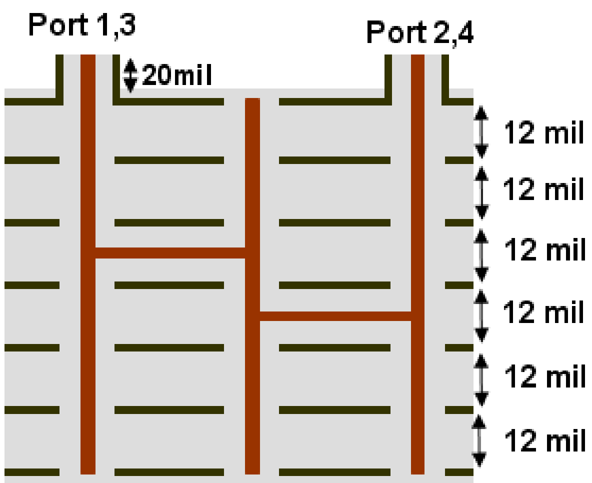
R. Rimolo-Donadio, H. D. Brüns, C. Schuster, "**Including Stripline Connections into Network Parameter Based Via Models for Fast Simulation of Interconnects,"** International Zurich Symposium on Electromagnetic Compatibility, Switzerland, Jan. 12-15, 2009

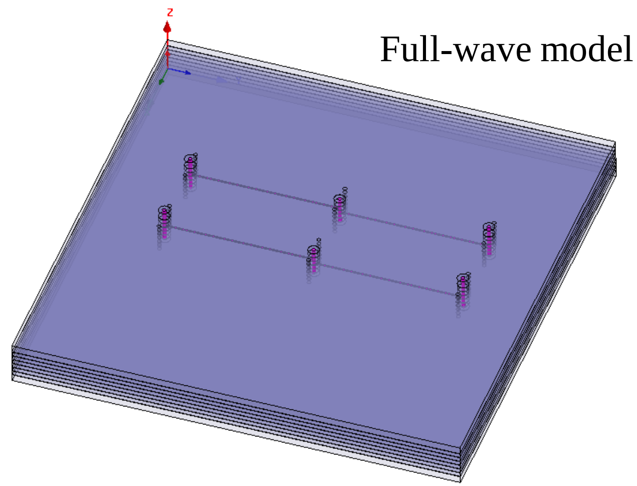
Stacking the Deck



R. Rimolo-Donadio et al., "**Physics-based via and trace models for efficient link simulation on multilayer structures up to 40 GHz"**, *IEEE Trans. Microw. Theory and Techn.*, vol. 57, no. 8, p.p. 2072-2083, August 2009.

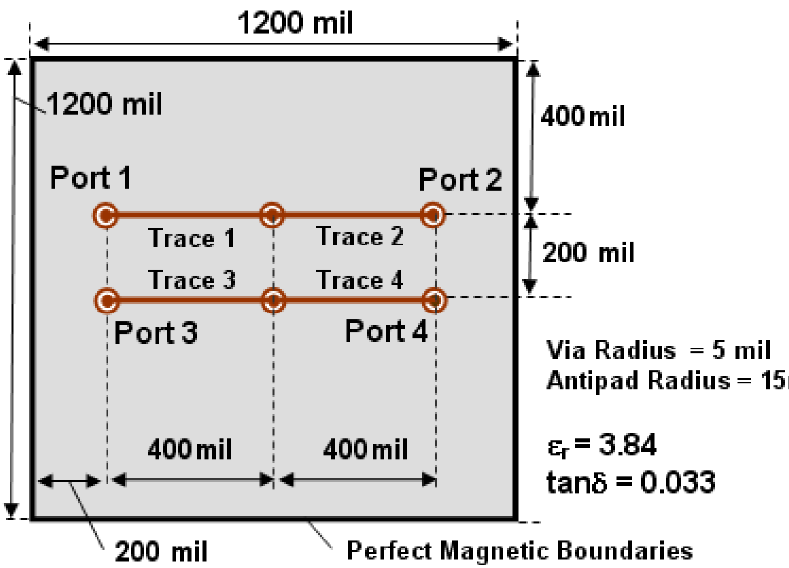
Comparison with Full-Wave Results

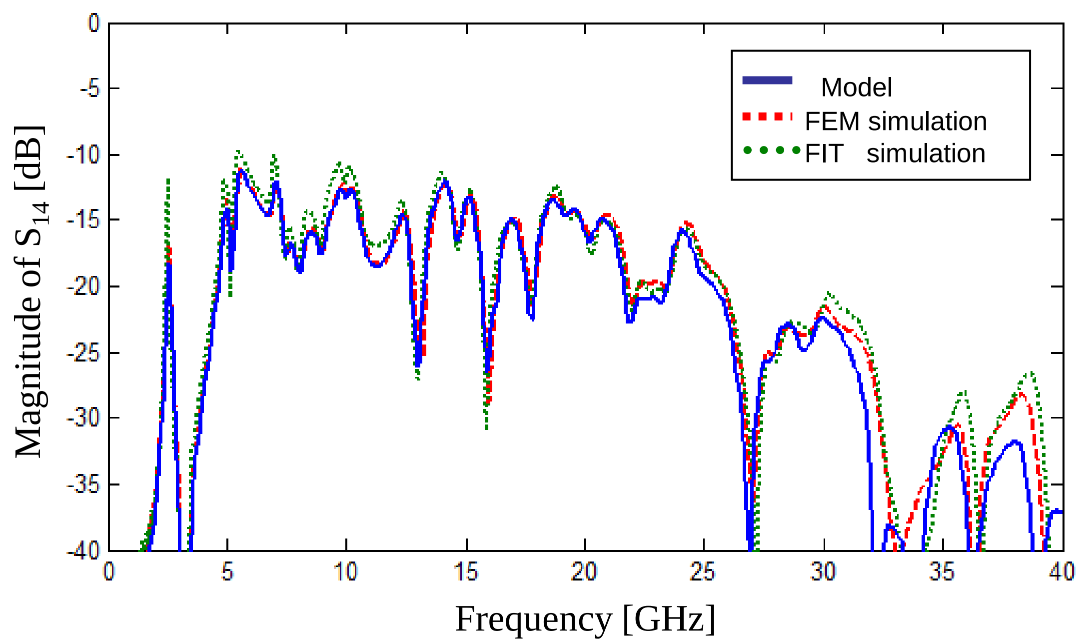




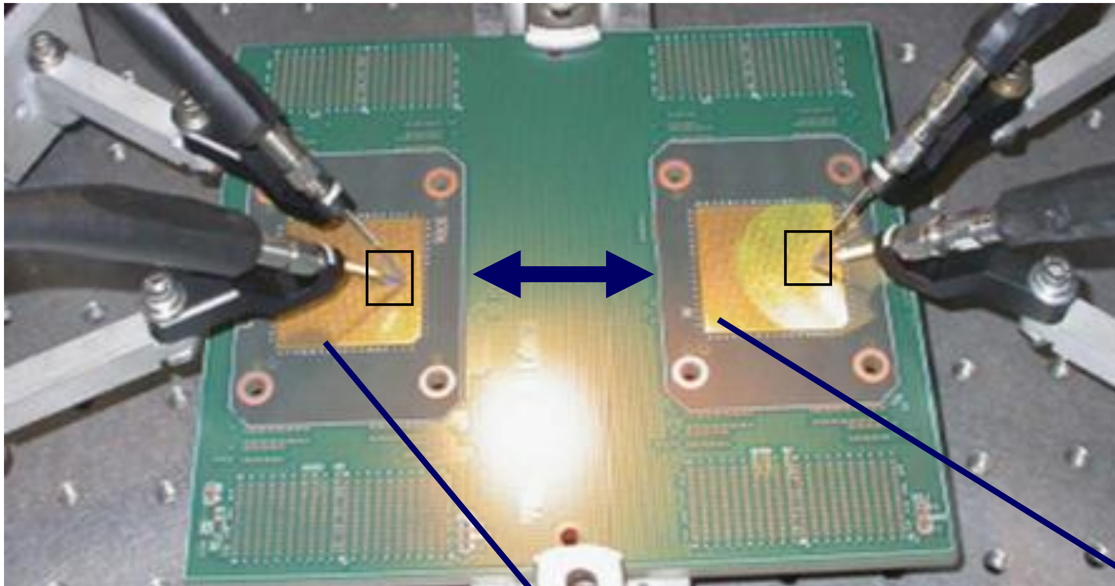
6 Vias, 4 traces case

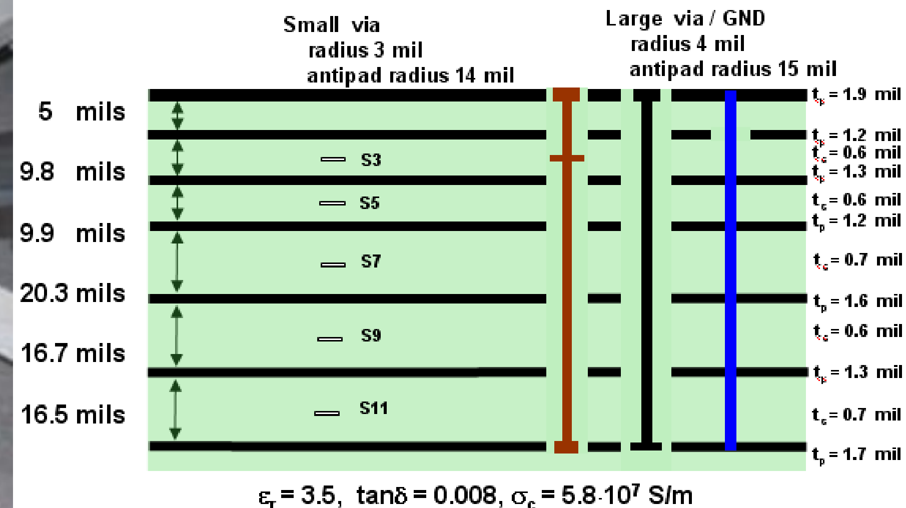
Centered striplines at two levels, and thru vias in a 6 cavity stackup



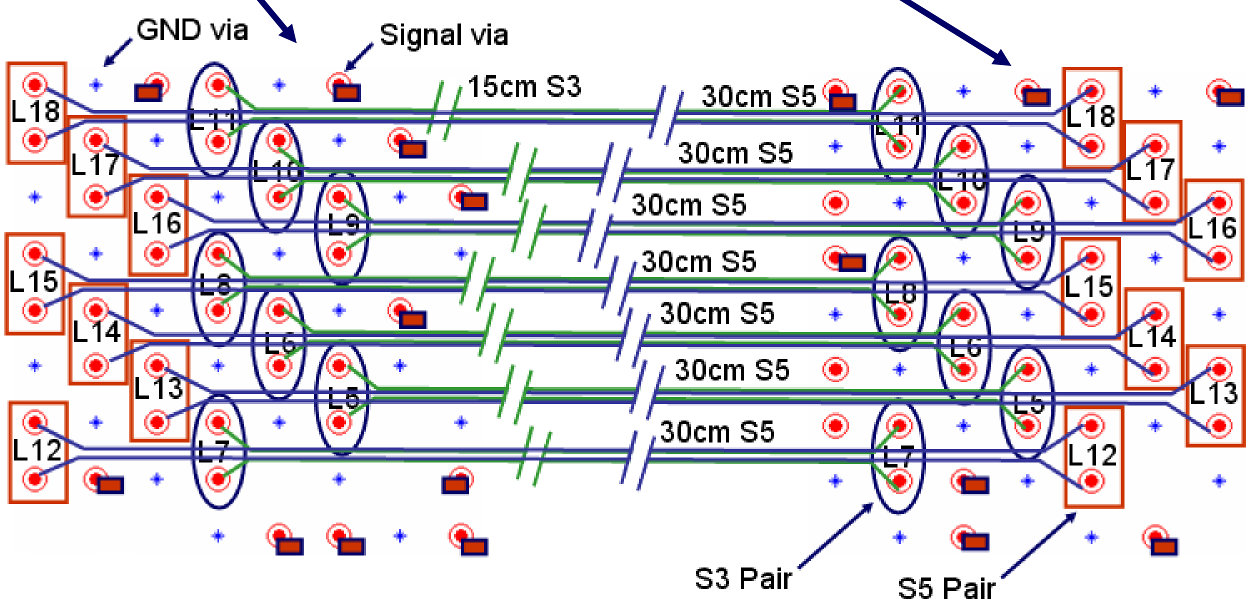


Comparison with Measurements





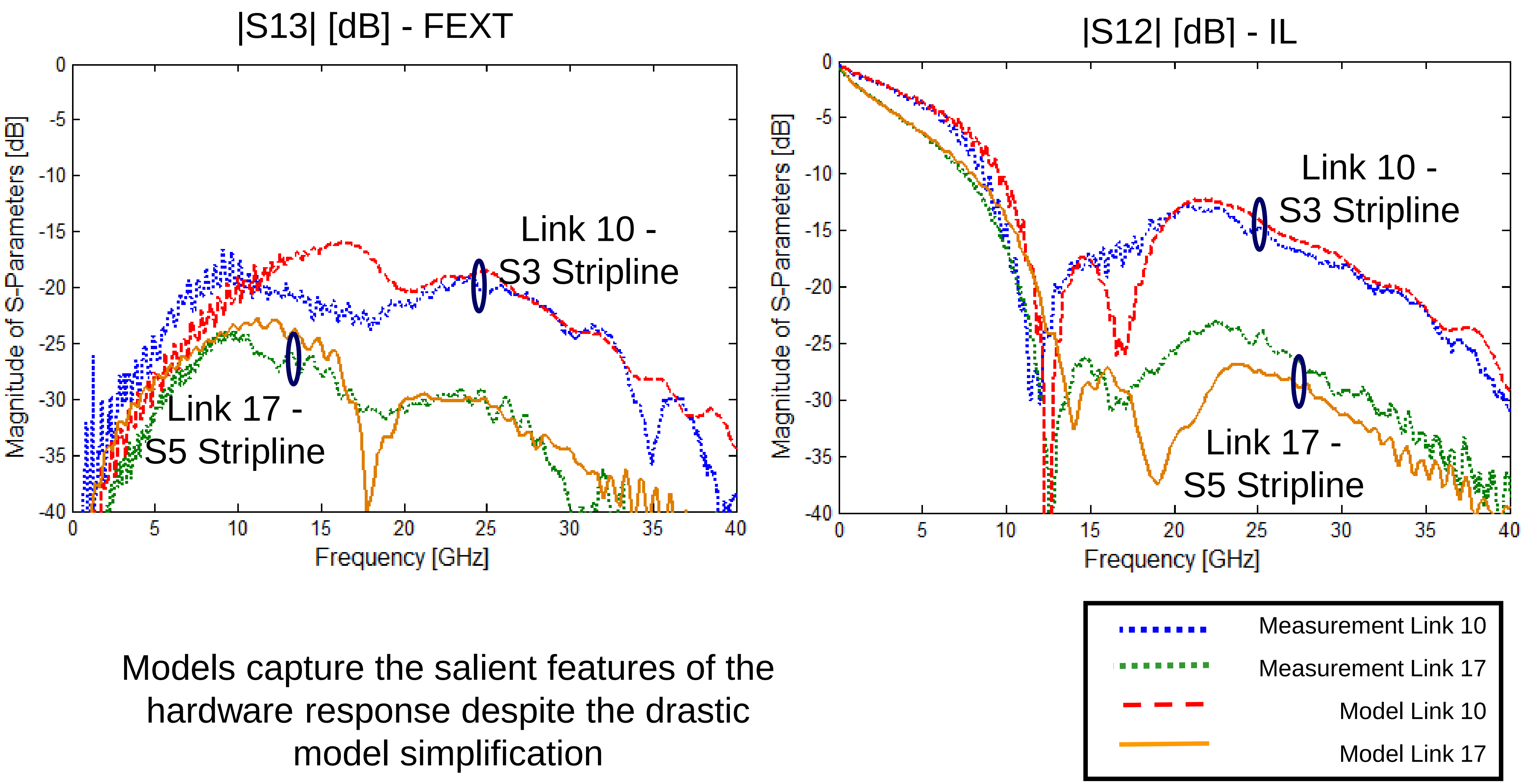
Assumption of infinite plates



- 119 vias (76 signal, 43 ground)
- 14 differential striplines (2D)
- 6 cavities
- Terminations

Comp. time: < 3 min

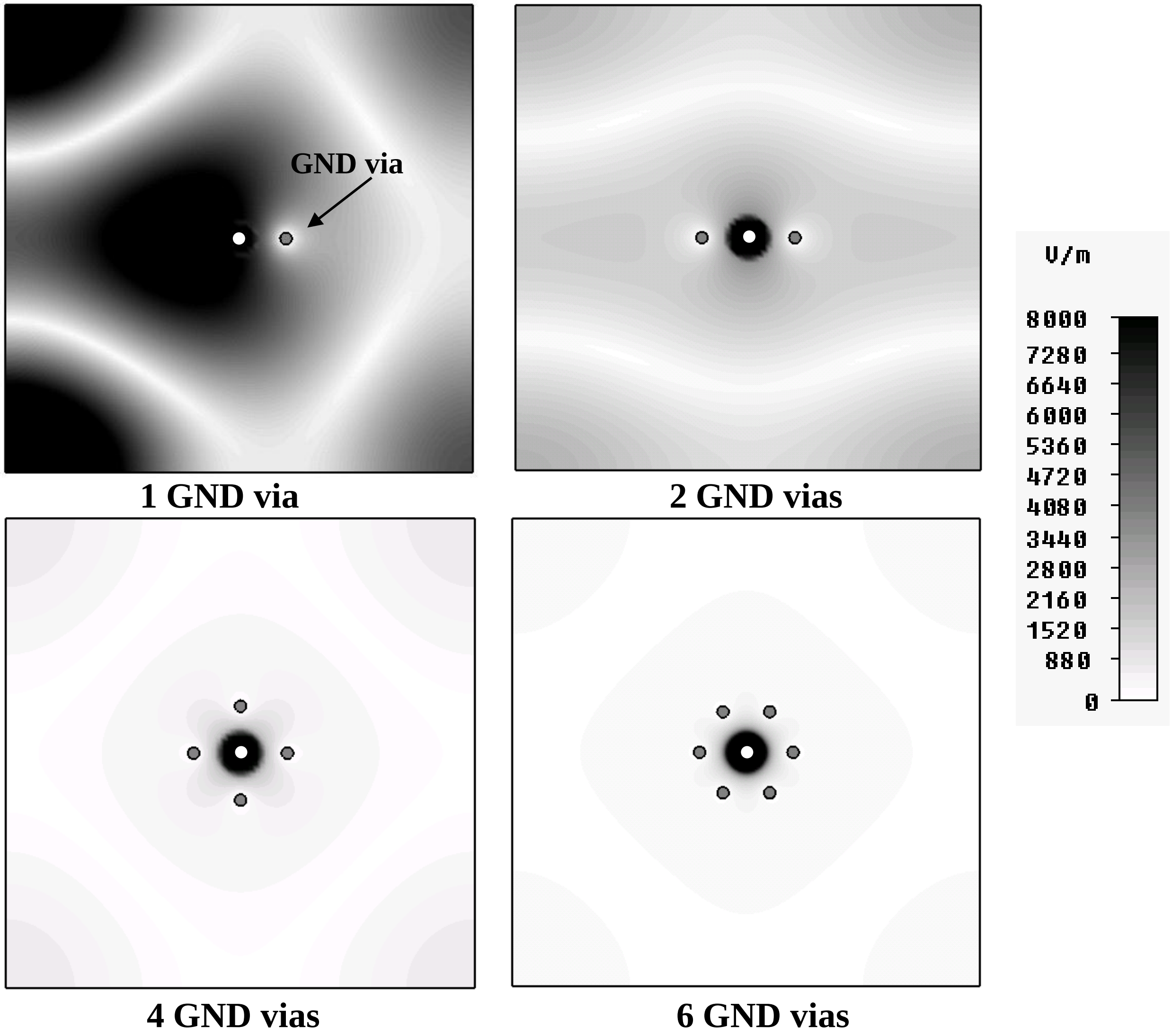
Comparison with Measurements



Models capture the salient features of the hardware response despite the drastic model simplification

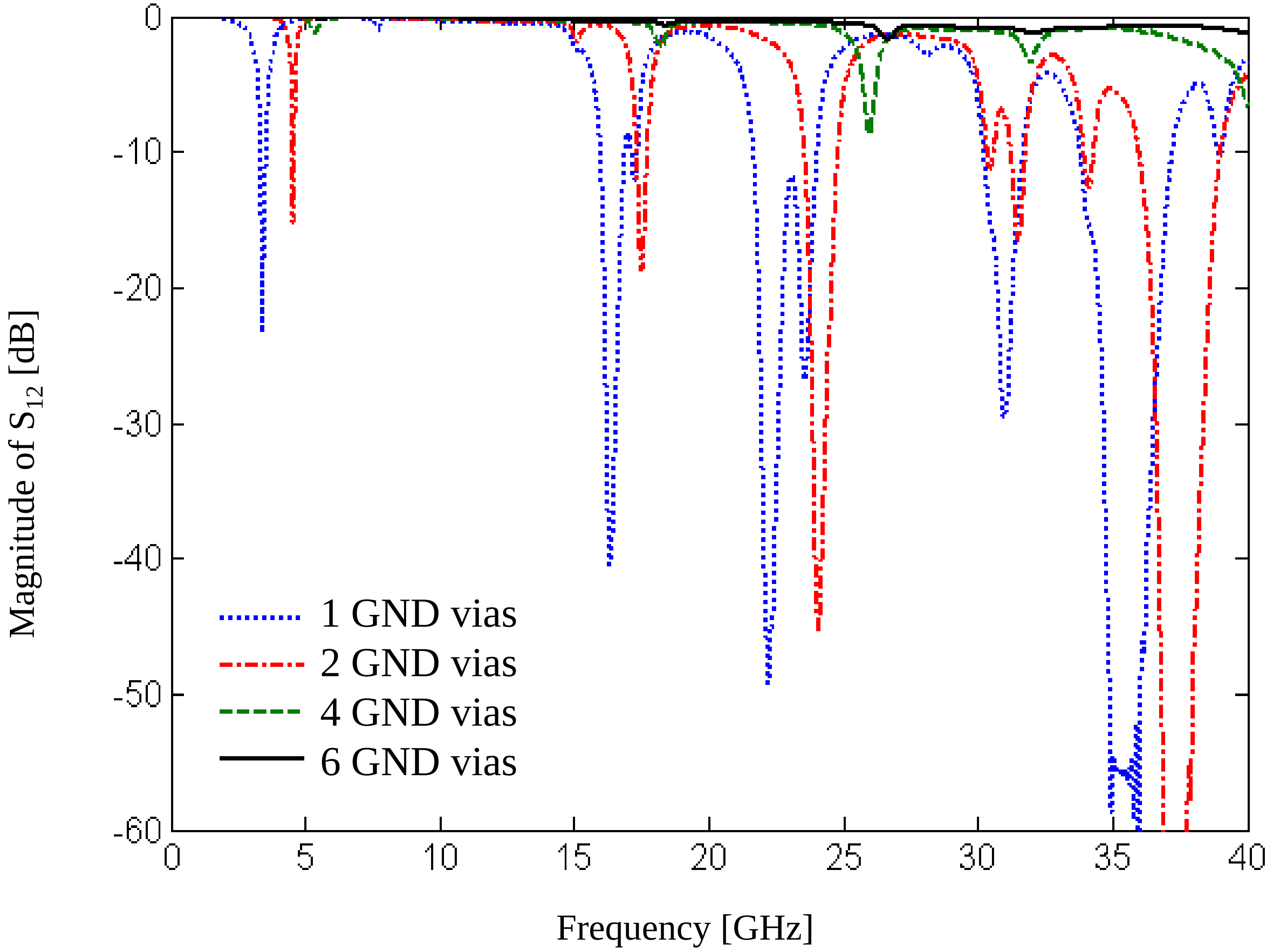
Investigation of Via Return Currents

Effect of number of ground vias:



Investigation of Via Return Currents

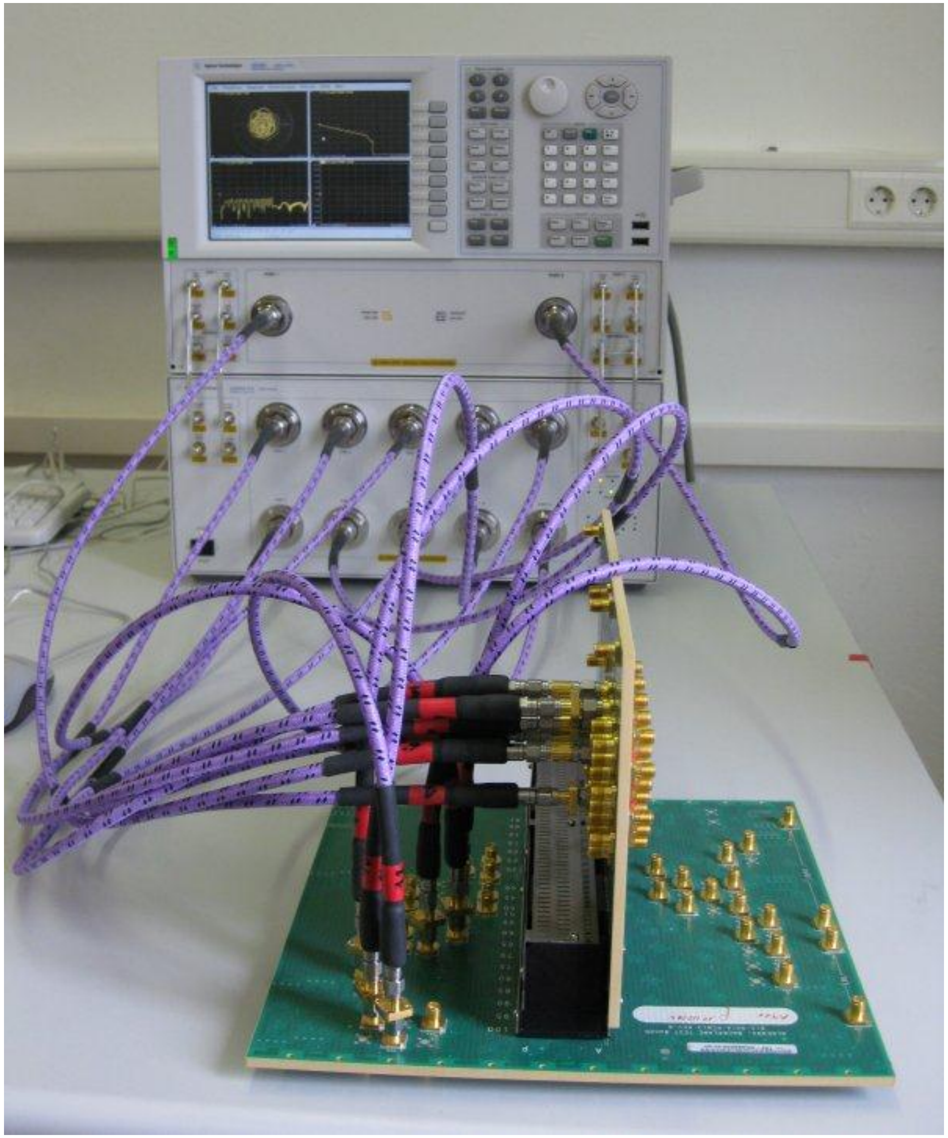
Effect of number of ground vias:



(5)

Measurement Techniques

Multiport Vector Network Analysis



Agilent Vector Network Analyzer 8364C with 12-port extension at Institute of Electromagnetic Theory (TUHH)

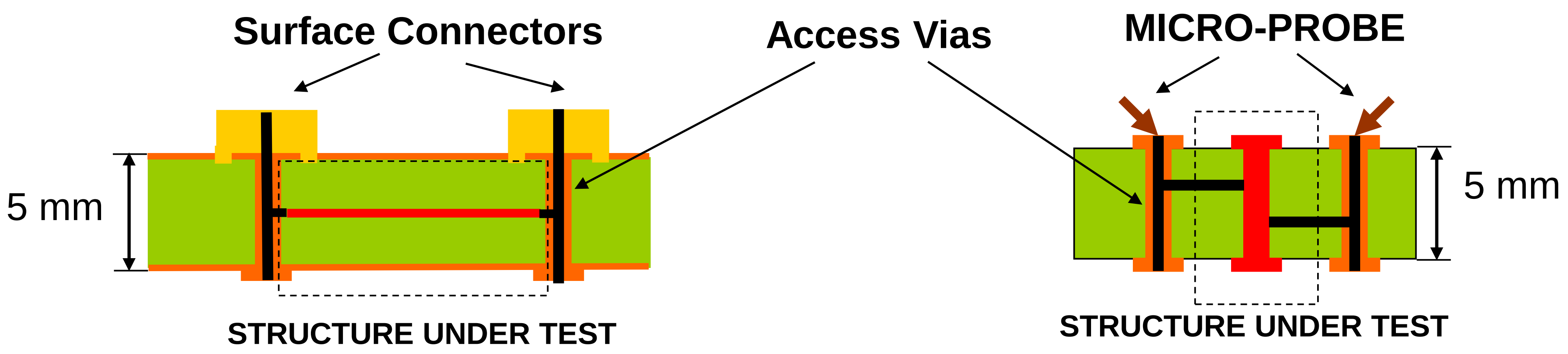
12 ports

Bandwidth 10 MHz – 50 GHz

Electronic calibration module

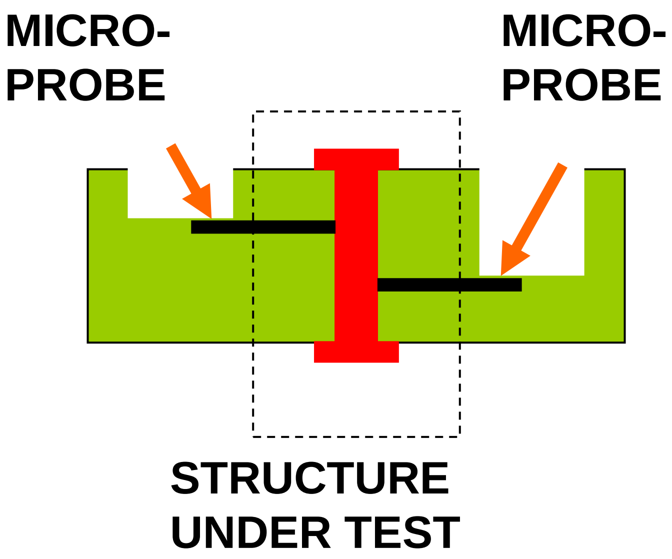
Advanced calibration software

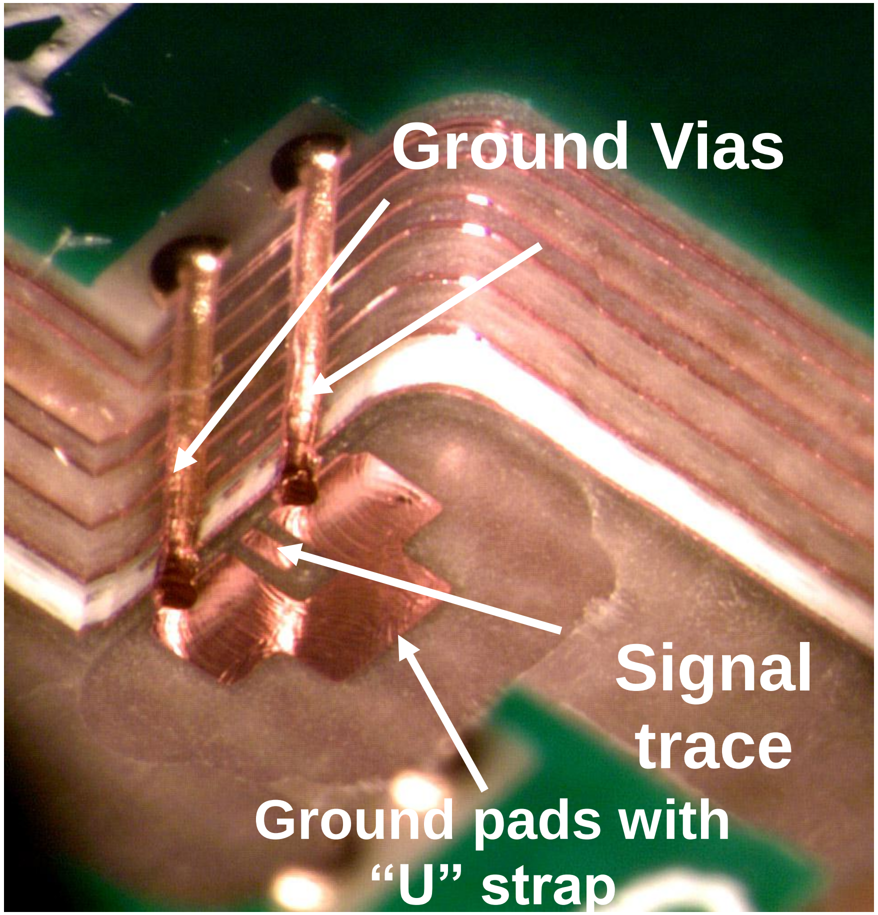
Common Surface Launches



... but vias are usually a high frequency bottleneck !

The Recessed Probe Launch (RPL)

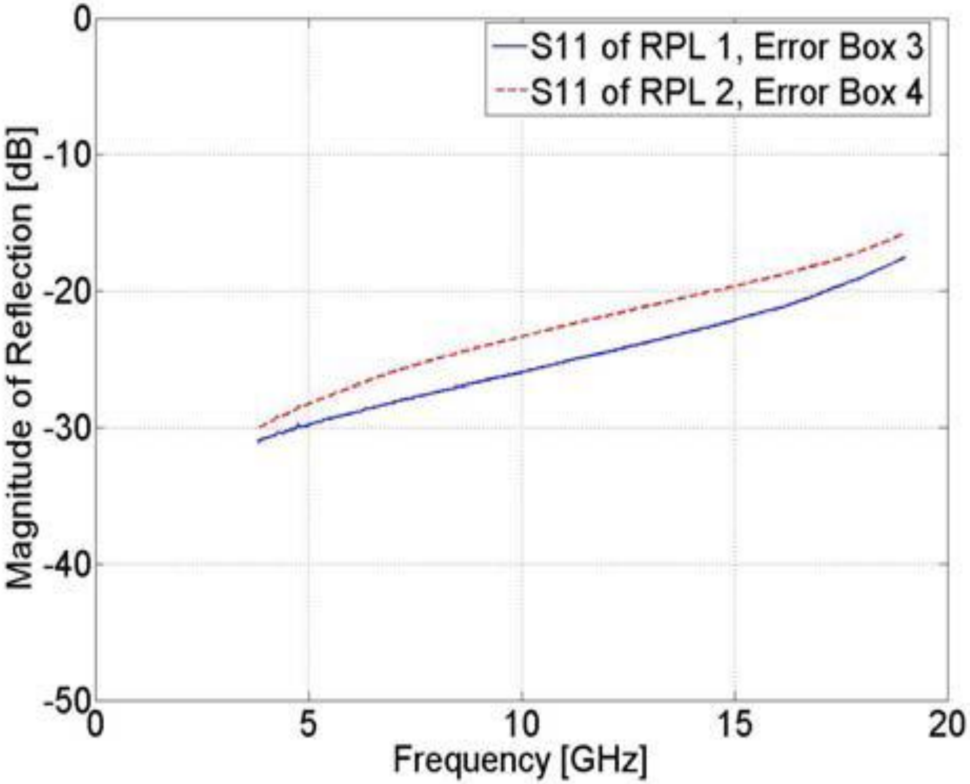


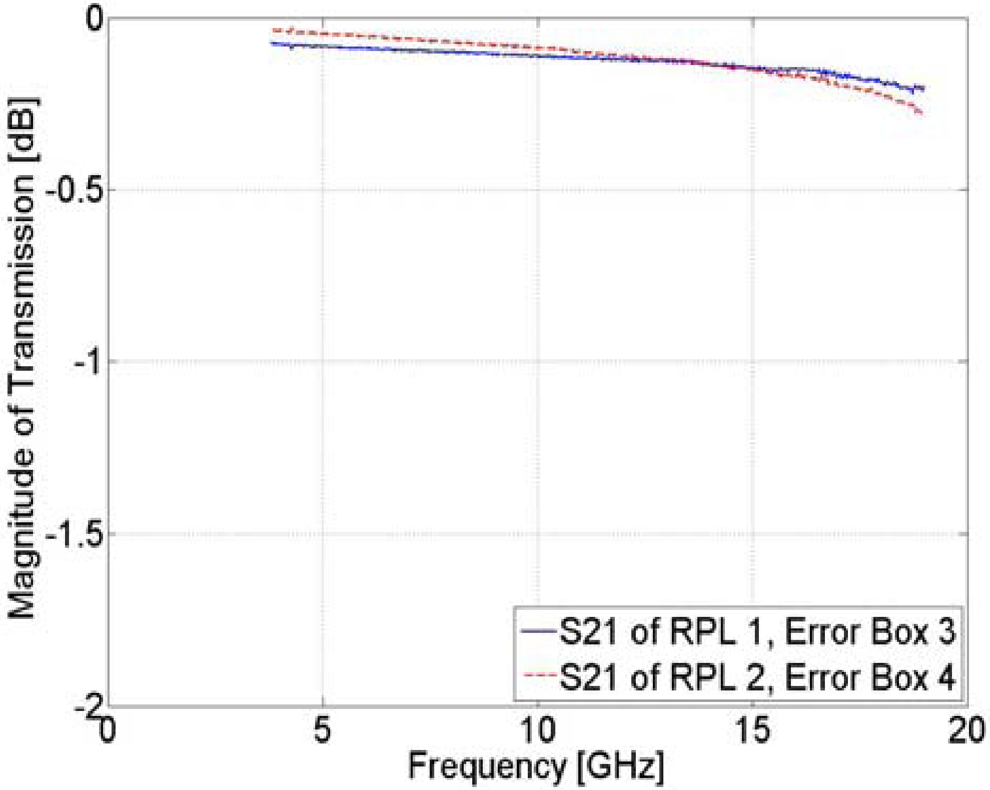


No access vias

→ less distortion
→ probes closer to the structure under test

RPL Error Box Extraction

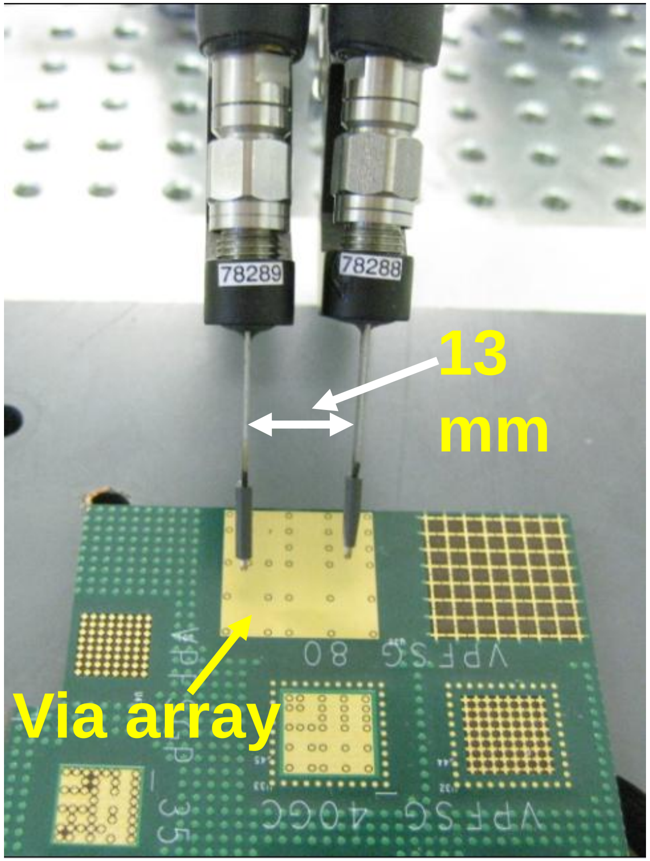


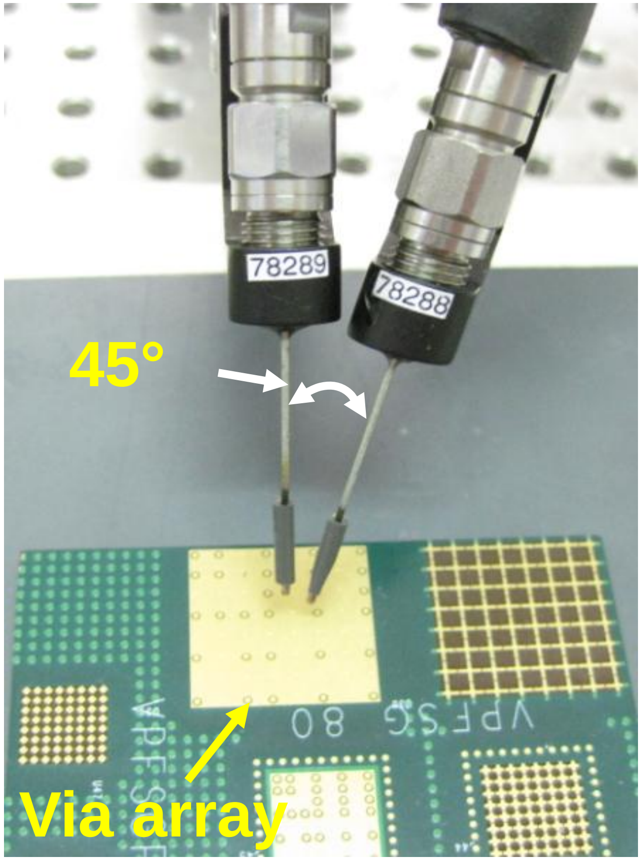


Error boxes of RPLs from TRL calibration

(thru = 90 mil long, line = 220 mil long)

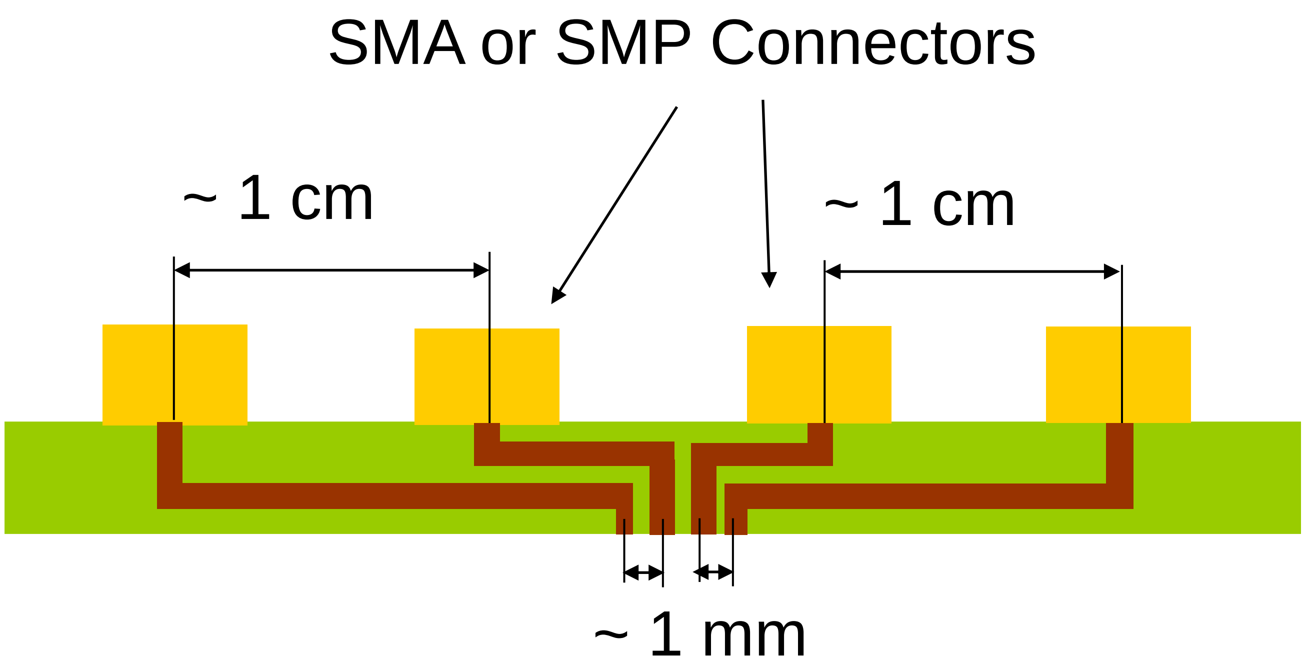
Problems with Via Arrays





… many vias at tight pitch!

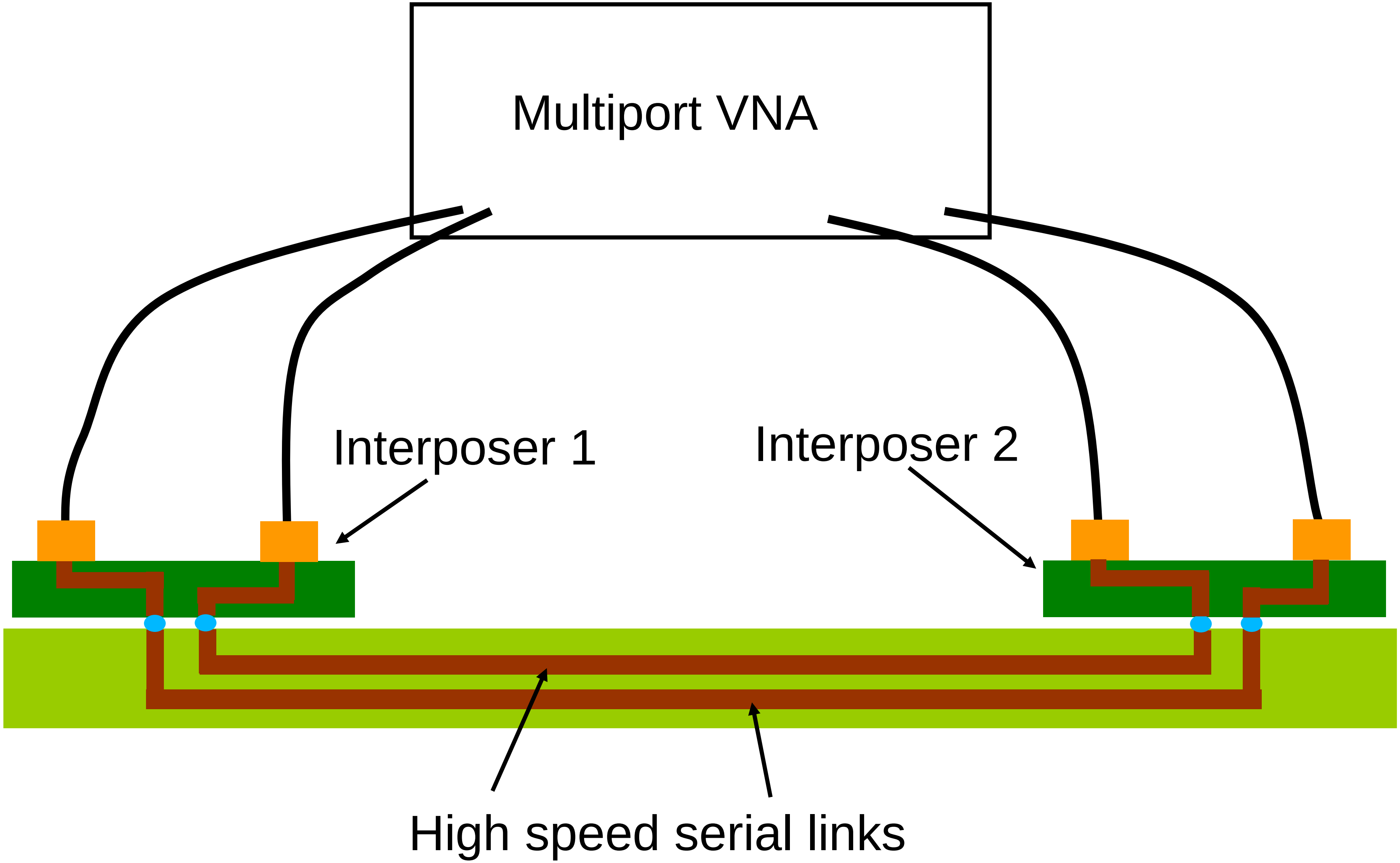
The Interposer Concept



Signal pitch conversion from ~1 cm to ~1 mm

& easy multiport access

Typical Measurement Set-up

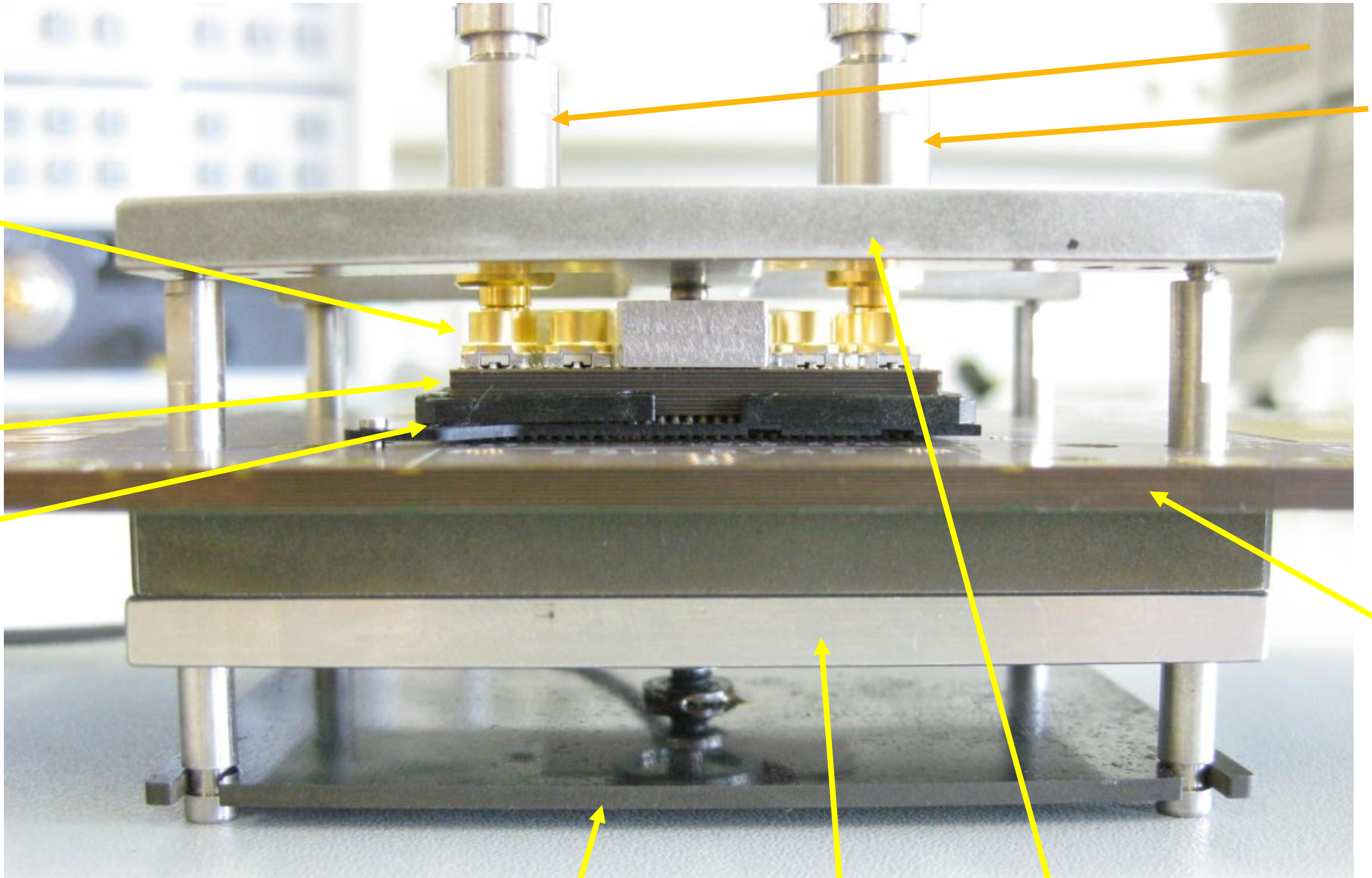


Interposer Prototype

SMP connectors

Interposer

LGA



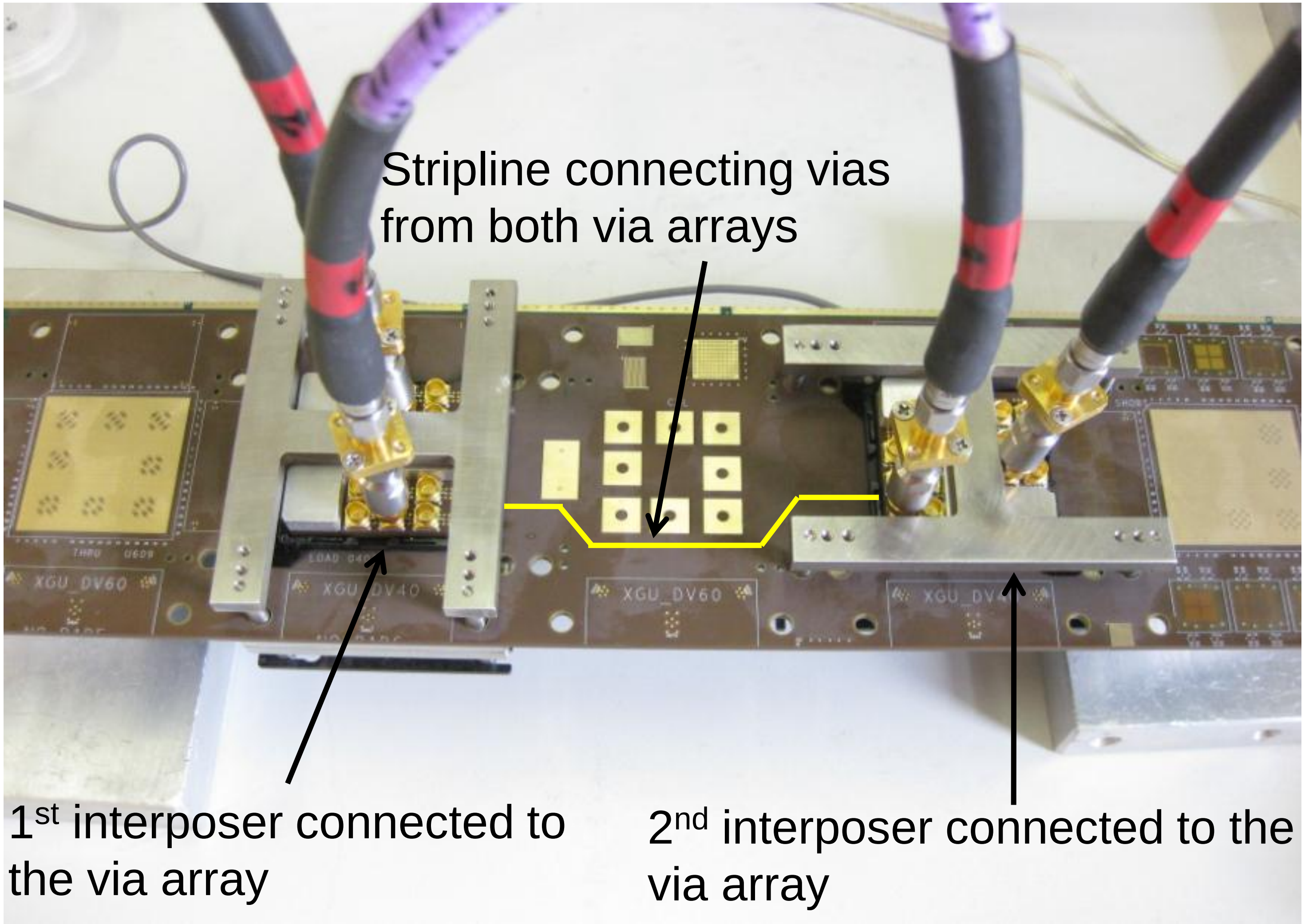
SMP adapters

Test board

Clamping and pressure plates

Hardware courtesy of IBM YKT (Y. Kwark)

Application to Link Measurement



1st interposer connected to the via array

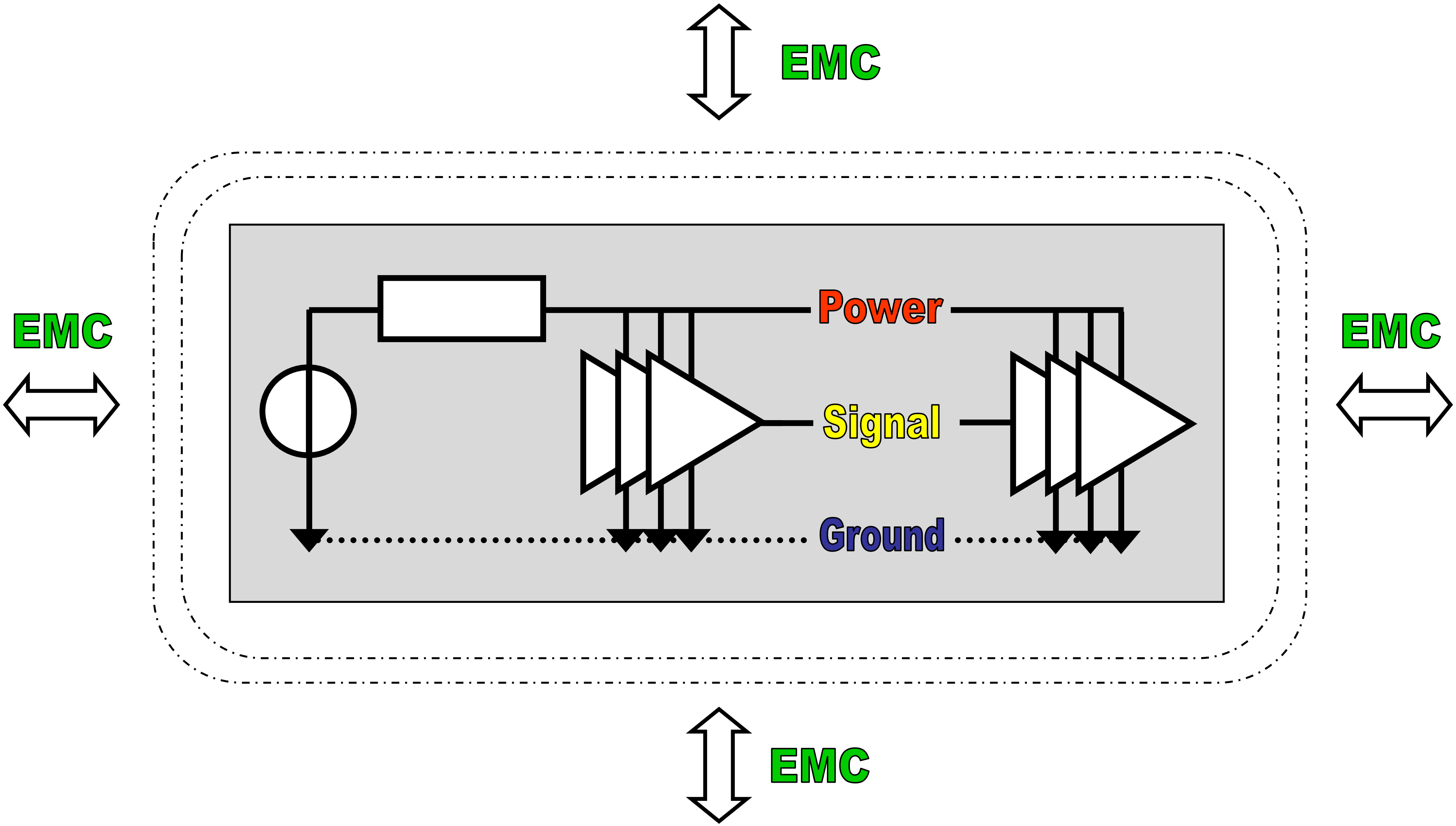
2nd interposer connected to the via array

Hardware courtesy of IBM YKT (Y. Kwark)

(6)

Wrapping Up

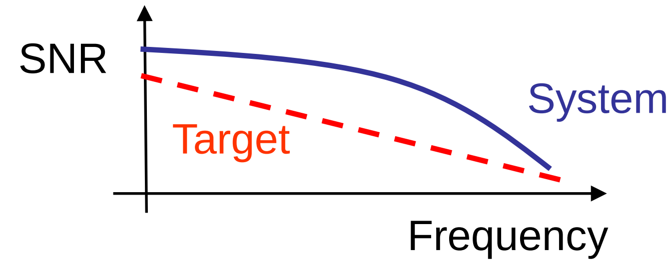
Electrical Integrity of Digital Systems



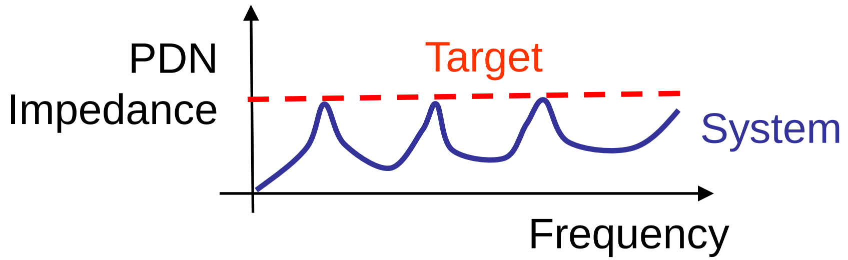
Electrical Integrity of Digital Systems

The basic goals of EMC, SI, and PI for an electrical system are complementary to each other.

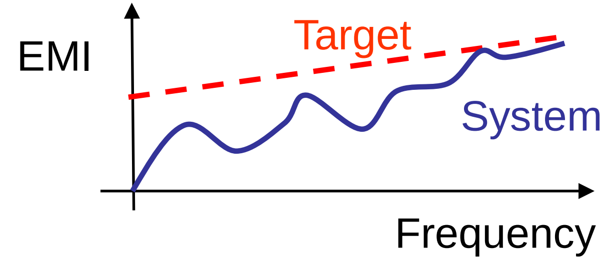
- ➔ **SIGNAL INTEGRITY**: insure acceptable quality of signals within



- ➔ **POWER INTEGRITY**: insure acceptable quality of power delivery within



- ➔ **EMC**: insure acceptable level of interference with the outside



Contact Information

Prof. Dr. sc. techn. Christian Schuster

Institut für Theoretische Elektrotechnik
Technische Universität Hamburg-Harburg
Harburger Schloss Str. 20
21079 Hamburg, Germany

Tel: +49 40 42878 3116
WWW: http://www.tet.tu-harburg.de/
E-Mail: schuster@tu-harburg.de