PCB Power Decoupling Myths Debunked

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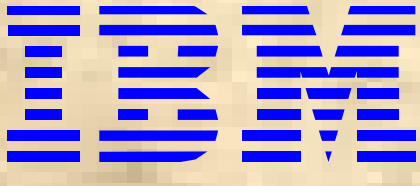
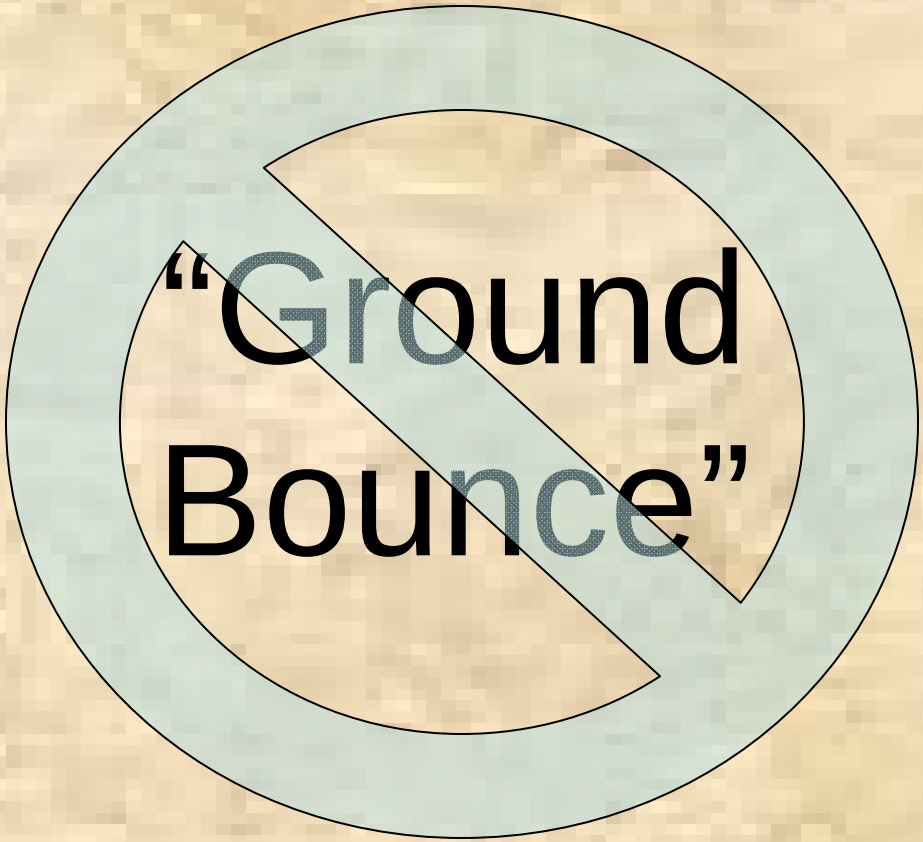


Conventional Wisdom

- Need a variety of capacitance values to maintain low impedance over frequency range
- Many capacitors of one value is better than many values
- Place capacitors close to ICs as possible
- Location does not matter
- Spread capacitors over entire board

Power Plane Noise Control



What is Capacitance?

$$C = \frac{Q}{V}$$

$$Q = CV$$

- Capacitance is the ability of a structure to hold charge (electrons) for a given voltage
- Amount of charge stored is dependant on the size of the capacitance (and voltage)

Note: Capacitance has no frequency dependence!

High Frequency Capacitors

- Myth or Fact?

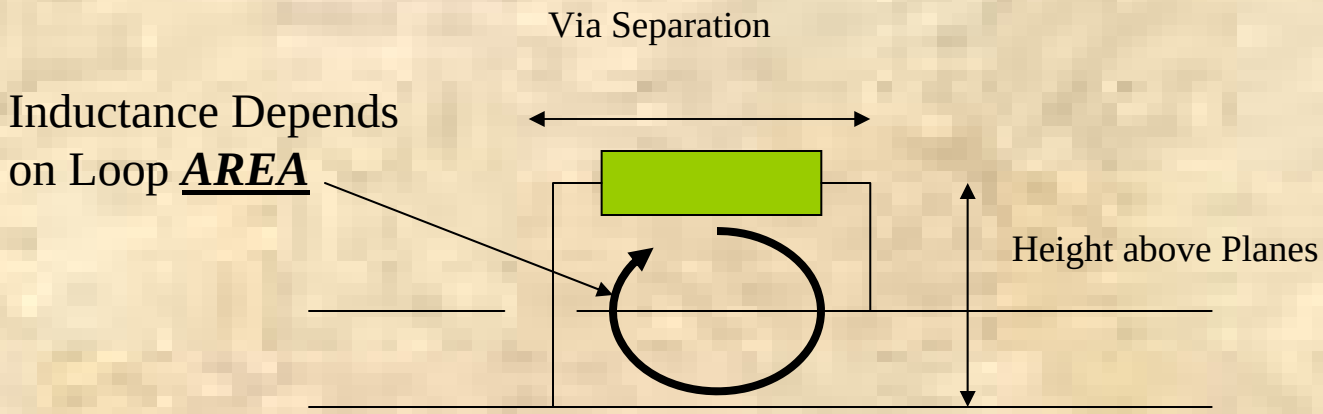
It’s really the inductance that matters!

Capacitance and Inductance

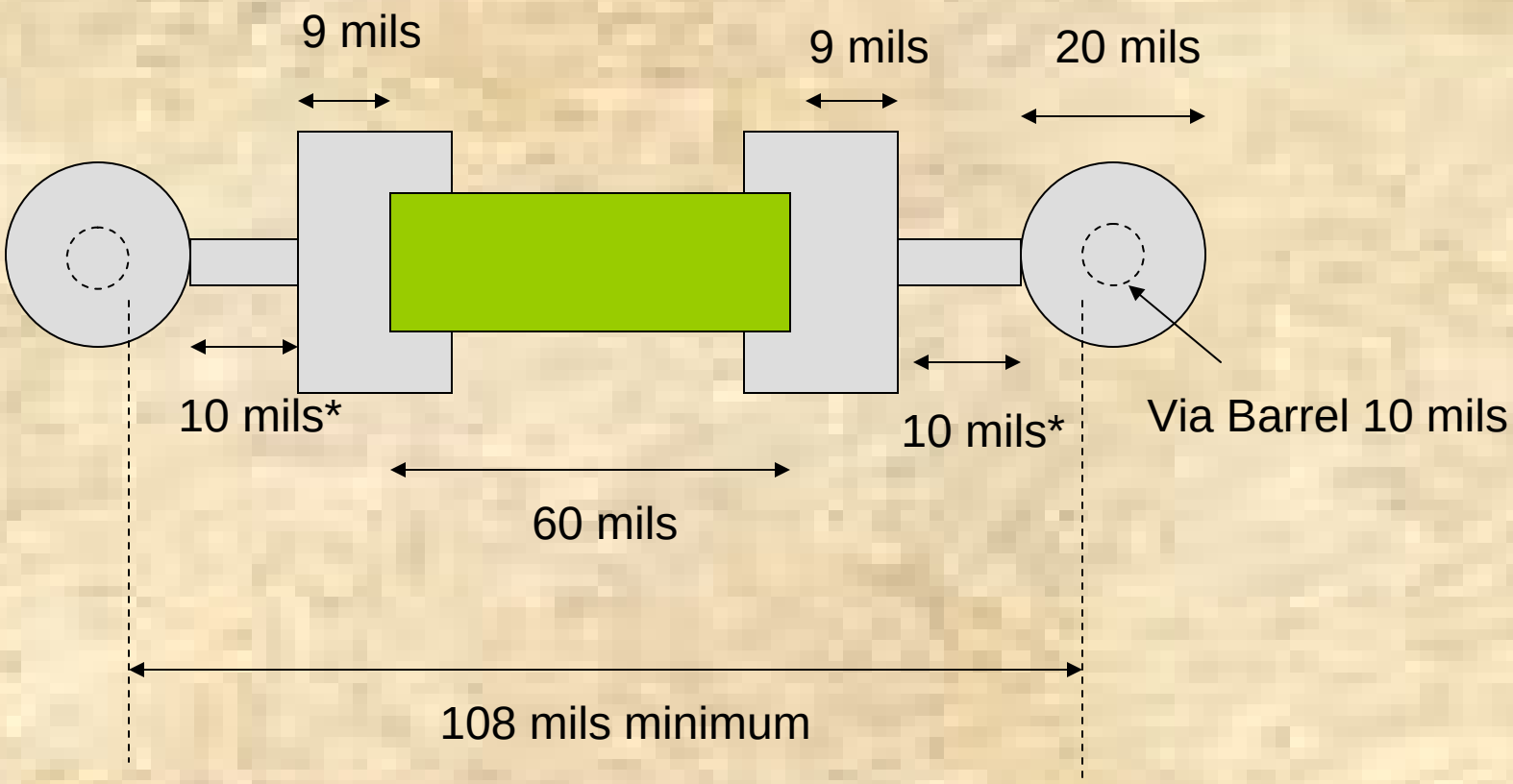
- ***Capacitance*** → amount of charge stored
- ***Inductance*** → speed that the charge can be delivered from capacitor

Decoupling Capacitor Mounting

- Keep as to planes as close to capacitor pads as possible

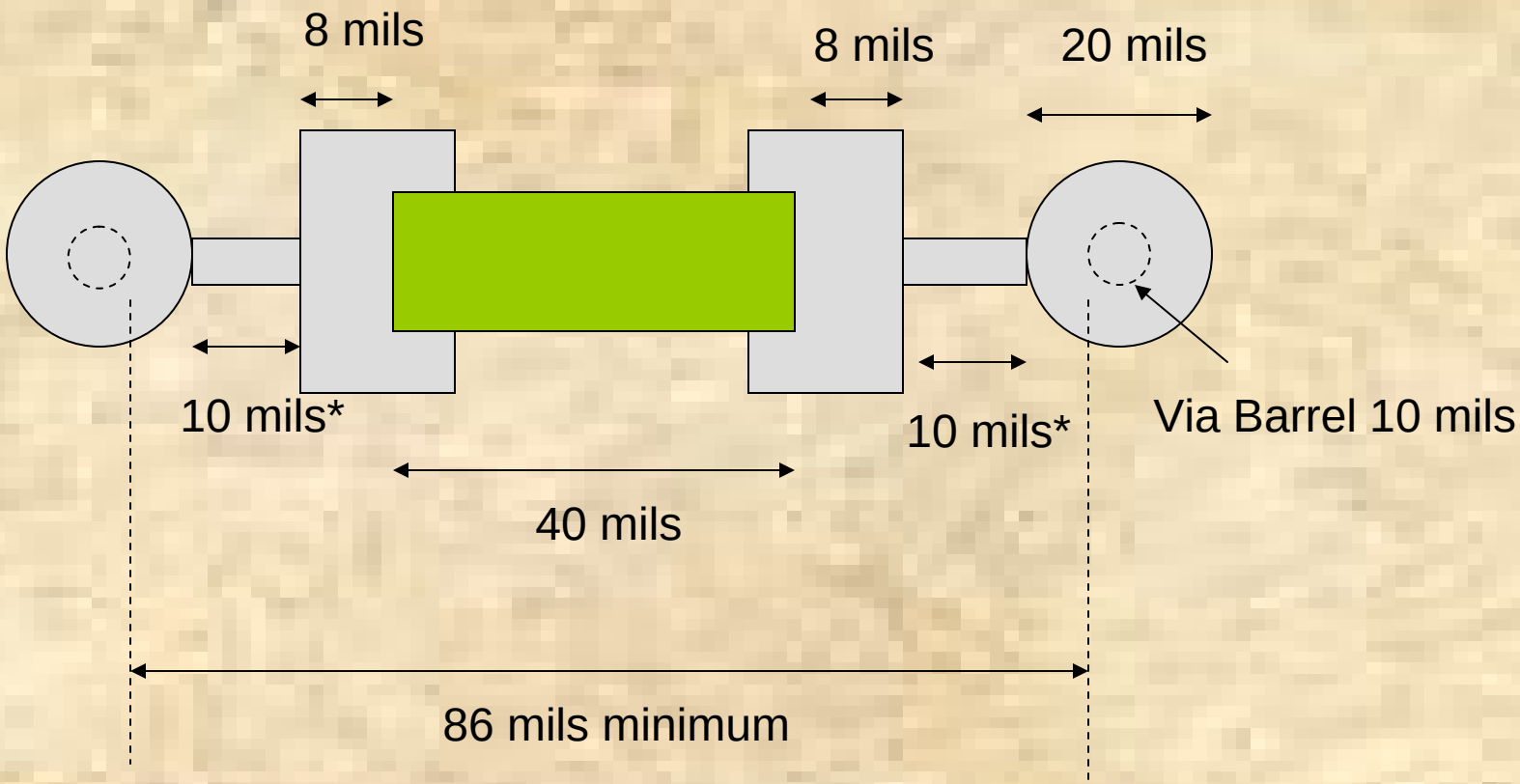


0603 Size Cap Typical Mounting



*Note: Minimum distance is 10 mils but more typical distance is 20 mils

0402 Size Cap Typical Mounting



*Note: Minimum distance is 10 mils but more typical distance is 20 mils

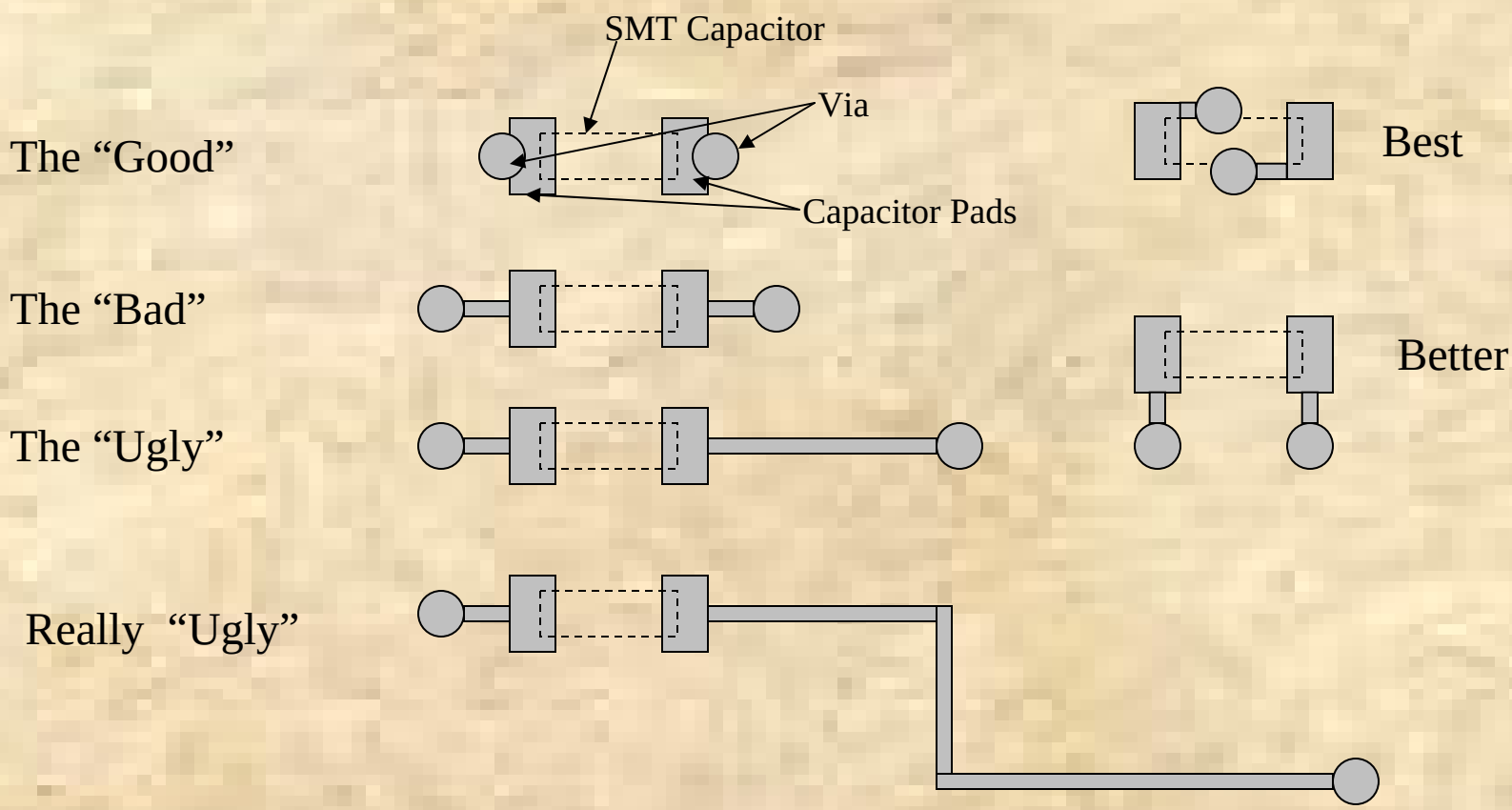
Connection Inductance for Typical Capacitor Configurations Configurations with 10 mils from Capacitor Pad to Via Pad

Distance into board to planes (mils)	0805 typical (148 mils between via barrels)	0603 typical (128 mils between via barrels)	0402 typical (106 mils between via barrels)
10	1.2 nH	1.1 nH	0.9 nH
20	1.8 nH	1.6 nH	1.3 nH
30	2.2 nH	1.9 nH	1.6 nH
40	2.5 nH	2.2 nH	1.9 nH
50	2.8 nH	2.5 nH	2.1 nH
60	3.1 nH	2.7 nH	2.3 nH
70	3.4 nH	3.0 nH	2.6 nH
80	3.6 nH	3.2 nH	2.8 nH
90	3.9 nH	3.5 nH	3.0 nH
100	4.2 nH	3.7 nH	3.2 nH

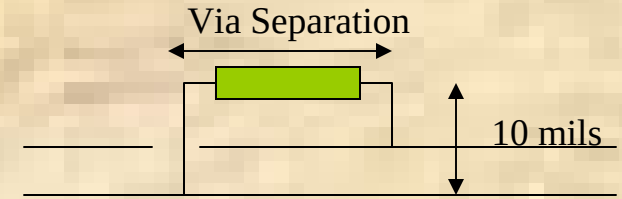
Connection Inductance for Typical Capacitor Configurations with 50 mils from Capacitor Pad to Via Pad

Distance into board to planes (mils)	0805 (208 mils between via barrels)	0603 (188 mils between via barrels)	0402 (166 mils between via barrels)
10	1.7 nH	1.6 nH	1.4 nH
20	2.5 nH	2.3 nH	2.0 nH
30	3.0 nH	2.8 nH	2.5 nH
40	3.5 nH	3.2 nH	2.8 nH
50	3.9 nH	3.5 nH	3.1 nH
60	4.2 nH	3.9 nH	3.5 nH
70	4.5 nH	4.2 nH	3.7 nH
80	4.9 nH	4.5 nH	4.0 nH
90	5.2 nH	4.7 nH	4.3 nH
100	5.5 nH	5.0 nH	4.6 nH

Via Configuration Can Change Inductance



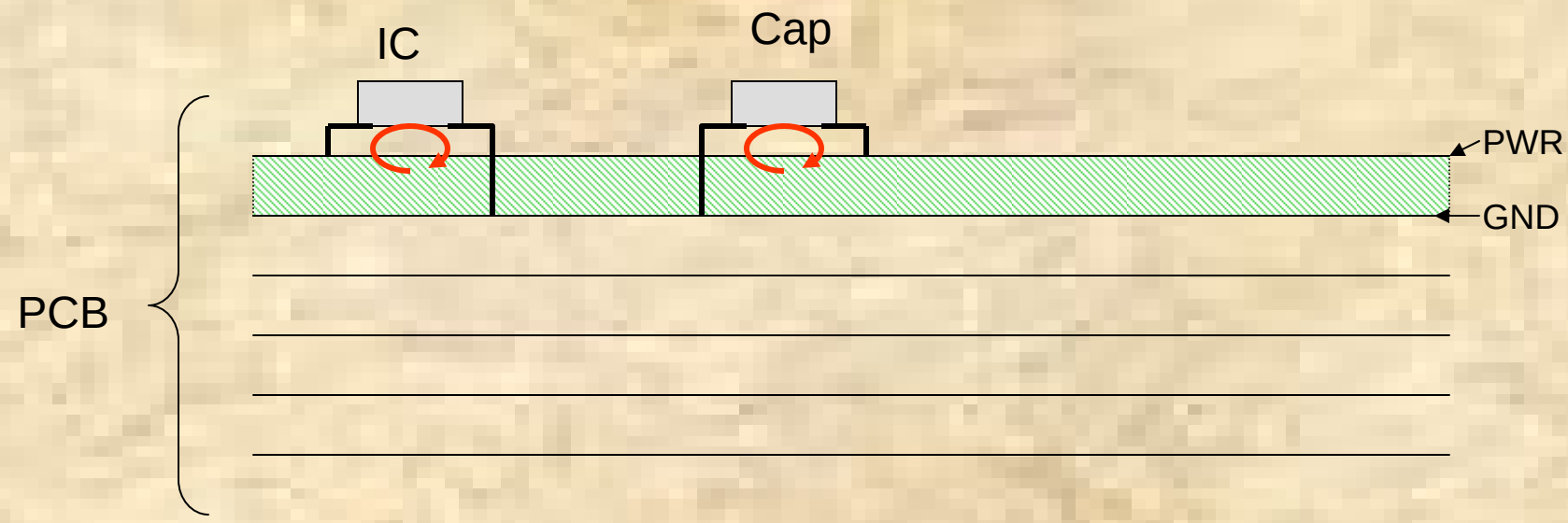
Comparison of Decoupling Capacitor Via Separation Distance Effects



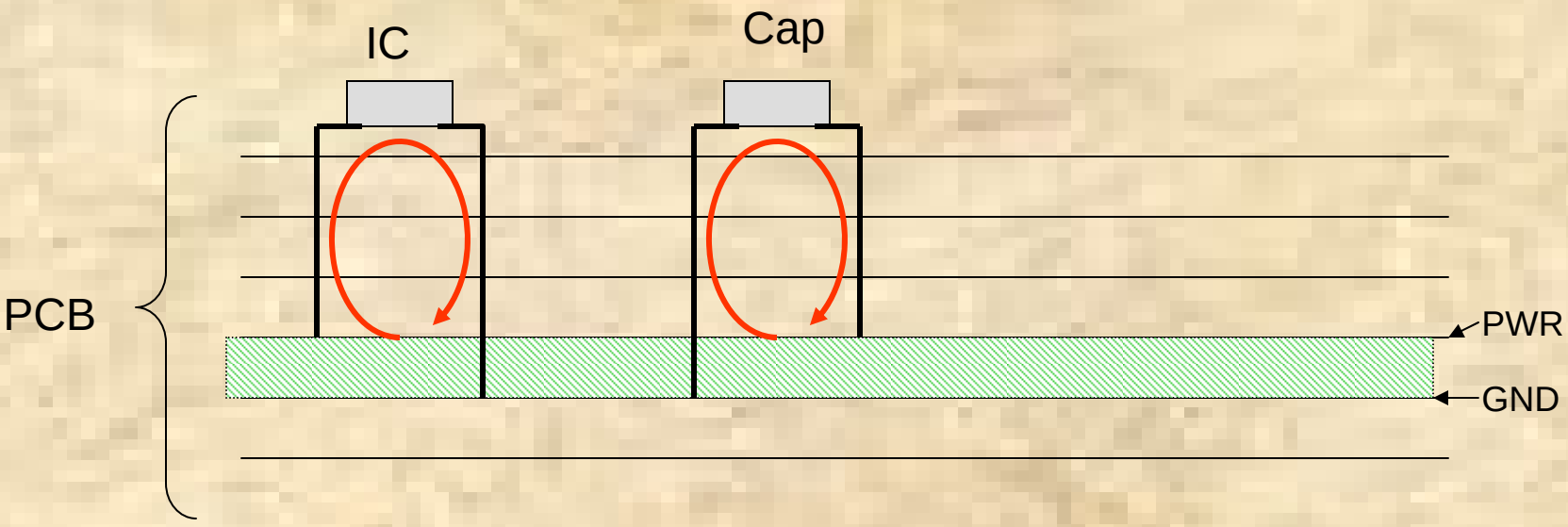
0.1 uF Capacitor

Via separation, mils	Inductance, nH	Impedance @1 GHz, Ohms
20	0.06	0.41
40	0.21	1.3
60	0.36	2.33
80	0.5	3.1
100	0.64	4.0
150	1.0	6.23
200	1.4	8.5
300	2.1	12.7
400	2.75	17.3
500	3.5	21.7

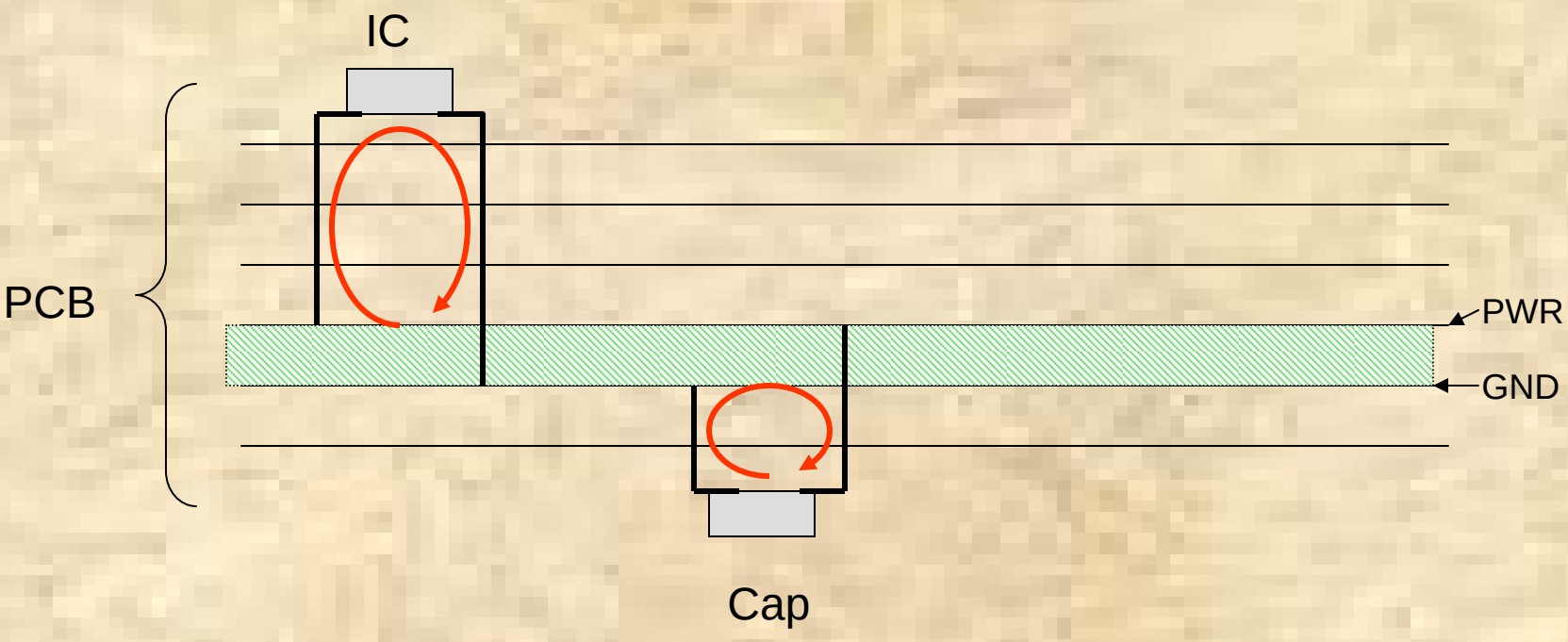
Example #1
Low Cap Connection Inductance



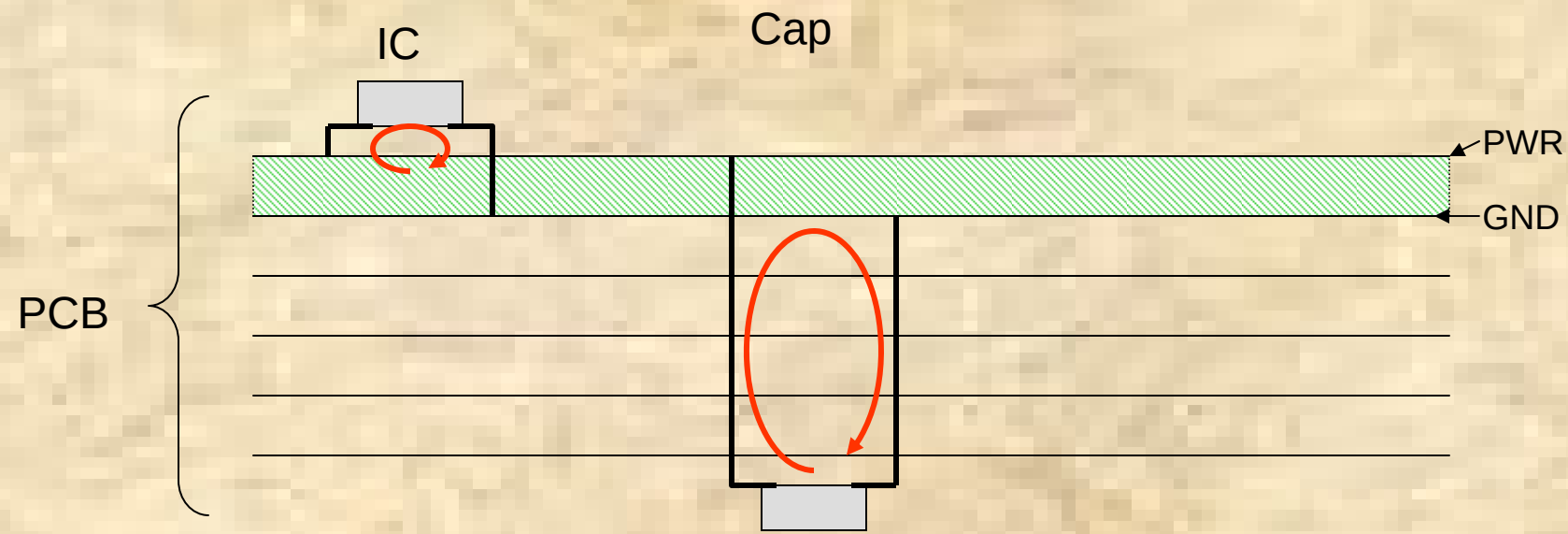
Example #2
Hi Cap Connection Inductance



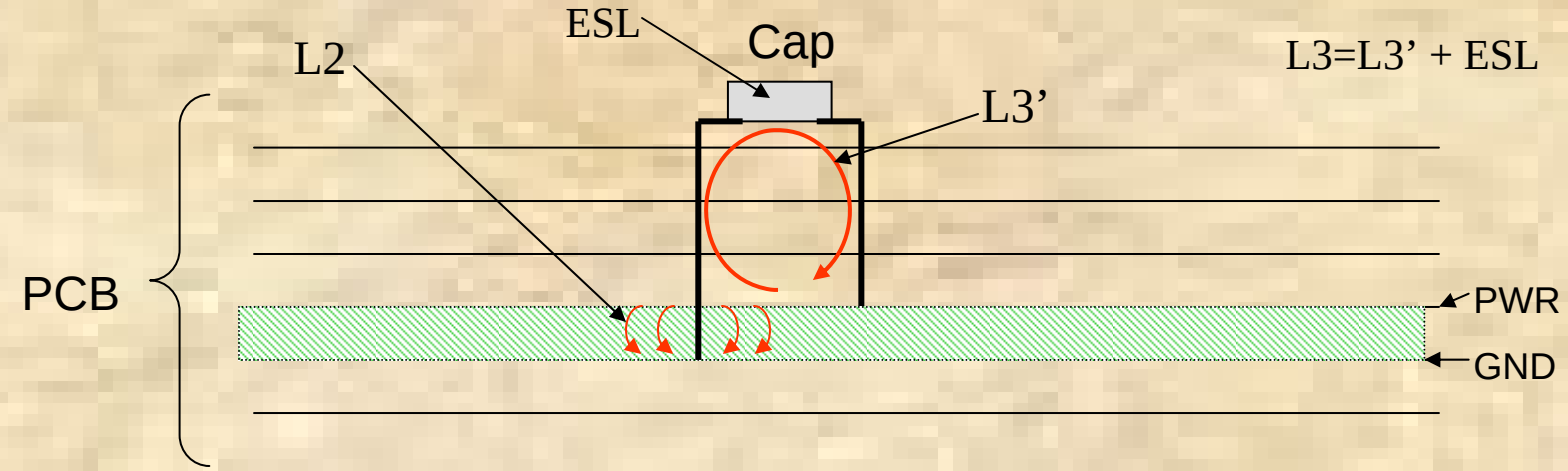
Example #3
Lower Cap Connection Inductance



Example #4
High Cap Connection Inductance



Capacitor Connection Inductance Ratio



Power/GND plane spacing, (mils)	via diameter, (mils)	L_2 (nH)
10	10	0.32
10	13	0.304
10	25	0.27
35	10	1.1
35	13	1.07
35	25	0.95

62mil brd centered plane spacing, mils	0603 SMT L3' (nH)	L3/L2	L3/L2 w/extra 100 mil trace length	L3/L2 w/extra 200 mil trace length	L3/L2 w/extra 300 mil trace length
10	1.66	6.75	9.13	11.50	13.88
35	0.92	1.29	1.98	2.67	3.36

For local decoupling need L3/L2 < 3

Decoupling Must be Analyzed in Different Ways for Different Functions

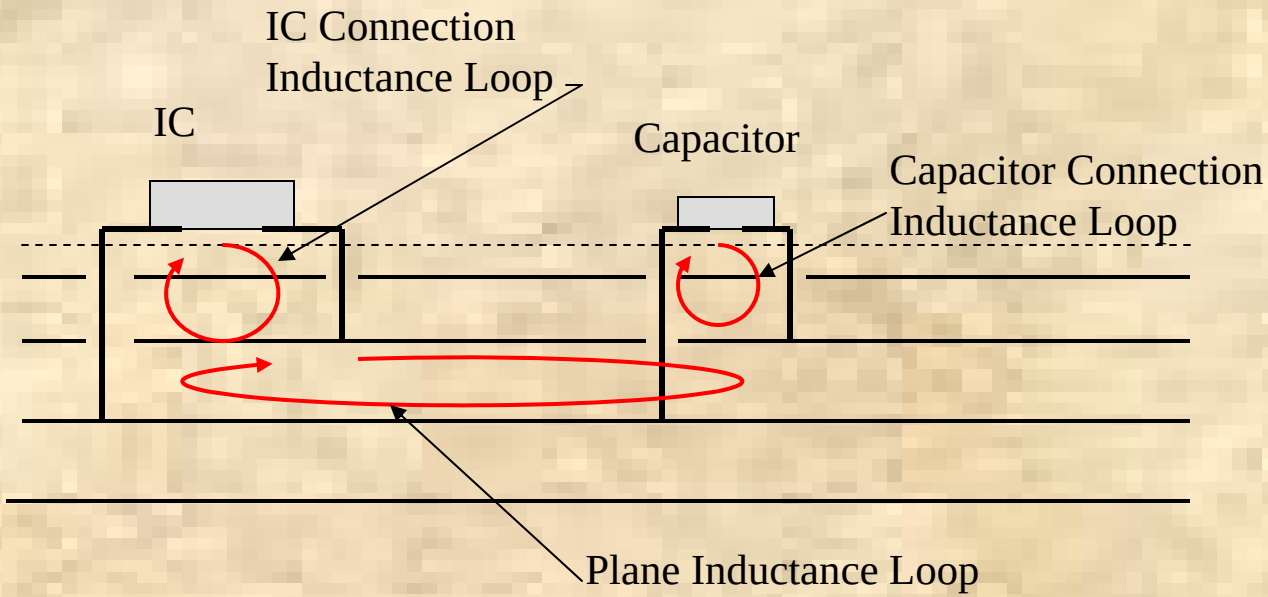
- EMC
  - Resonance big concern
  - Requires STEADY-STATE analysis
    - Frequency Domain
  - Transfer function analysis
    - Eliminate noise along edge of board due to ASIC/IC located far away

Decoupling Must be Analyzed in Different Ways for Different Functions

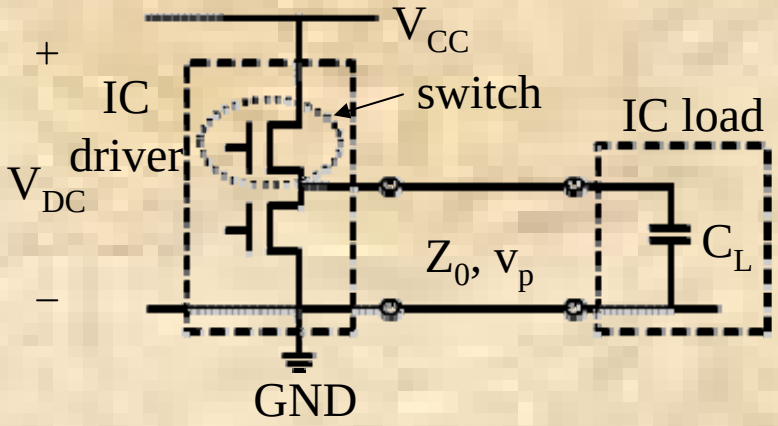
- Provide Charge to ASIC/IC
  - Requires time-limited analysis
    - Charge must get to the IC ***during the time it is needed!***
  - Charge will NOT travel from far corners of the board fast enough
  - Local decoupling capacitors dominate

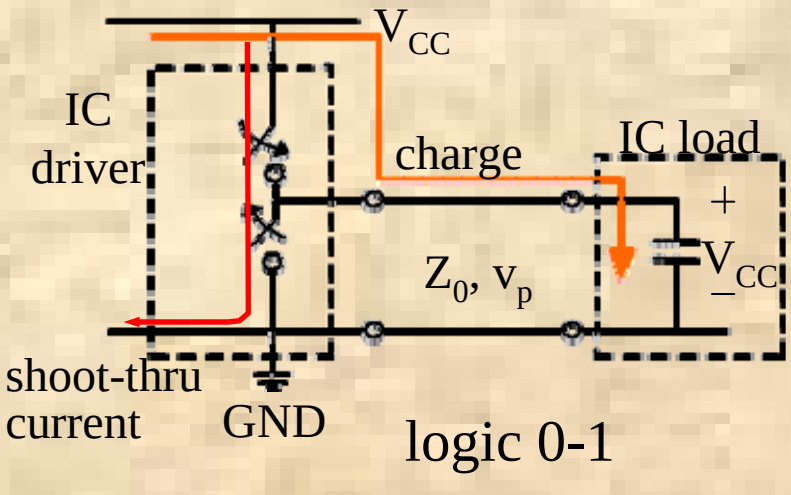
Decoupling Capacitor Mounting

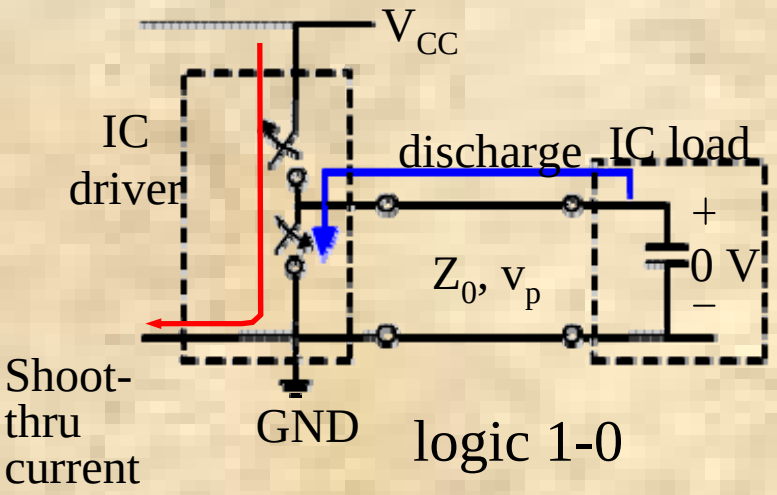
- Keep as to planes as close to capacitor pads as possible



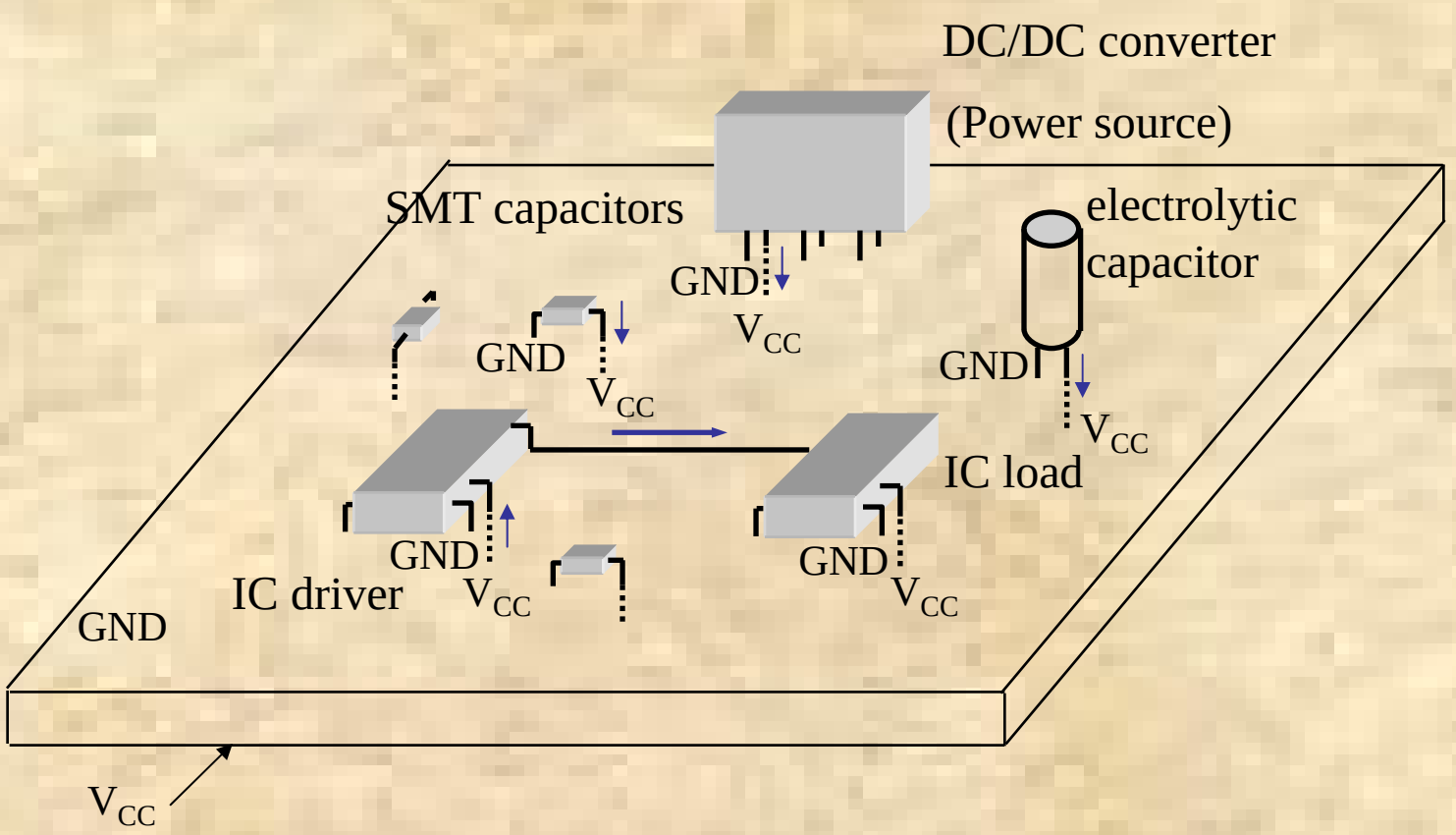
Current in IC During Logic Transitions (CMOS)



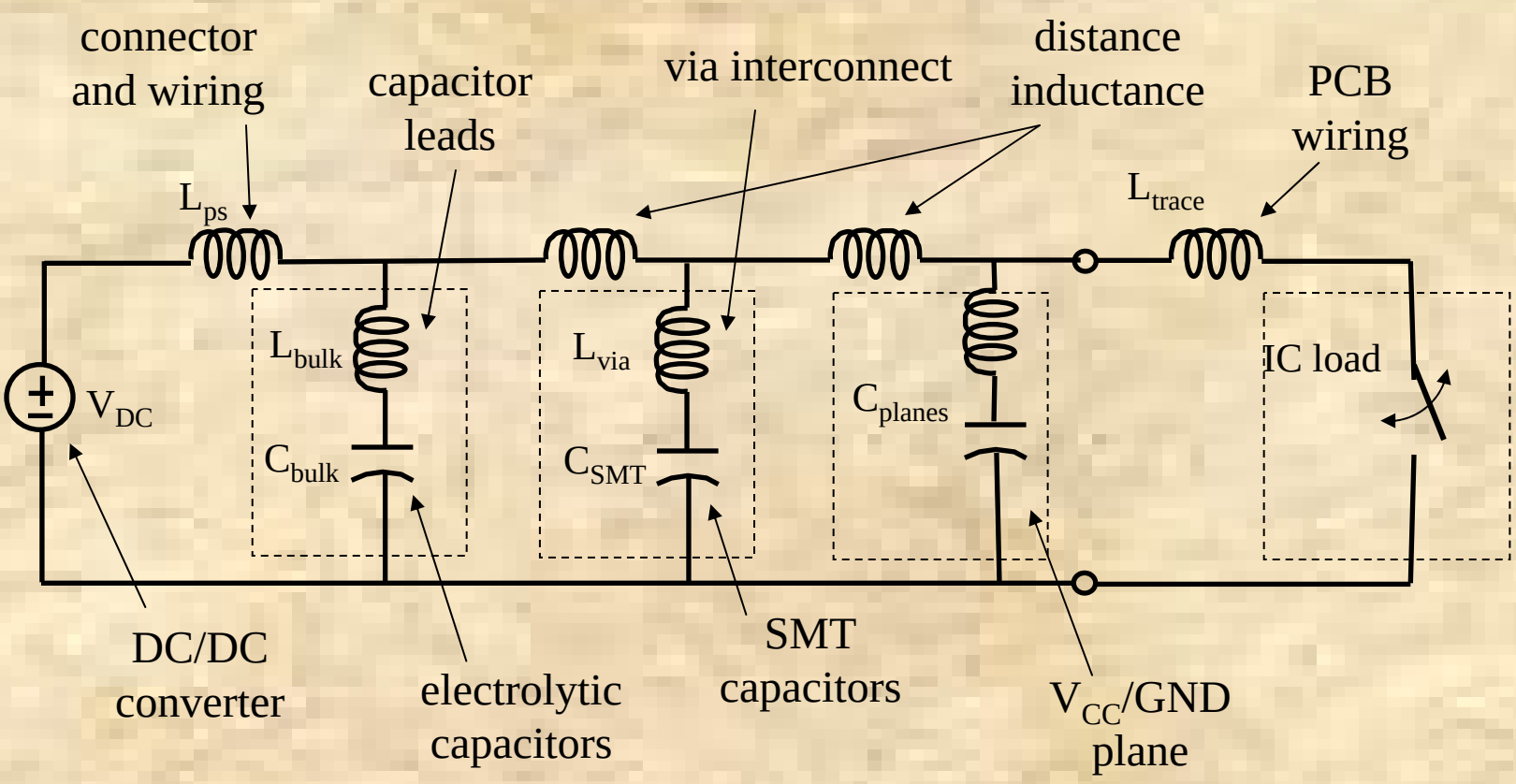




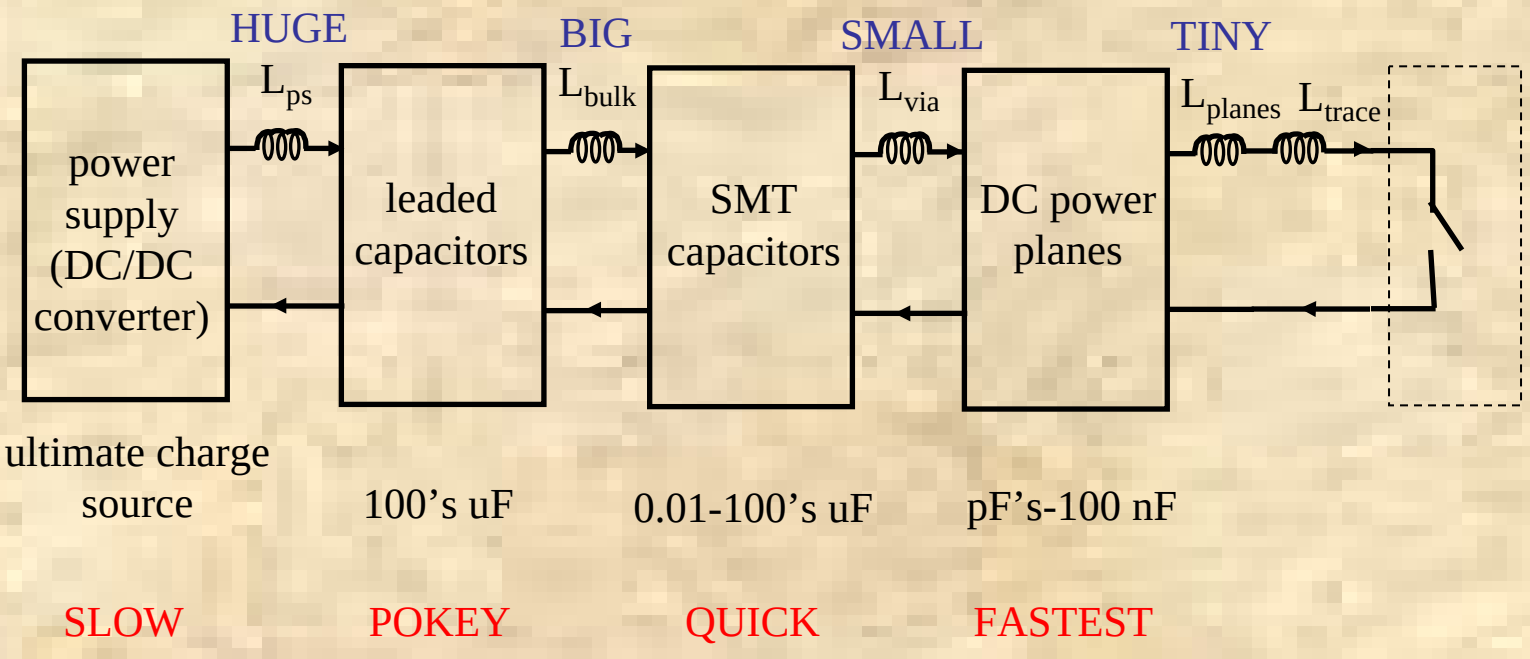
Typical PCB Power Delivery



Equivalent Circuit for Power Current Delivery to IC

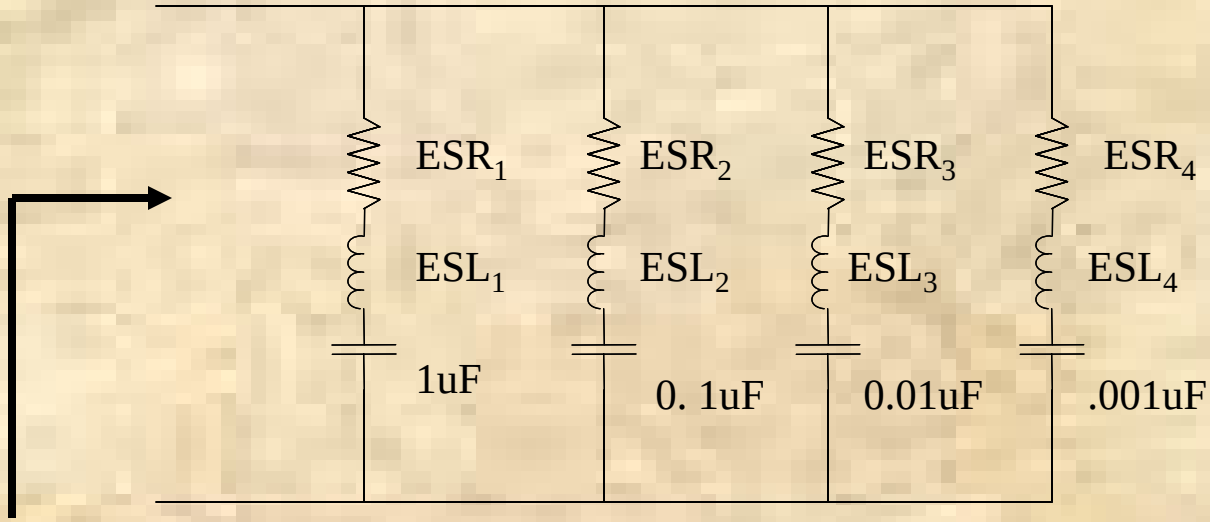


Power Bus Charging Hierarchy



Traditional Analysis #1

- Use impedance of capacitors in parallel



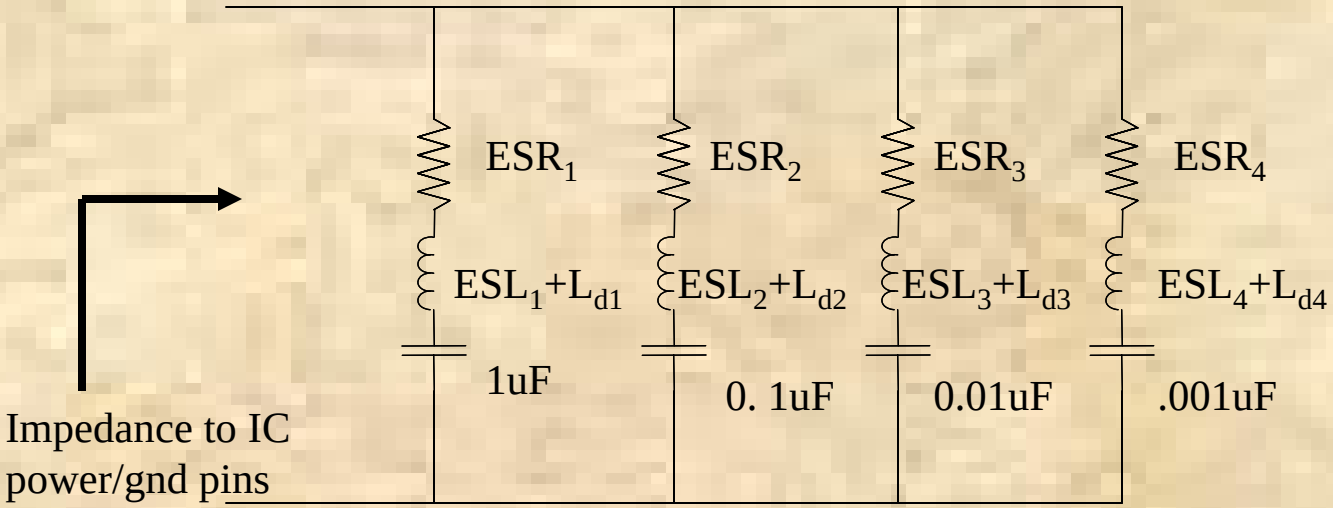
Impedance to IC power/gnd pins

No Effect of Distance Between Capacitors and IC Included!

Traditional Impedance Calculation for Four Decoupling Capacitor Values

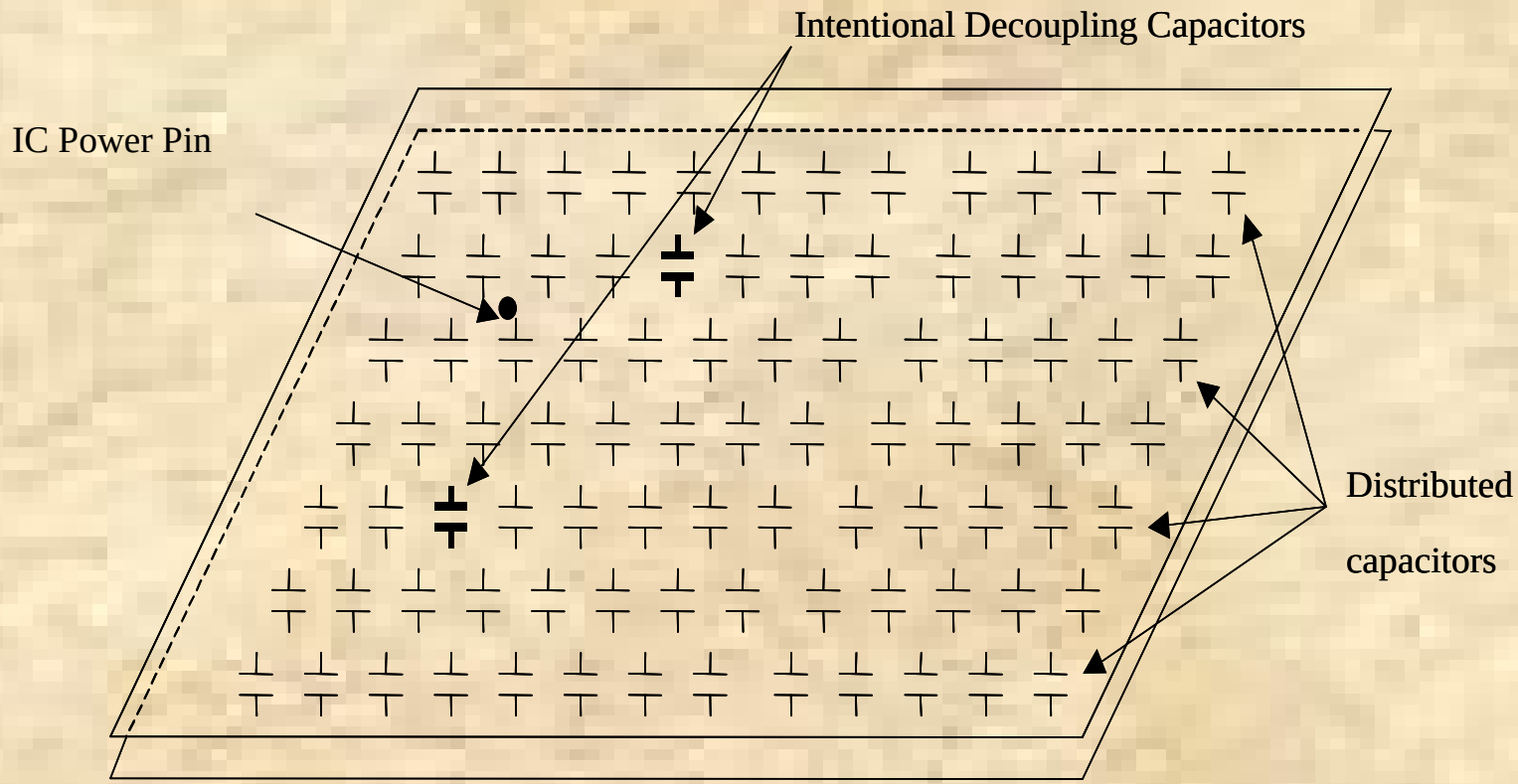
Traditional Analysis #2

- Calculate loop area – Traditional loop Inductance formulas
  - Which loop area? Which size conductor

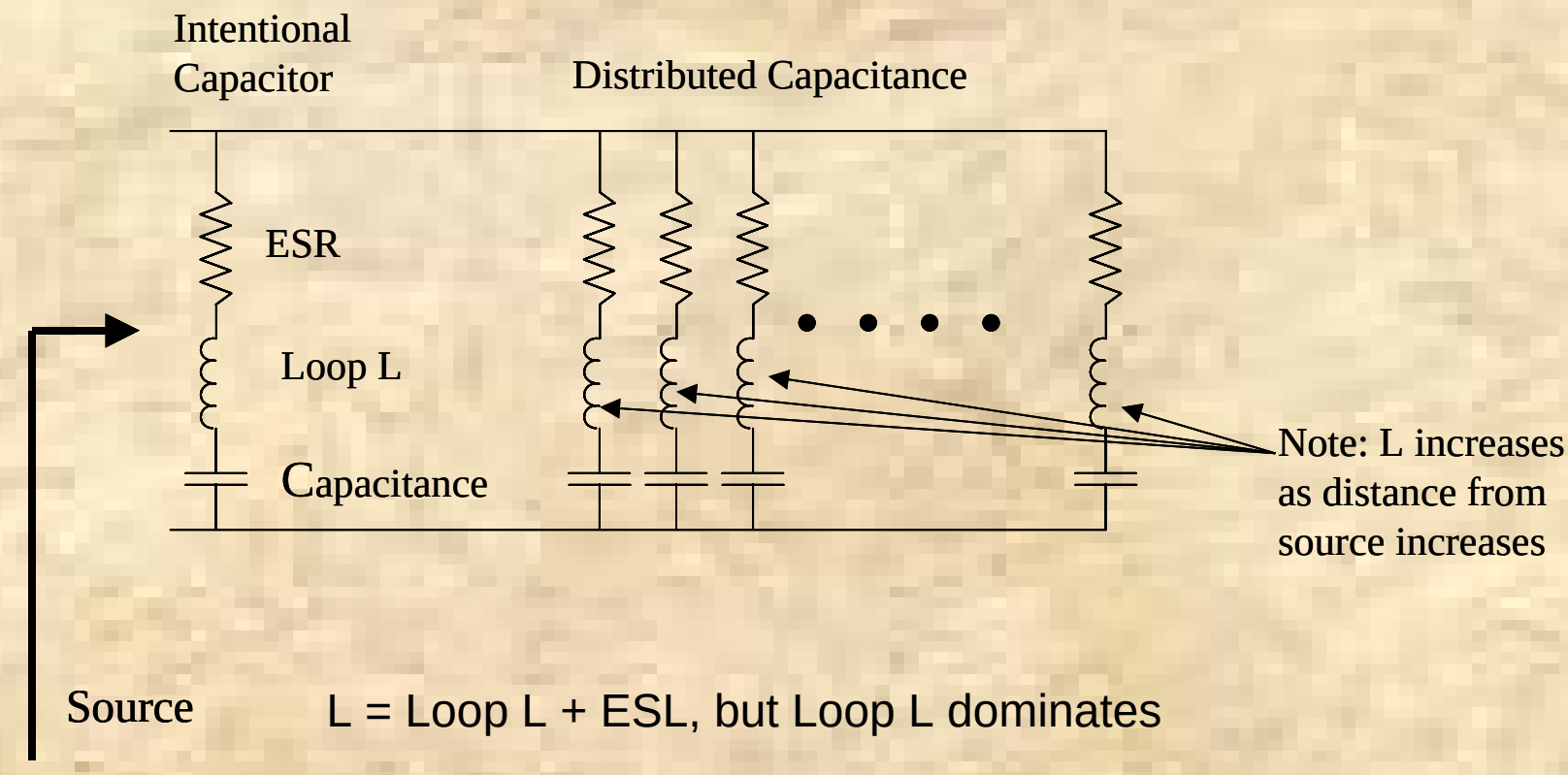


Over Estimates L and Ignores Distributed Capacitance

More Accurate Model Includes Distributed Capacitance



Distributed Capacitance Schematic



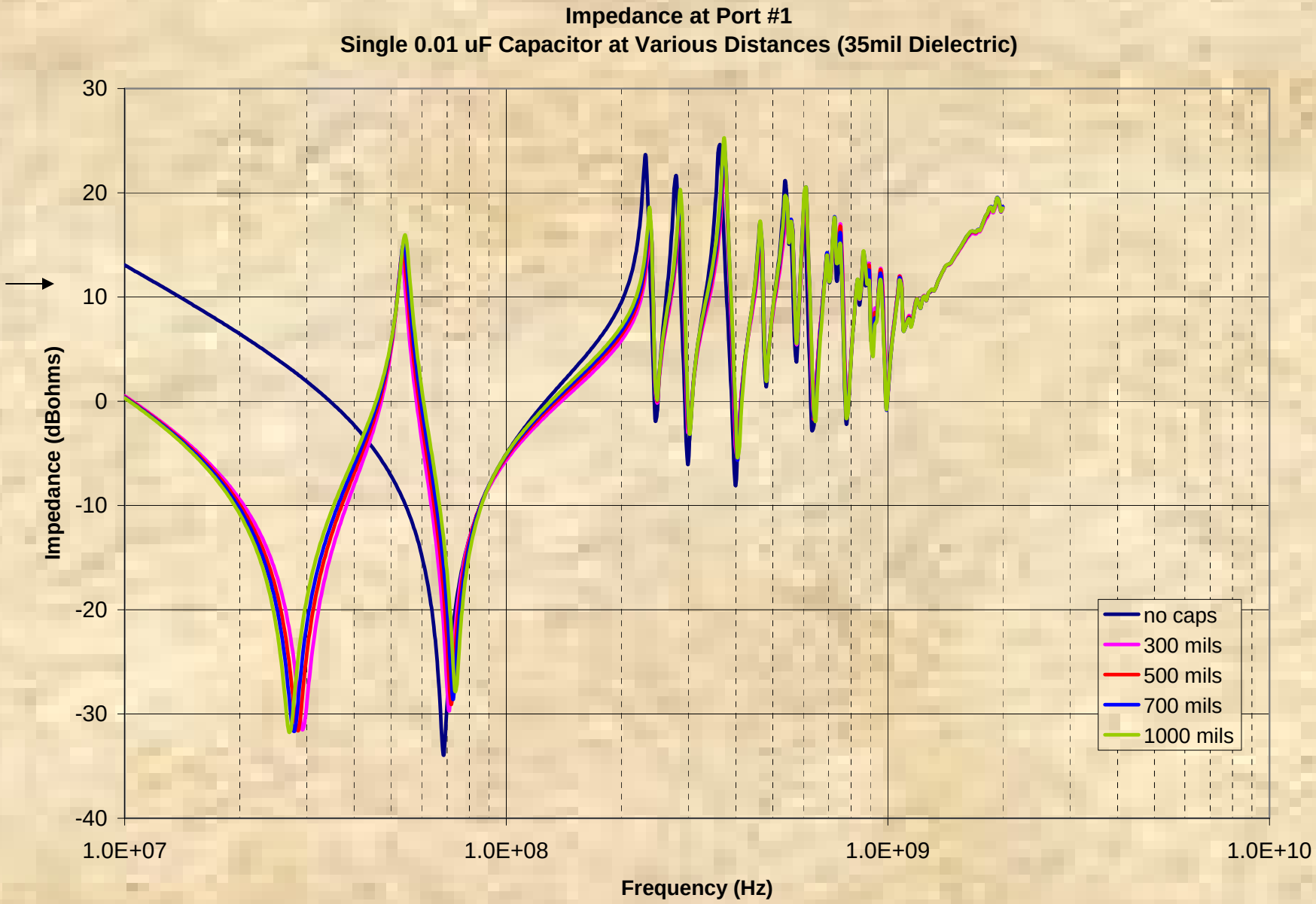
L = Loop L + ESL, but Loop L dominates

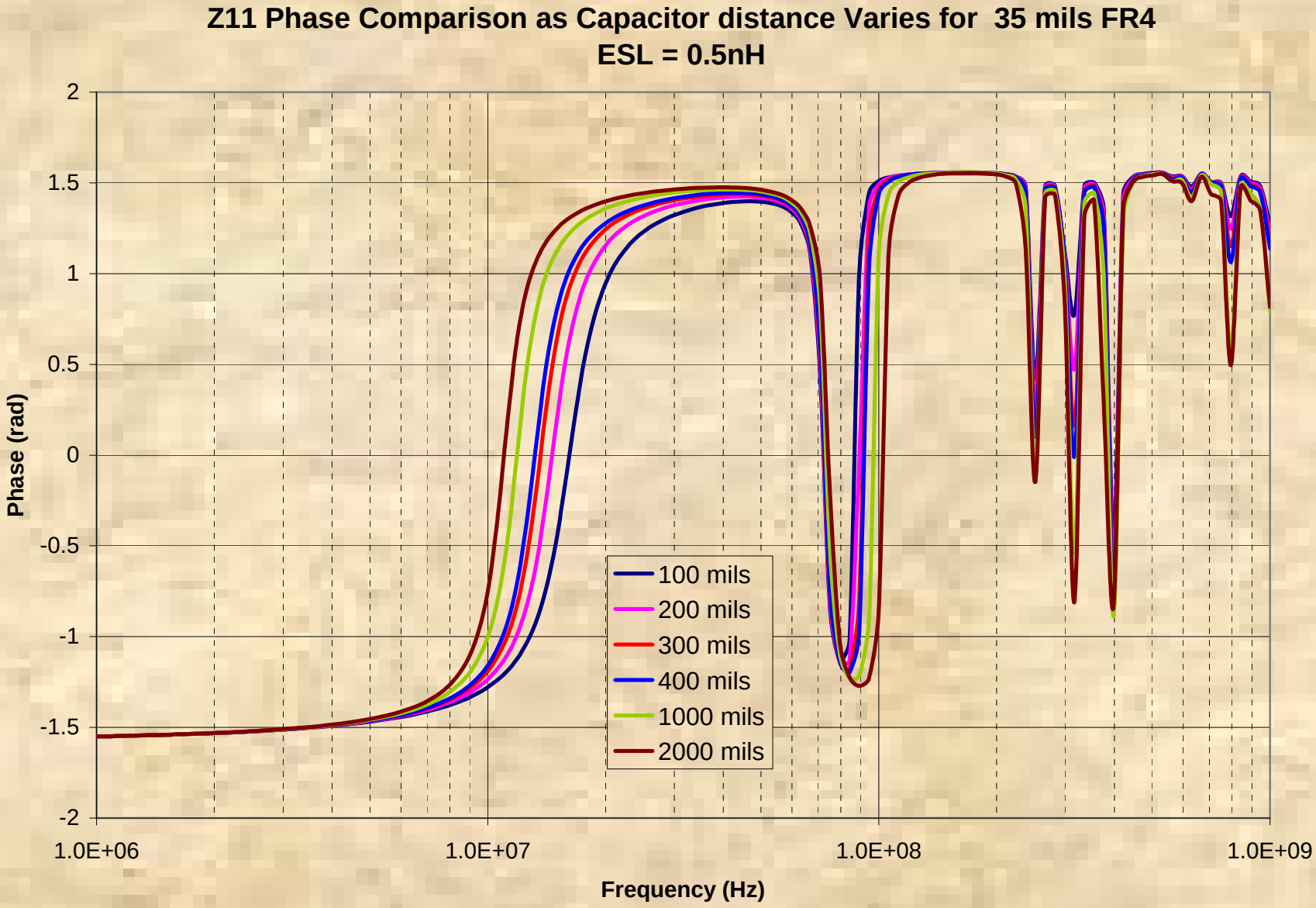
Effect of Distributed Capacitance

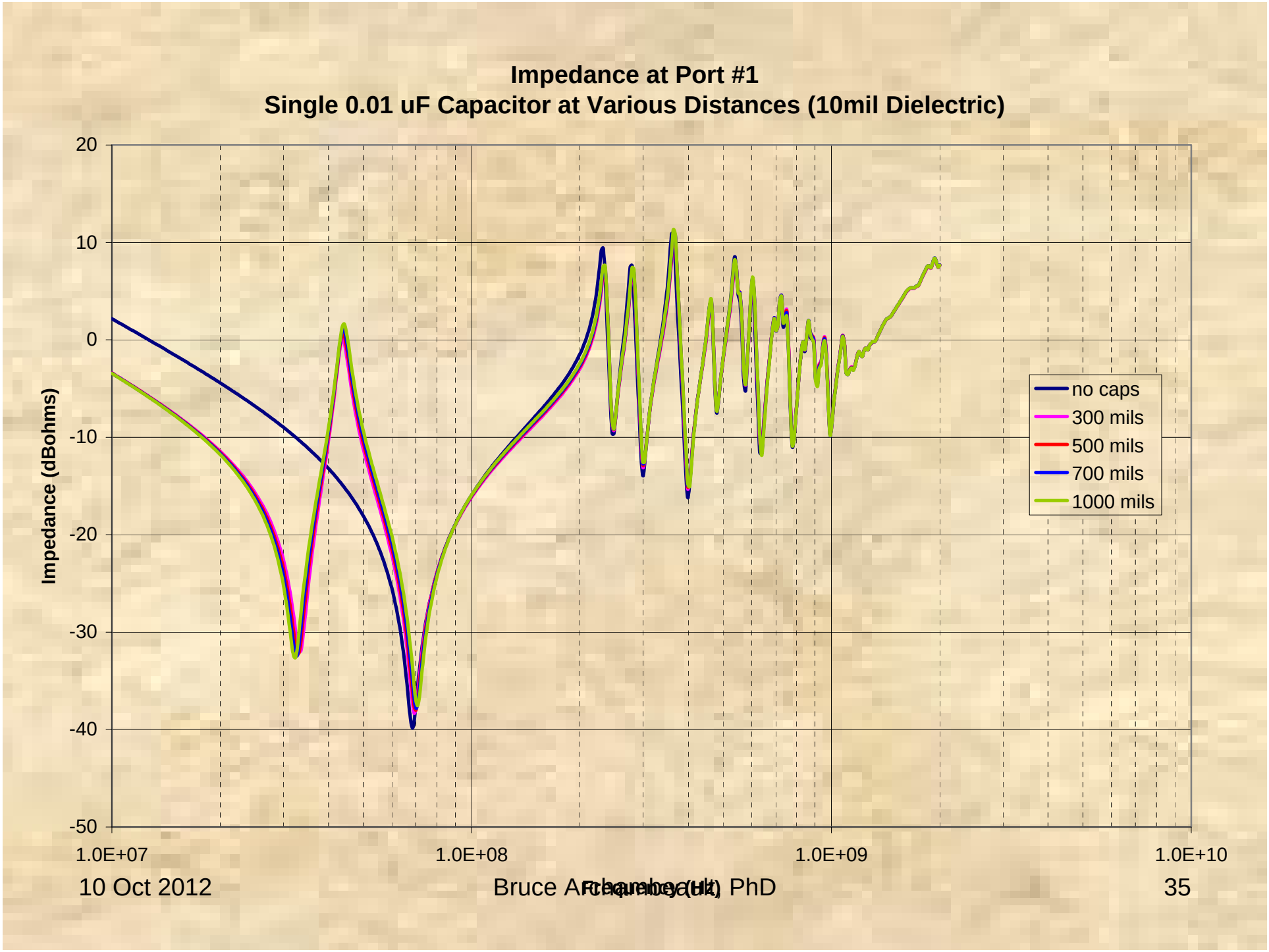
- Can NOT be calculated/estimated using traditional capacitance equation – need to use full-wave technique
- Displacement current amplitude changes with position and distance from the source

Sample Parameters for Comparison to Measurements

- Dielectric thickness = 35 mils
- Dielectric constant = 4.5, Loss tan = 0.02
- Copper conductivity = 5.8 e7 S/m


Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (35mil Dielectric)
Impedance (dBohms)
30
20
10
0
-10
-20
-30
-40
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
no caps
300 mils
500 mils
700 mils
1000 mils


Z11 Phase Comparison as Capacitor distance Varies for 35 mils FR4
ESL = 0.5nH
Phase (rad)
2
1.5
1
0.5
0
-0.5
-1
-1.5
-2
1.0E+06
1.0E+07
1.0E+08
1.0E+09
Frequency (Hz)
100 mils
200 mils
300 mils
400 mils
1000 mils
2000 mils


Impedance at Port #1
Single 0.01 uF Capacitor at Various Distances (10mil Dielectric)
Impedance (dBohms)
20
10
0
-10
-20
-30
-40
-50
1.0E+07
1.0E+08
1.0E+09
1.0E+10
Frequency (Hz)
no caps
300 mils
500 mils
700 mils
1000 mils

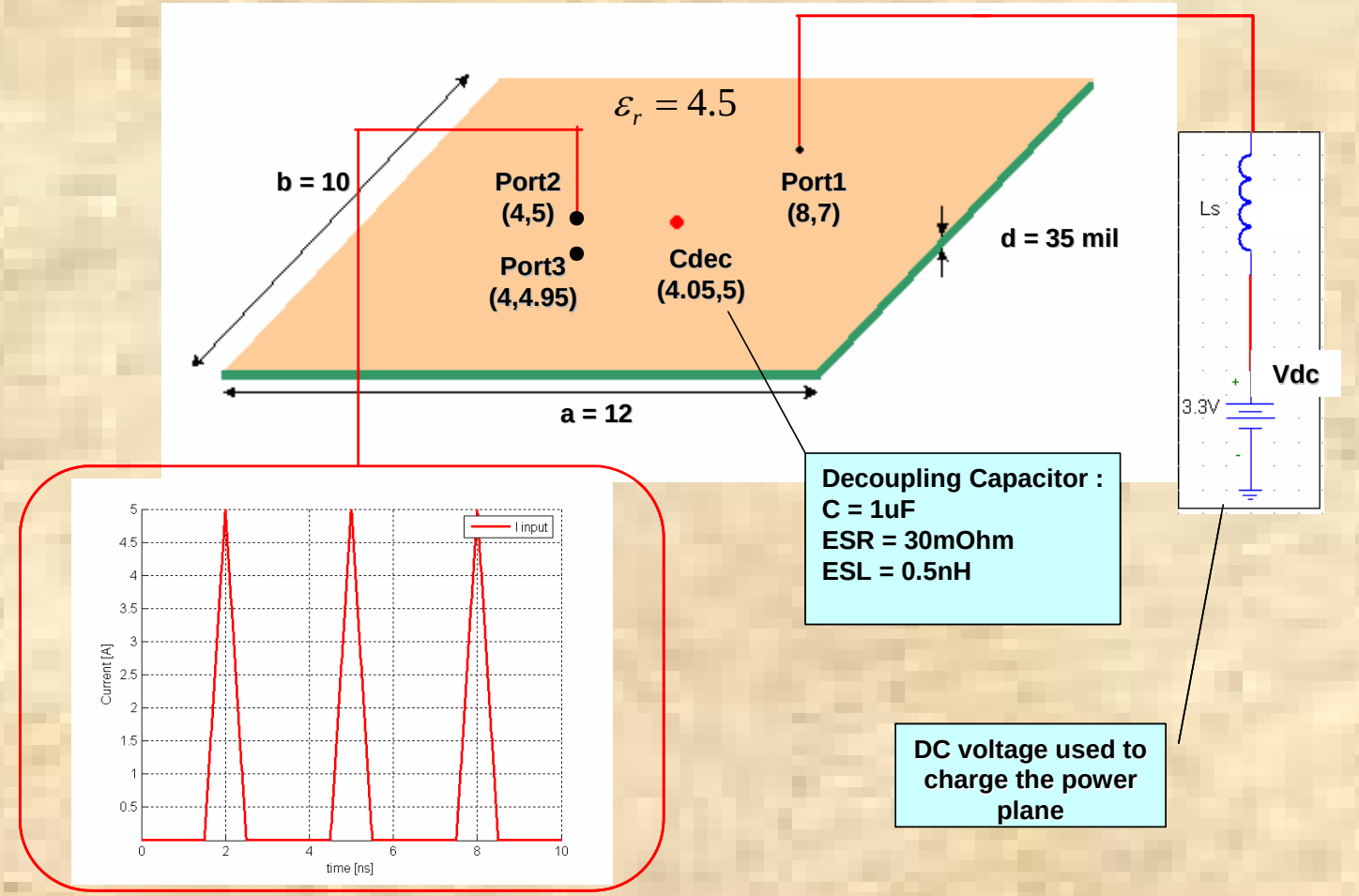
Effect of Capacitor Value??

- Need enough charge to supply need
- Depends on connection inductance

Charge Depletion

- IC draws charge from planes
- Capacitors will re-charge planes
  - Location ***does*** matter!

Model for Plane Recharge Investigations



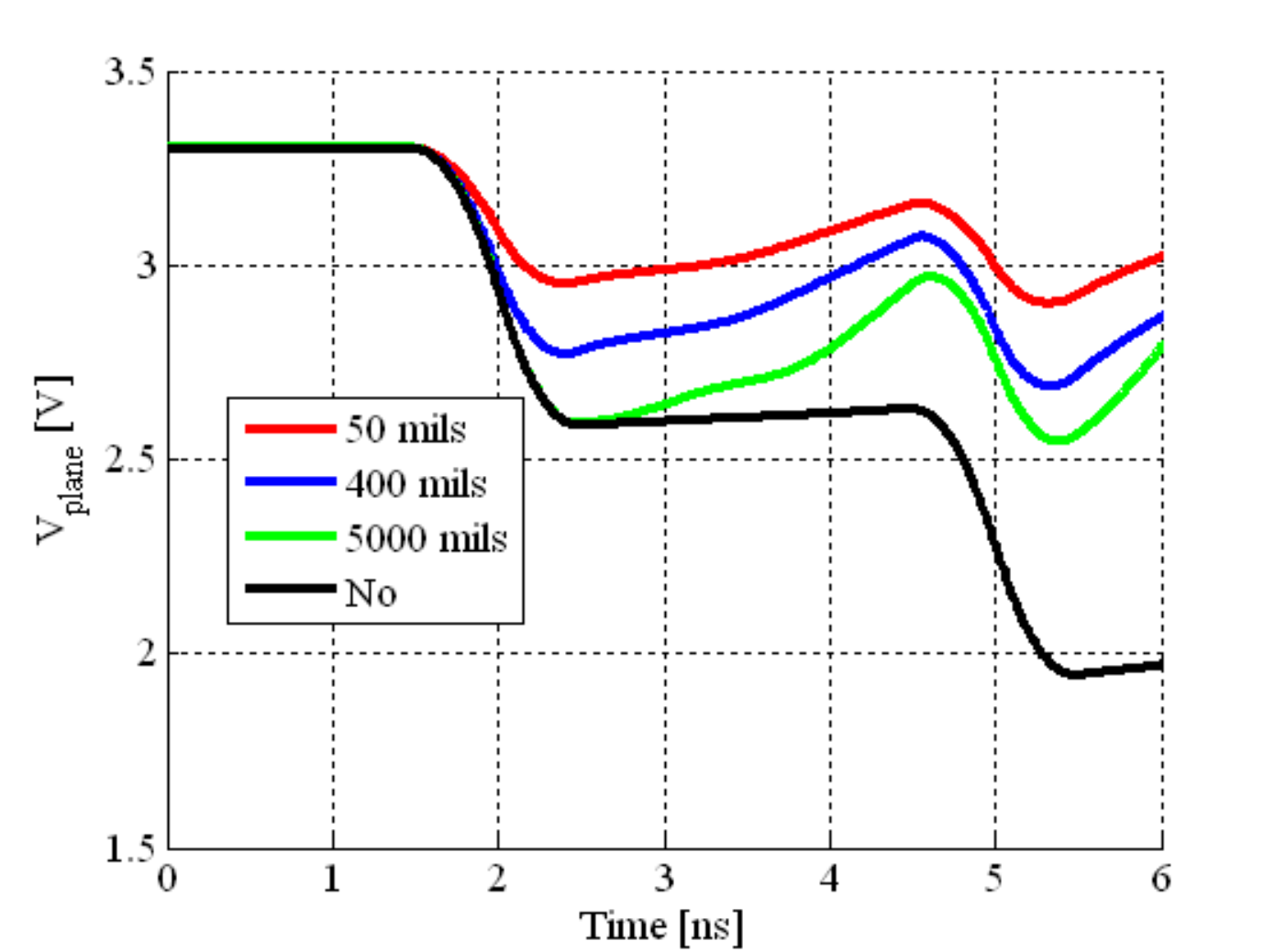
Port 2 represents IC current draw

Charge Between Planes vs. Charge Drawn by IC

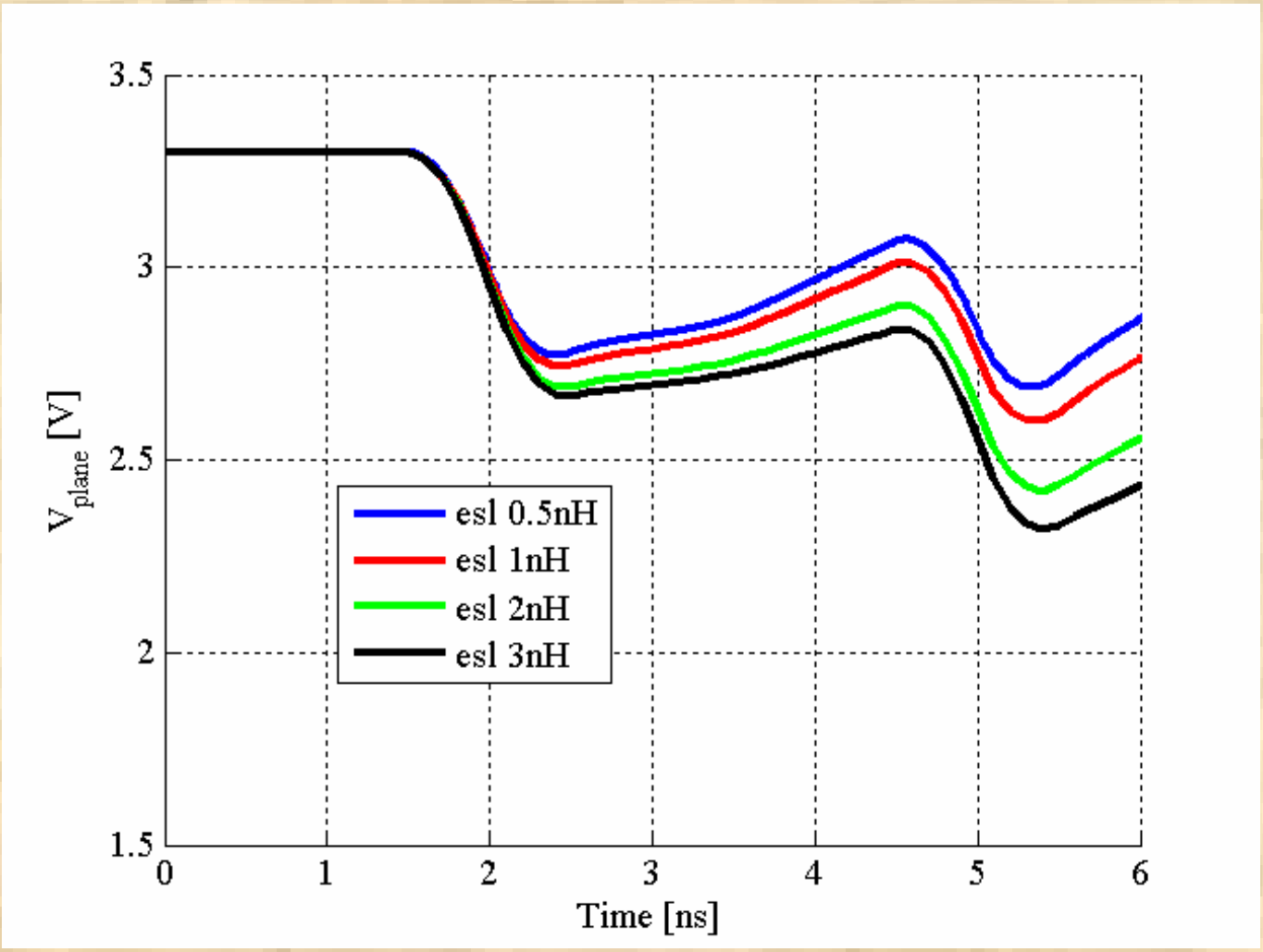
Board total charge : C*V = 3.5nF*3.3V = 11nC

Pulse charge 5A peak : I*dt/2 = (1ns*5A)/2=2.5nC

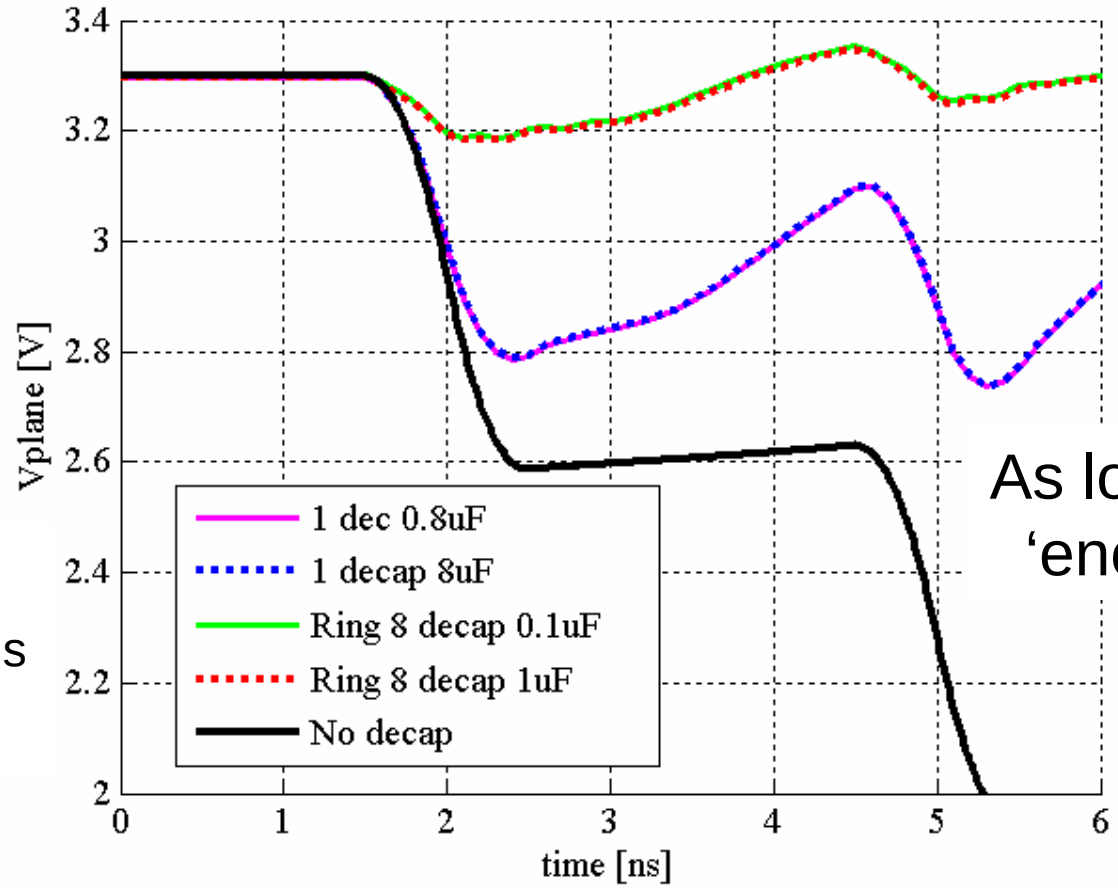
Charge Depletion vs. capacitor distance



Charge Depletion for Capacitor @ 400 mils for various connection Inductance



Noise Voltage is INDEPENDENT of Amount of Capacitance!



Dist=400 mils

ESR=30mOhms

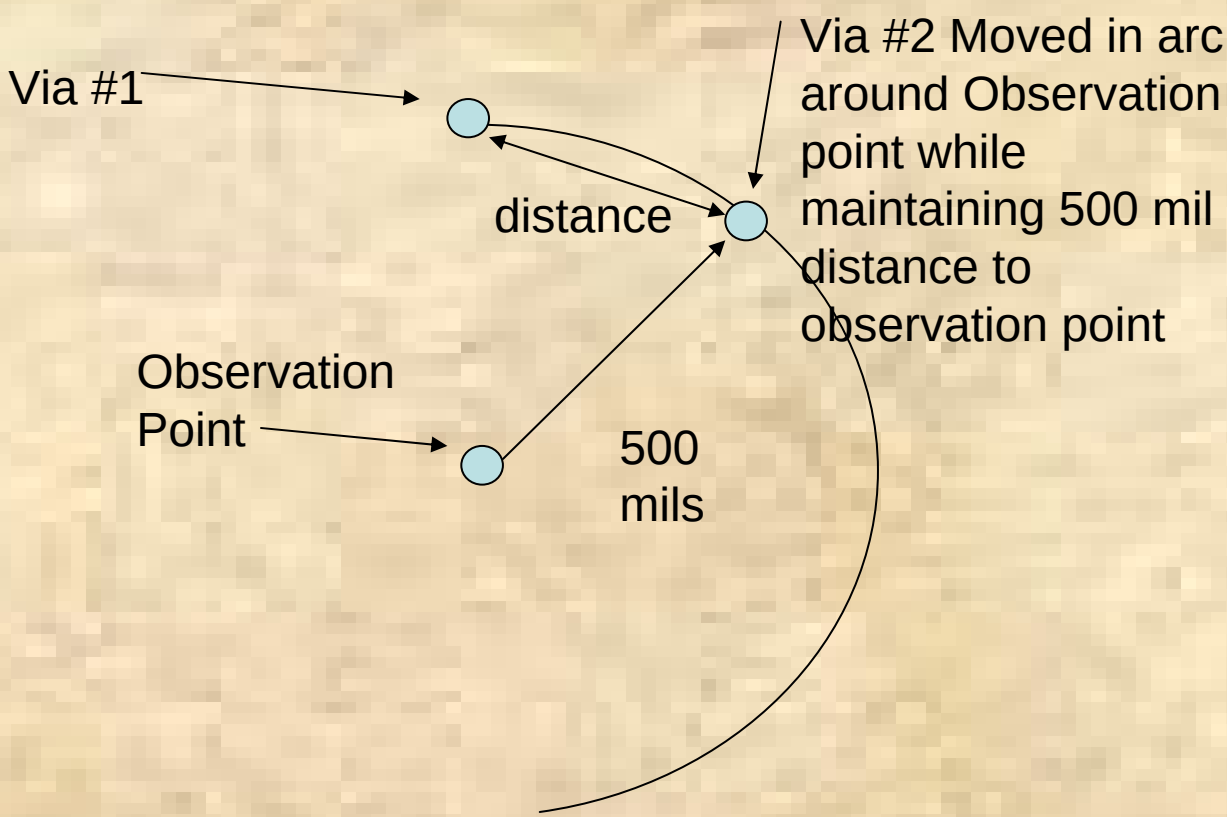
ESL=0.5nH

As long as there is 'enough' charge

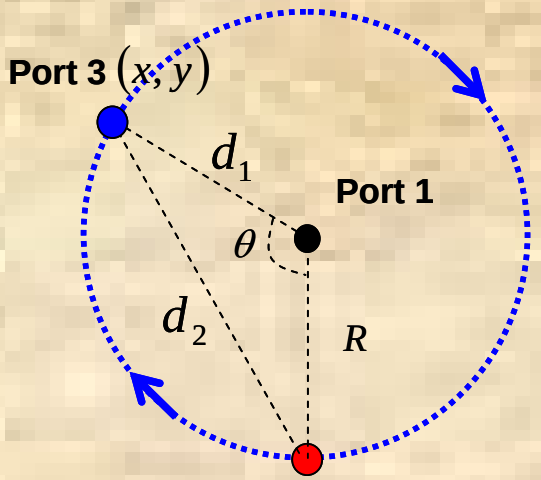
Capacitor Locations and Orientation

- Many myths about decoupling capacitor design
- Proximity between capacitors has been shown to impact capacitors' performance
- Wish to quantify these various effects, not just show which is best
- Current (not voltage) important for decoupling capacitor analysis

What Happens if a 2nd Decoupling Capacitor is placed near the First Capacitor?



Second Via Around a circle



$d_1 = R$

$d_2 = 2R\sin\frac{\theta}{2}$

$$\frac{\mu d}{4\pi}\ln\left(\frac{(R+r)^2(d_1+r)^2}{r^3(d_2+r)}\right)-\frac{\mu d}{4\pi}\frac{\ln^2\left(\frac{d_1+r}{R+r}\right)}{\ln\left(\frac{d_2+r}{r}\right)}$$

$$=\frac{\mu d}{4\pi}\ln\left(\frac{(R+r)^4}{(2R\sin(\theta/2)+r)r^3}\right)$$

R: distance between Port 1 and Port 2 in mil

r: radius for all ports in mil

d: thickness of dielectric layer in mil

d1: distance between Port 3 and Port 1 in mil

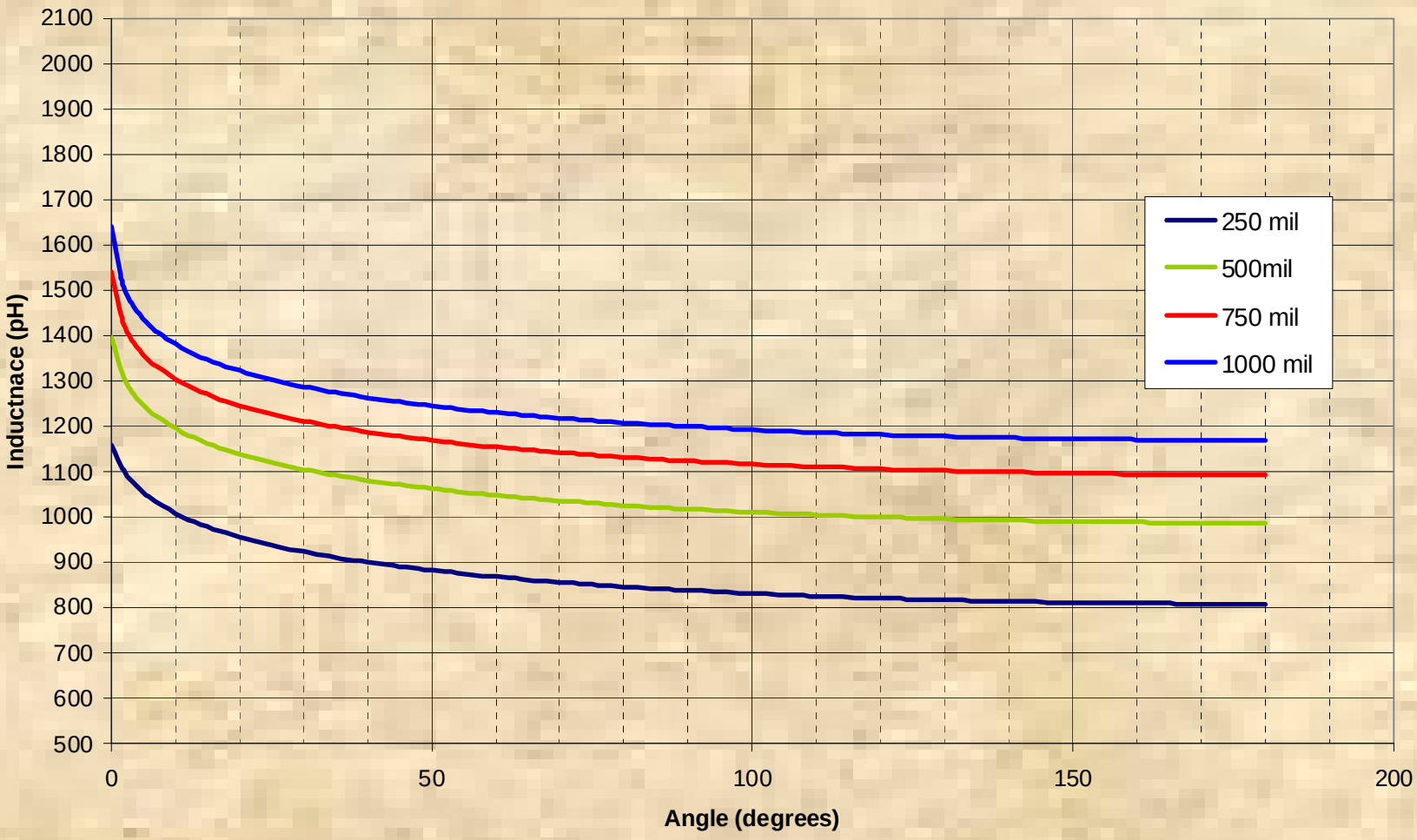
d2: distance between Port 2 and Port 3 in mil

theta: angle as shown in the figure in degree

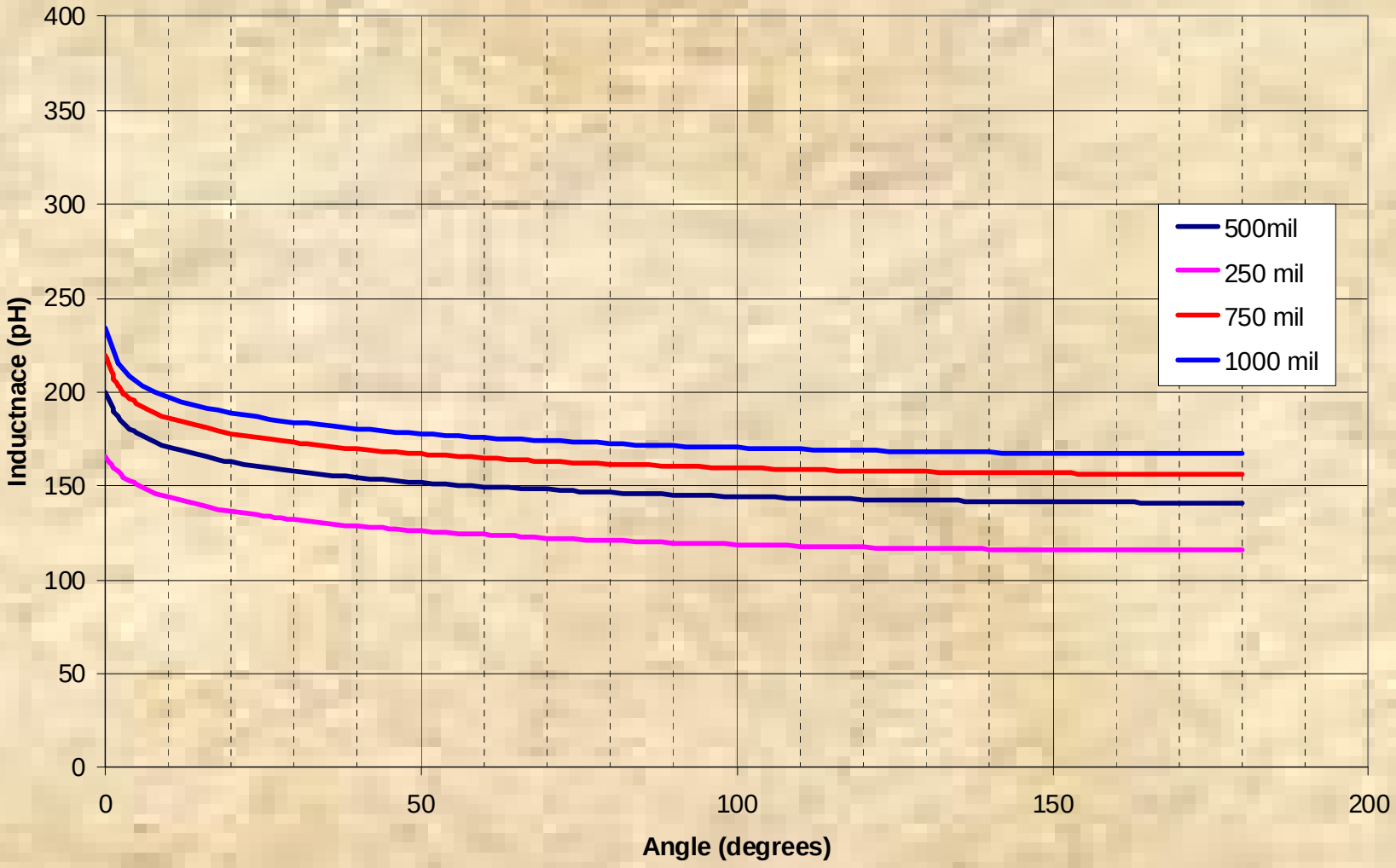
Courtesy of Jingook Kim, Jun Fan, Jim Drewniak

Missouri University of Science and Technology

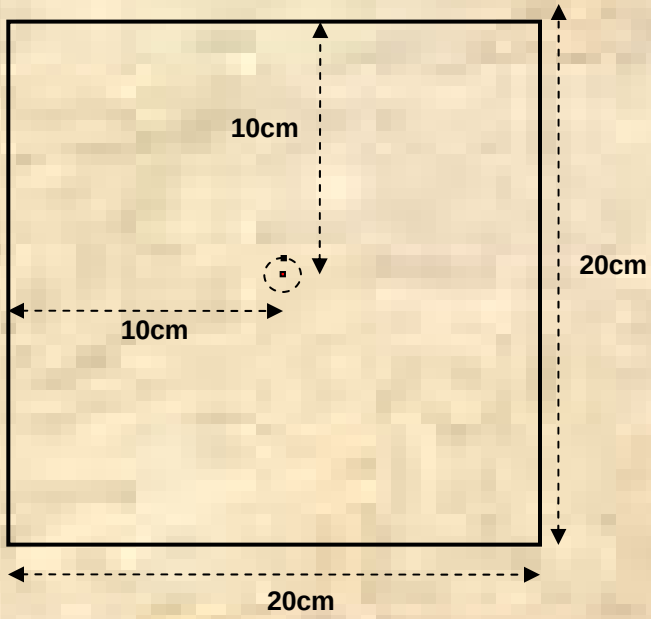
Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 35 mil -- Via Diameter = 20 mil



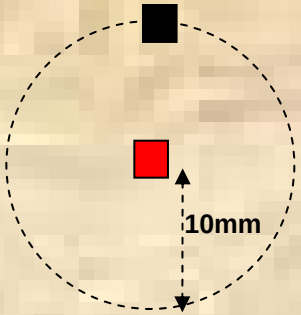
Effective Inductance for Various Distances to Decoupling Capacitor
With Second Capacitor (Via) Equal Distance Around Circle
Plane Seperation = 5 mil -- Via Diameter = 20 mil



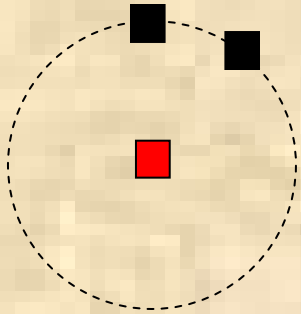
Understanding Inductance Effects and Proximity



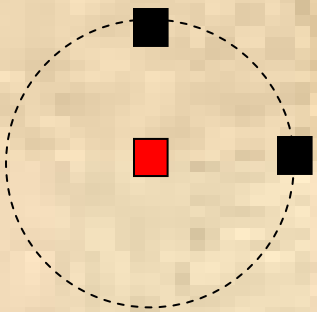
1 via



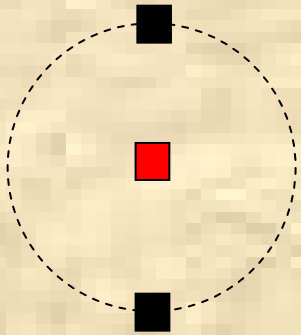
2 via with degree 30°



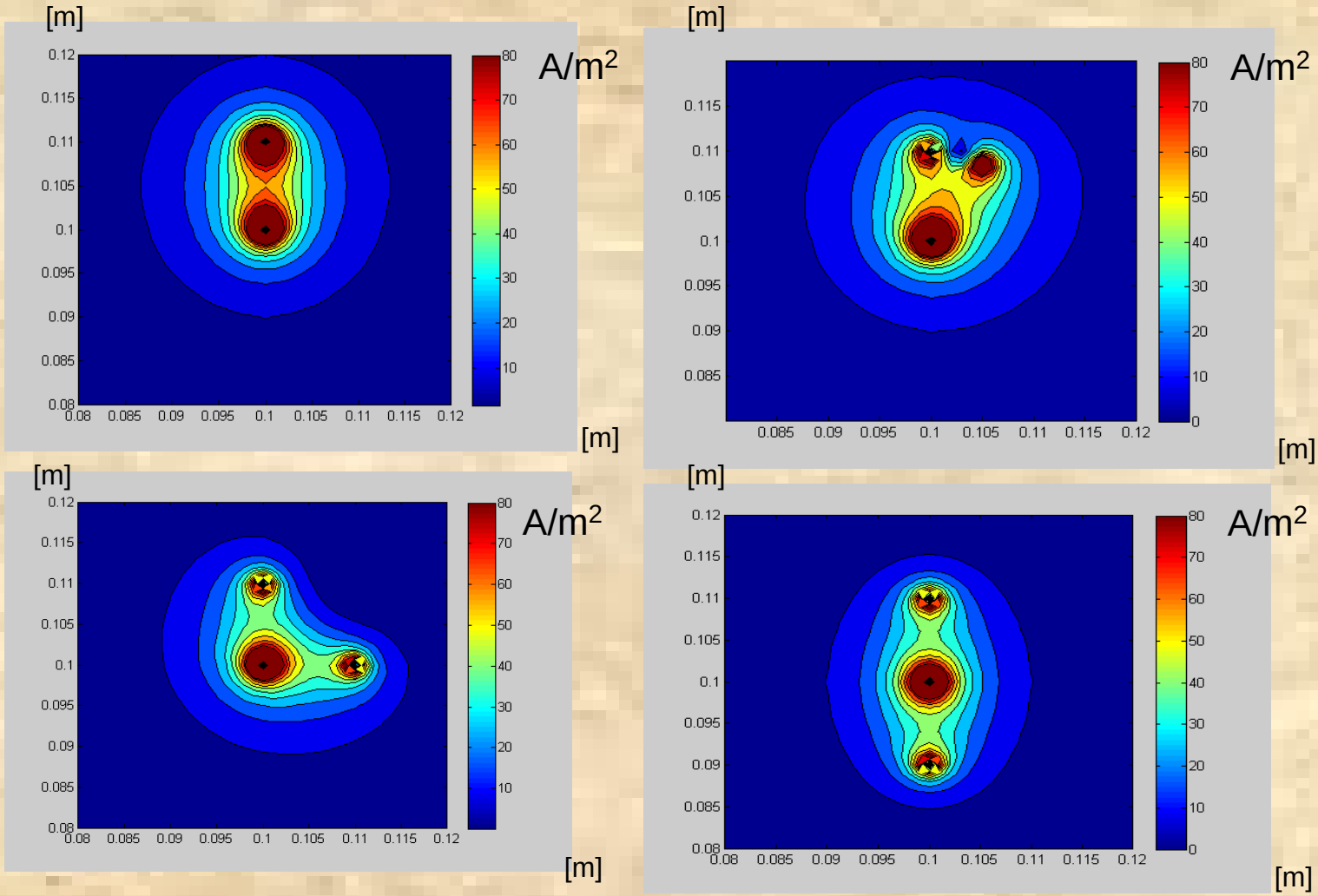
2 via with degree 90°



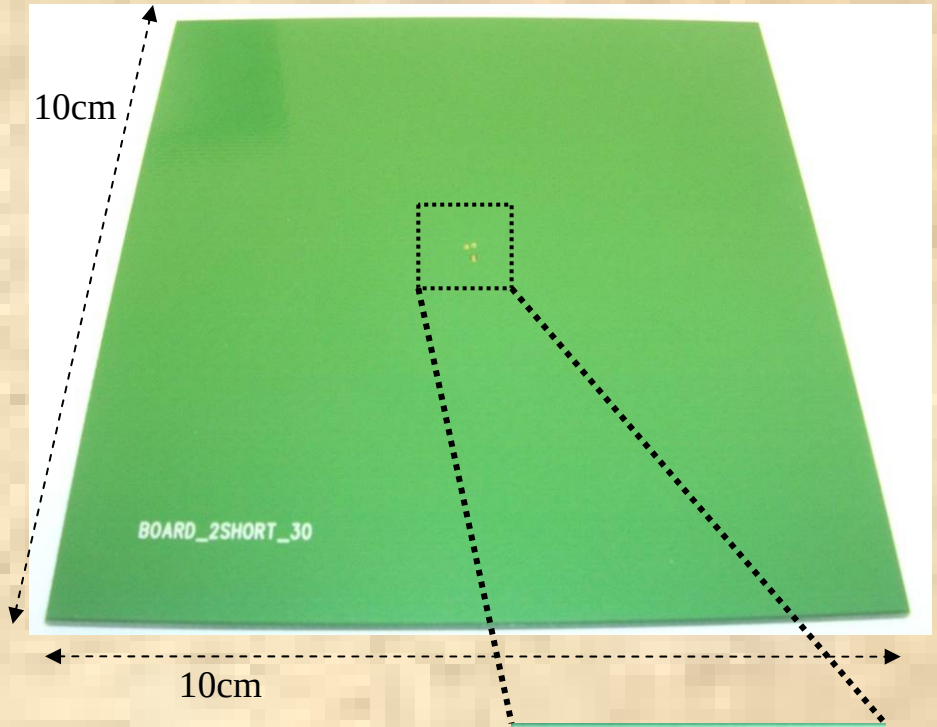
2 via with degree 180°

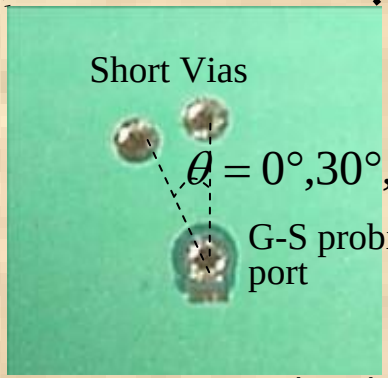


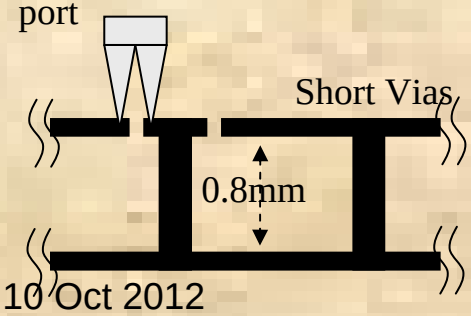
Current Density - simulation

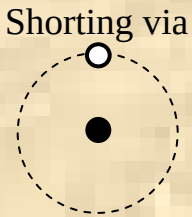


DUT for Experimental Validation (Single Plane pair)



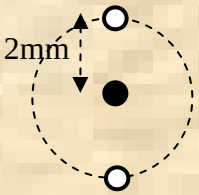






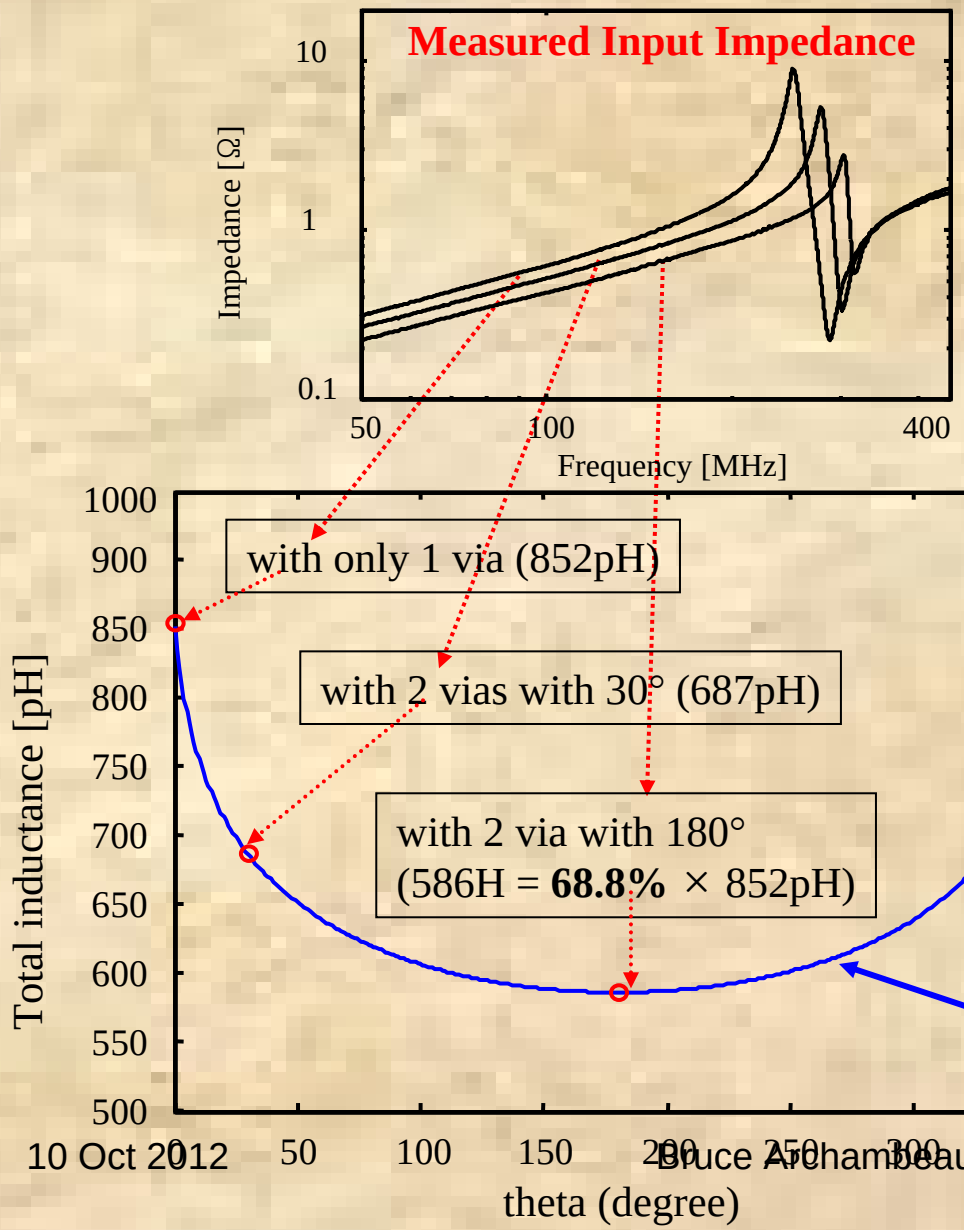
1 shorting

2 shorting with 30°



2 shorting with 180°

Experimental Validation (Single Plane Pair)



- Even in the case with two shorting vias at opposite sides (θ=180°), the inductance value is 68.8% of that with one shorting via
- As two shorting vias get closer together, mutual inductance between two shorting vias increases.

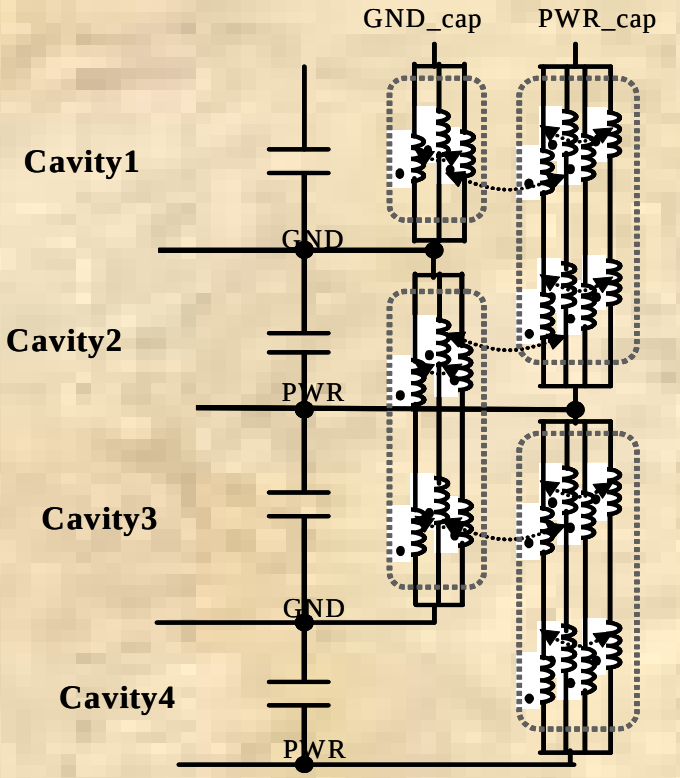
$$\frac{\mu d}{4\pi}\ln\left(\frac{(R+r)^4}{(2R\sin(\theta/2)+r)r^3}\right)$$

Equation

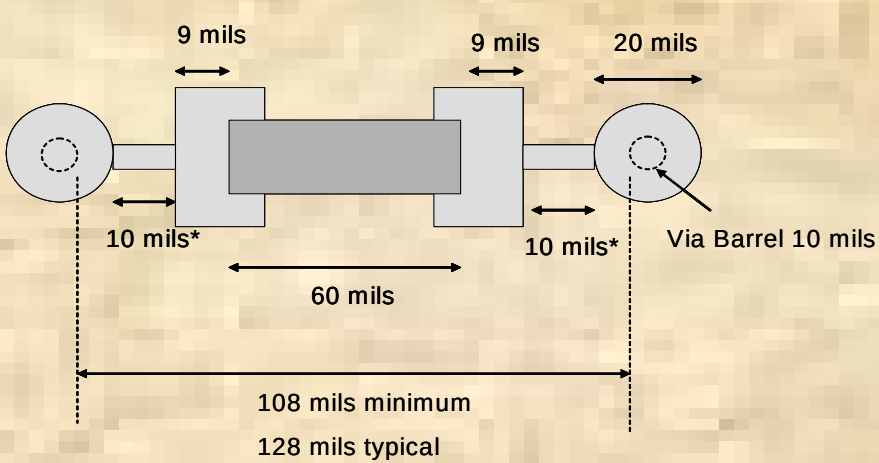
Observations

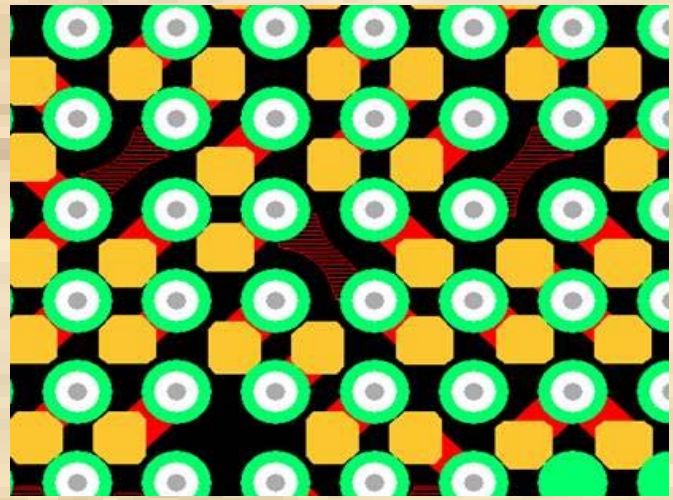
- Added via (capacitor) does not lower effective inductance to 50%
  - 70-75% of original single via case
- Thicker dielectric results in higher inductance

Multiple Capacitors



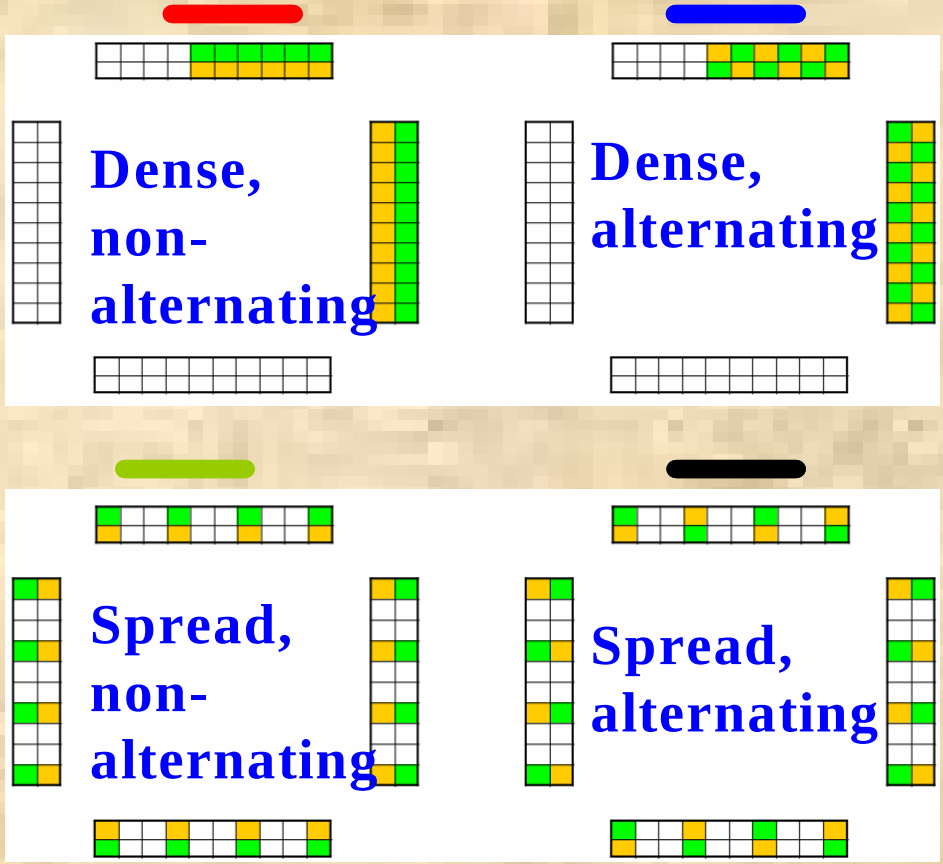
Via Spacing

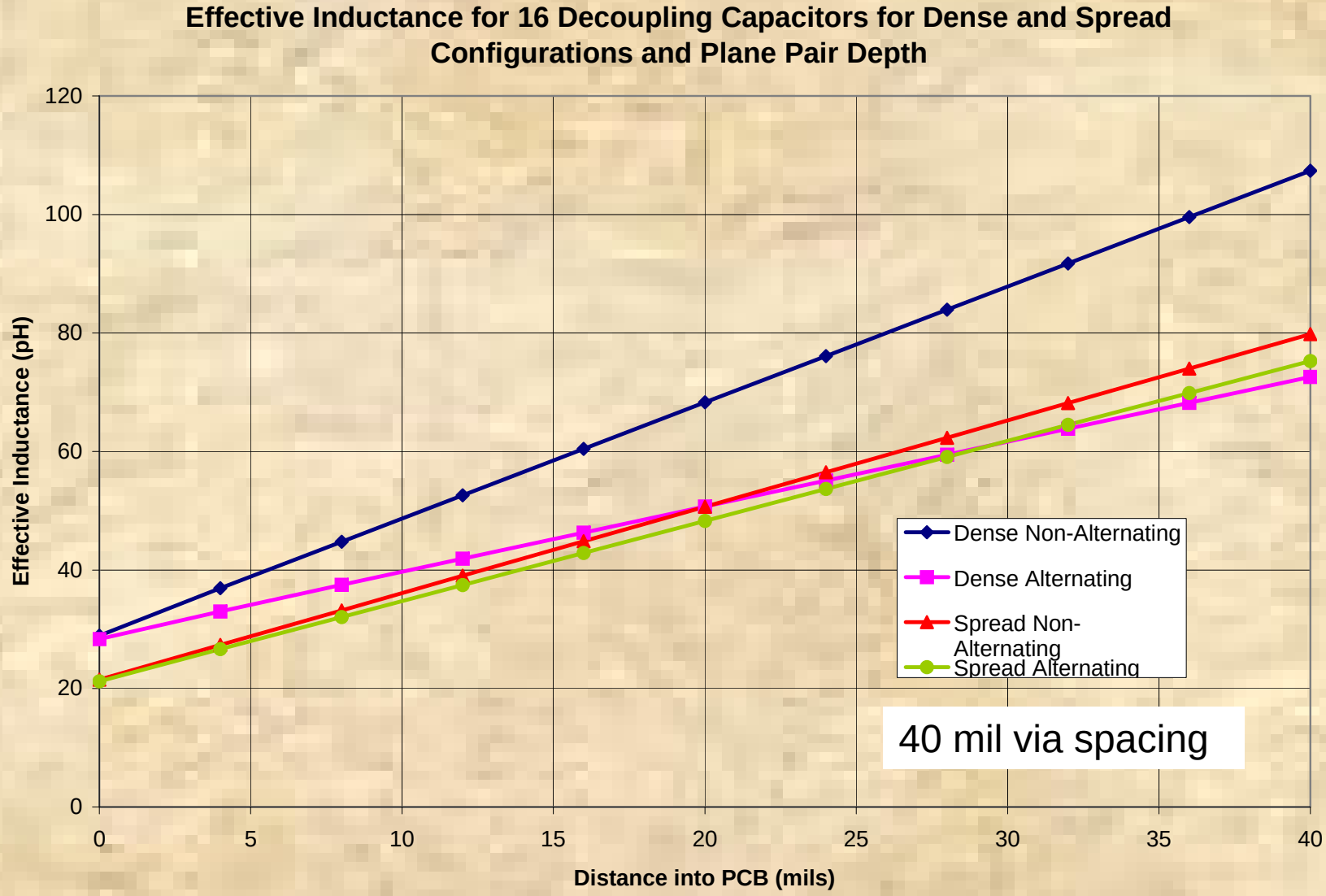




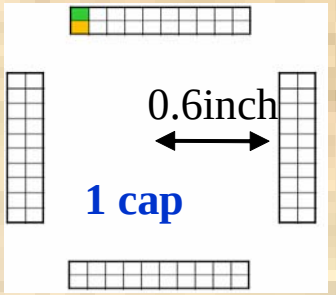
Distance to Planes (mils)	40 mil Spacing (nH)	0402 SMT (nH)	0603 SMT (nH)
10	0.3	0.9	1.1
20	0.5	1.3	1.6
30	0.75	1.6	1.9
40	0.95	1.9	2.2

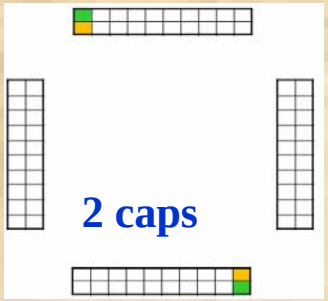
Possible Configurations

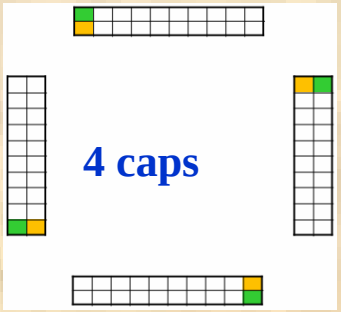


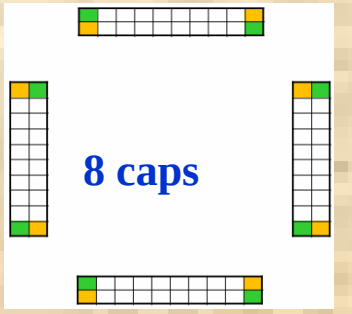

Effective Inductance for 16 Decoupling Capacitors for Dense and Spread Configurations and Plane Pair Depth
Effective Inductance (pH)
120
100
80
60
40
20
0
0
5
10
15
20
25
30
35
40
Distance into PCB (mils)
Dense Non-Alternating
Dense Alternating
Spread Non-Alternating
Spread Alternating
40 mil via spacing

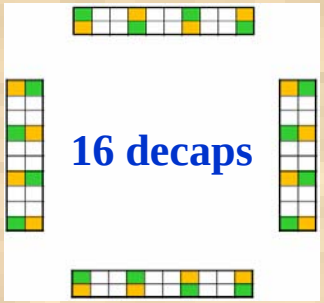
Number of Capacitors

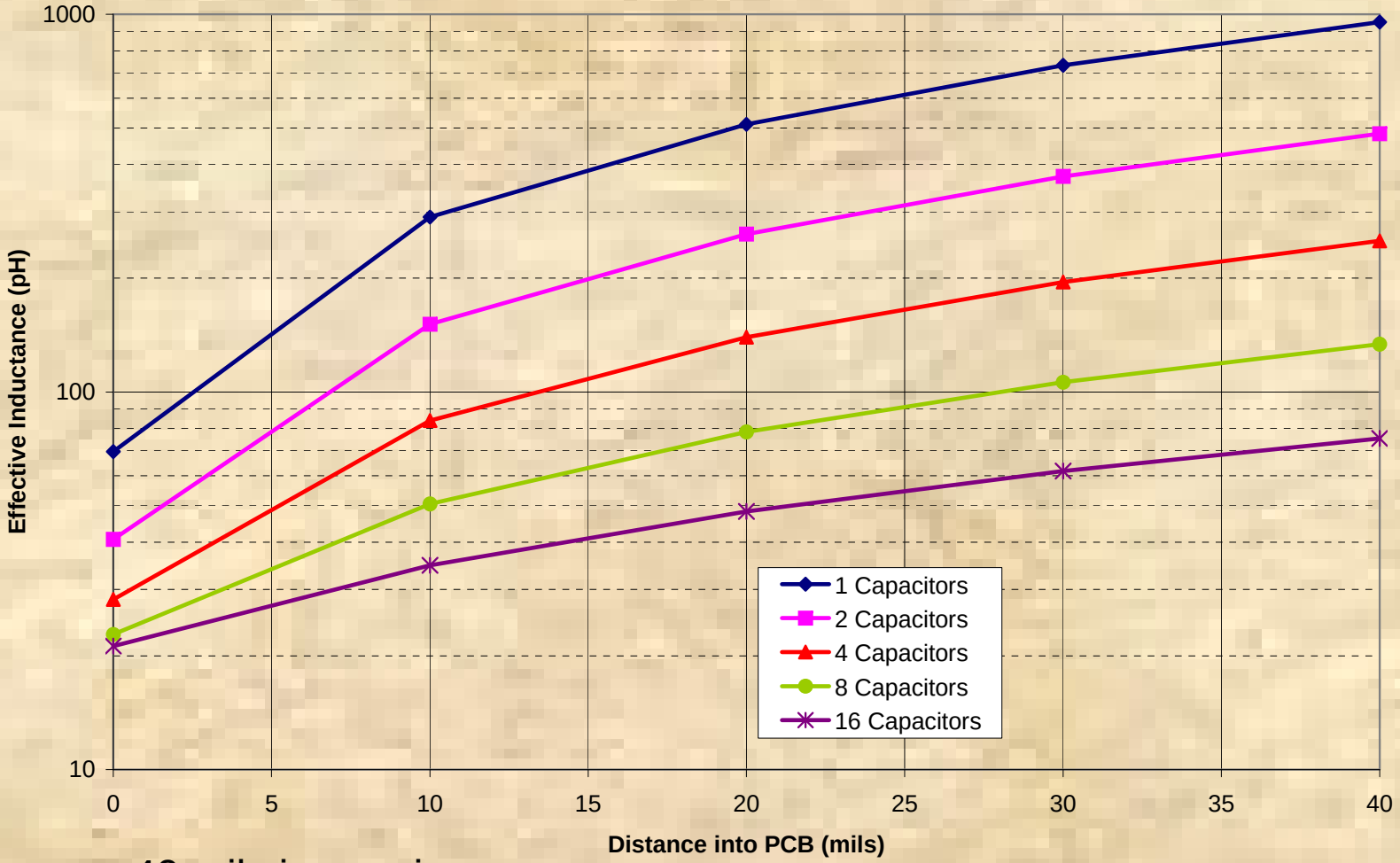










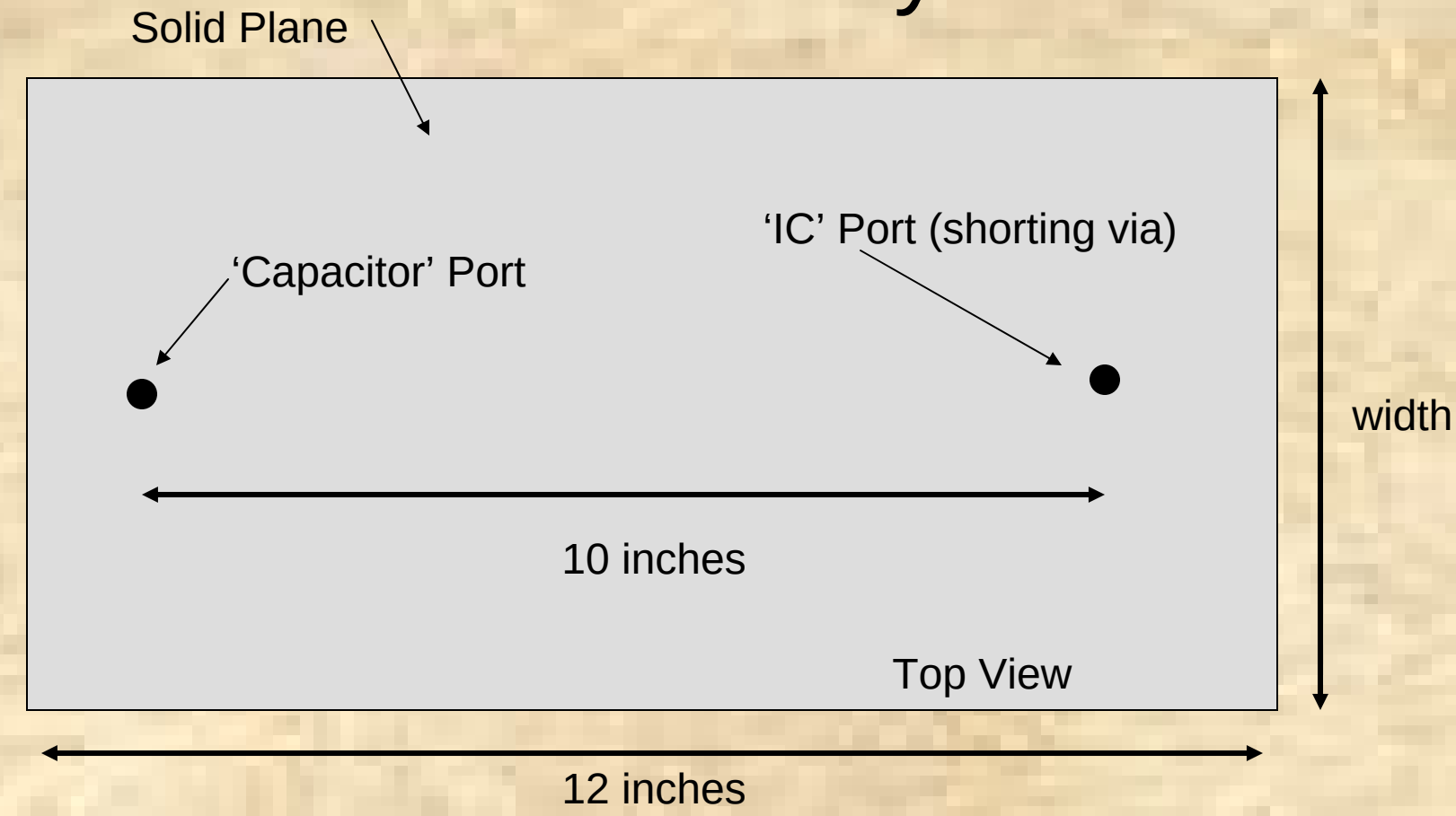


40 mil via spacing

Inductance vs. Plane Width

- Current tends to spread to minimize the impedance
- What is the effect of narrow power/ground planes?
- Using PowerPEEC in quasi-static inductance extraction mode
- Plane widths of 10”, 5”, 2” and 1”
- Distance between planes = 10 mils

Geometry


Solid Plane
'IC' Port (shorting via)
'Capacitor' Port
width
10 inches
Top View

12 inches

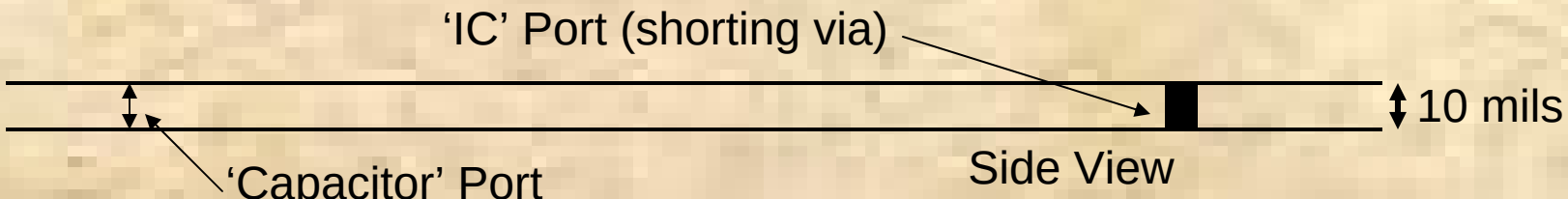

'IC' Port (shorting via)
10 mils
'Capacitor' Port
Side View

Table 1 Inductance as a Function of Plane Width

Plane Width (inches)	Inductance (pH)
10	545
5	709
2	1352
1	2574

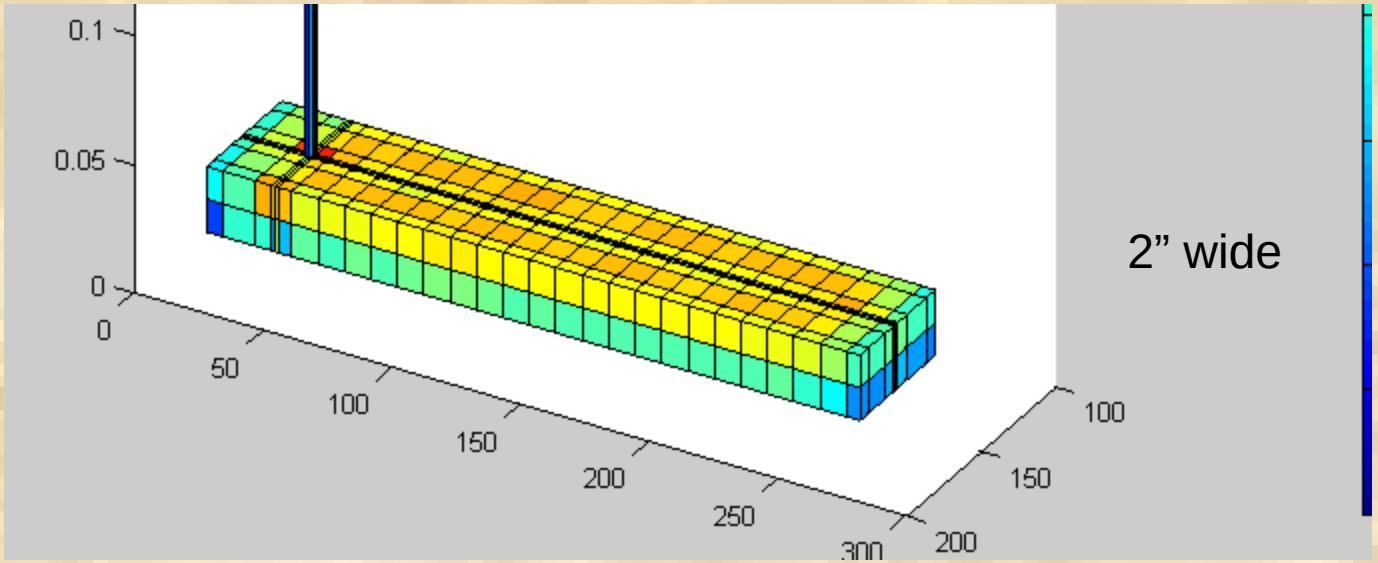
Effect of distance between Capacitor and IC

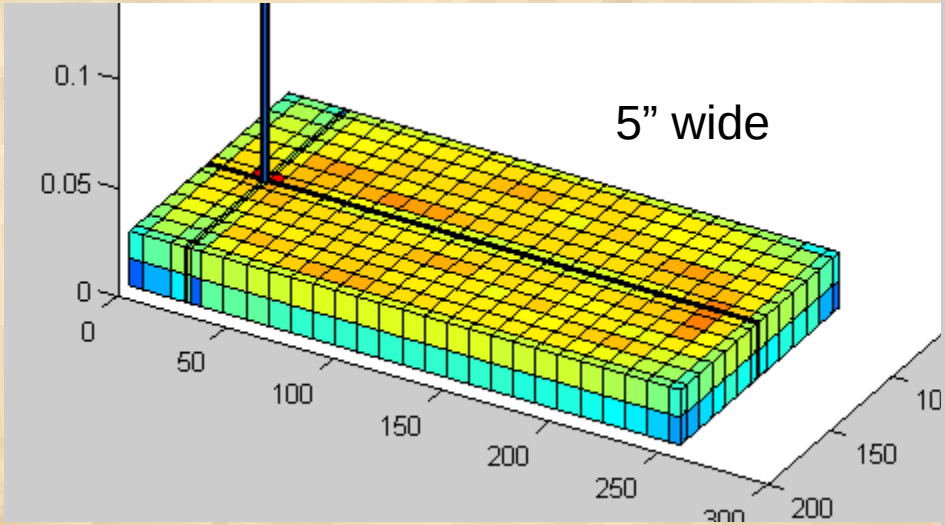
- Initially used 10” now use 2” and 1”
- Vary plane width as before

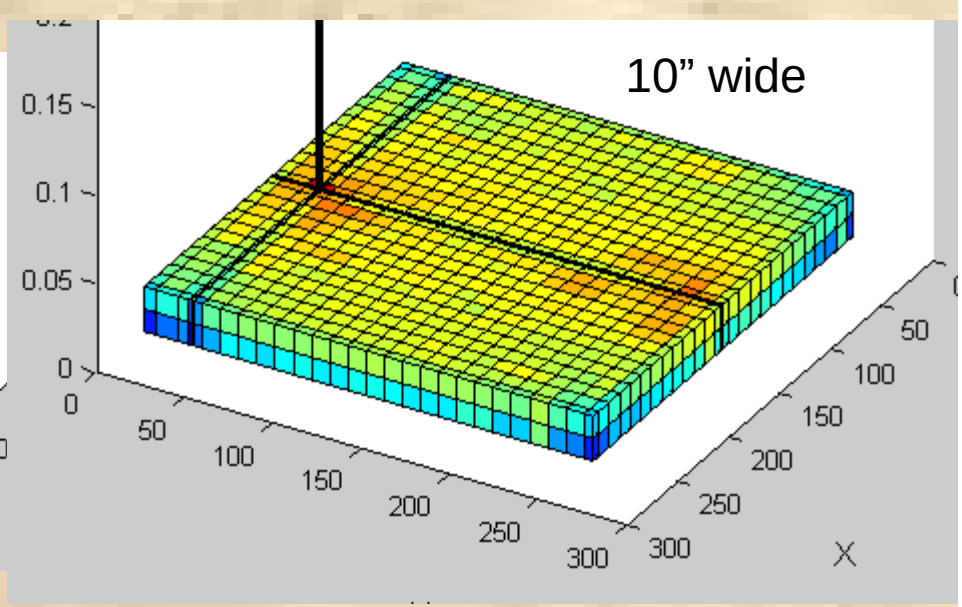
Table 2 Inductance as a Function of Plane Width

Plane Width (inches)	Inductance (pH) (Distance=10”)	Inductance (pH) (Distance=2”)	Inductance (pH) (Distance=1”)
10	545	173	154
5	709	178	156
2	1352	355	163
1	2574	658	240

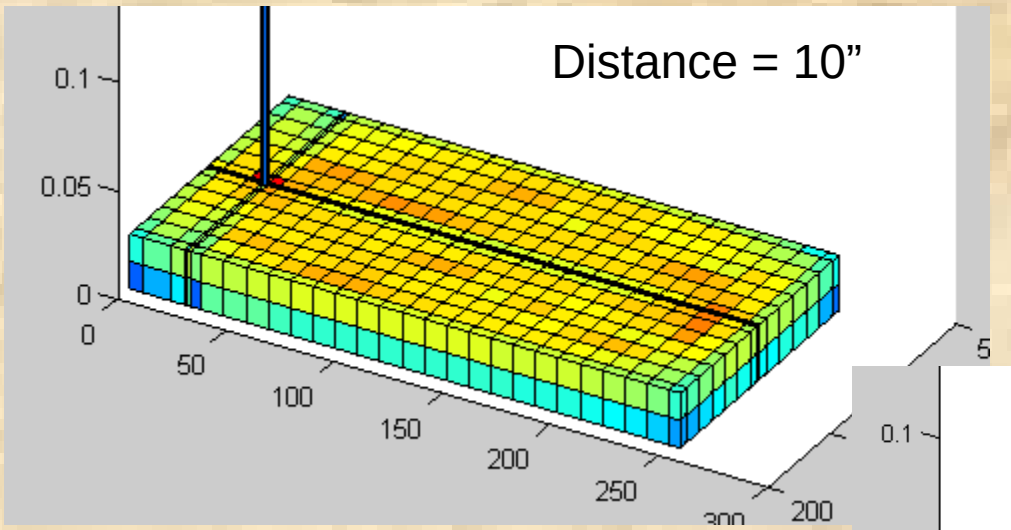
Current Density

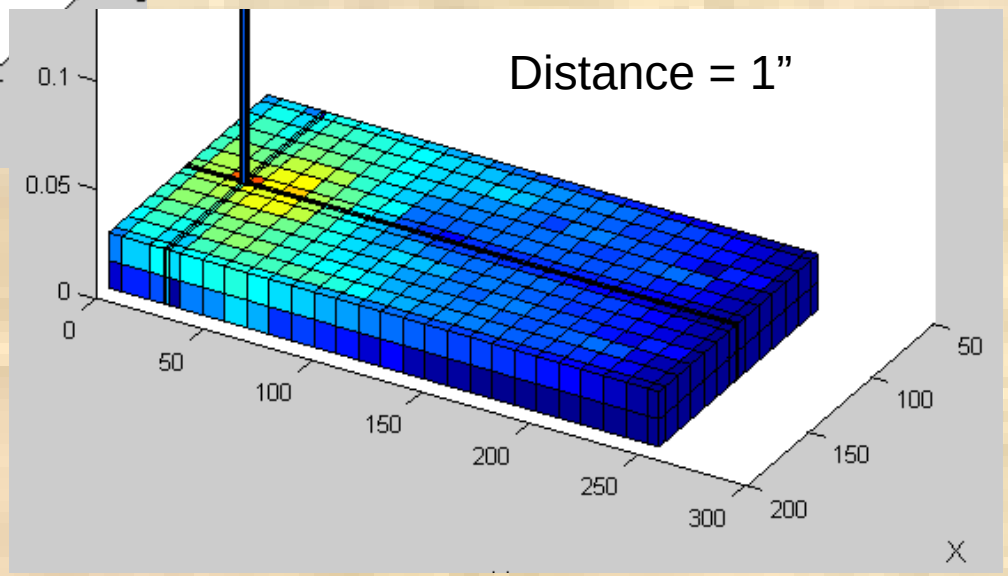




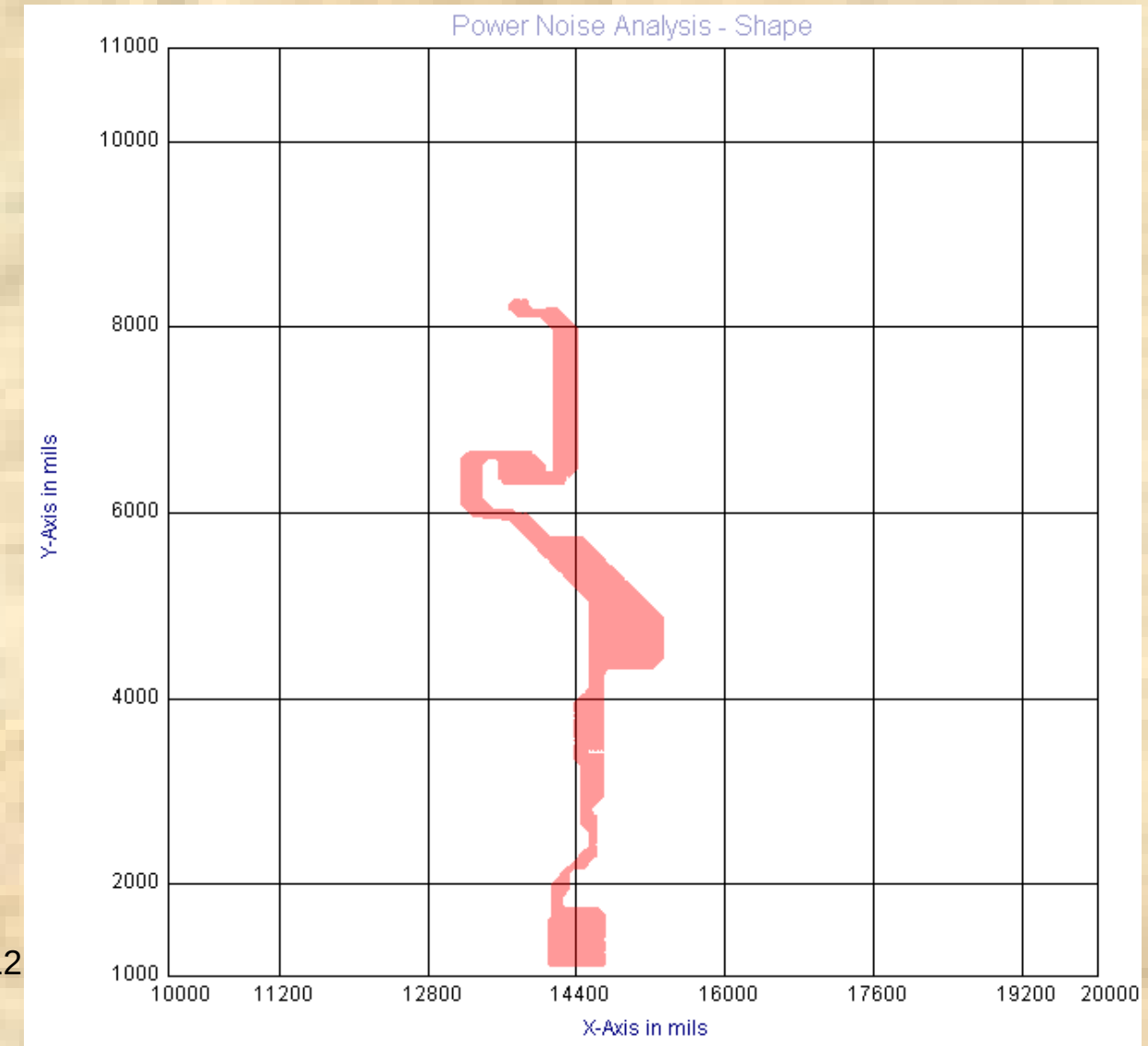


Current Spread Comparison Planes 5” Width





Really Ugly
From Actual PCB



Conclusions

- Inductance increases rapidly as plane width decreases
- Impact of plane width not as severe when capacitor and IC are close
- Should avoid all long thin power/ground structures

Summary

- Capacitance values should be as large as possible within the package size
- In most cases, IC takes charge from between the plates, capacitors replenish that charge
- Capacitors are better able to provide charge when spread out
- If placed near each other, capacitors should alternate power/ground pins
  - *Worst configuration* is when capacitors are close together and all pins in the same direction
- When plane pair is deep in PCB stackup, effective inductance is higher

Conventional Wisdom

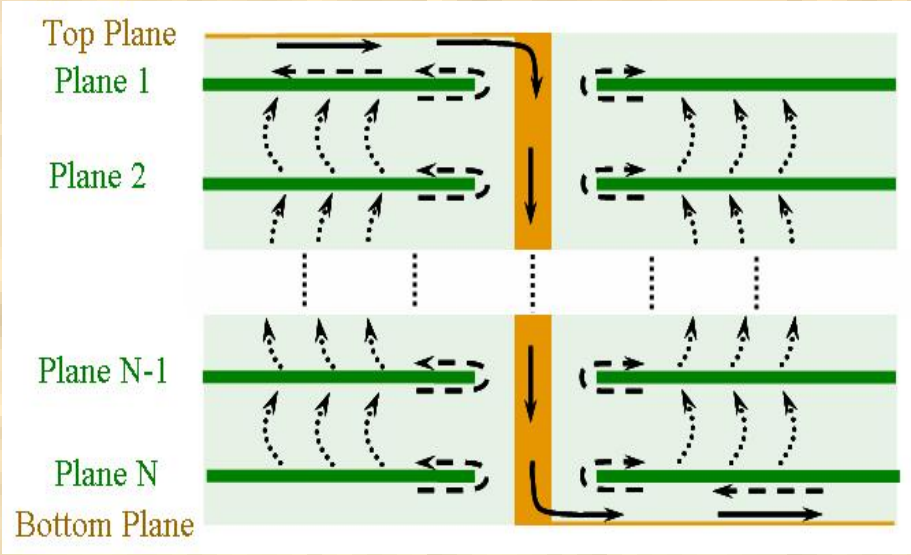
- ~~Need a variety of capacitance values to maintain low impedance over frequency range~~
- ~~Many capacitors of one value is better than many values~~
- Place capacitors close to ICs as possible
- ~~Location does not matter~~
- ~~Spread capacitors over entire board~~

Backup

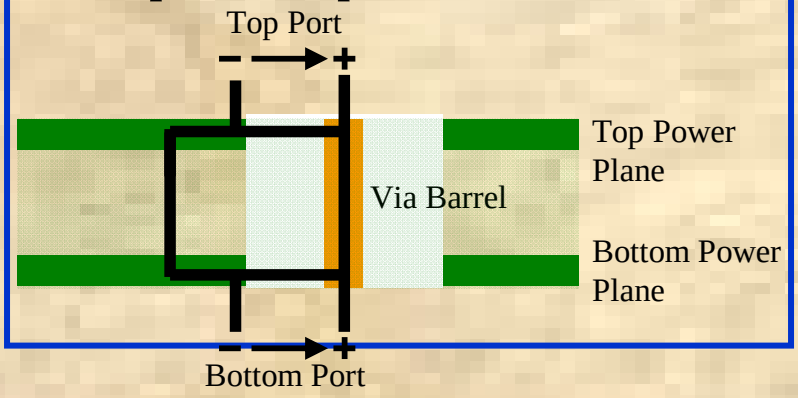
Modeling Technique

- Difficult to model many layer PCB with full wave models
- Multi-Via Transition Tool (MVTT)
  - Breaks multiple layers into individual via transitions
  - Cavity resonance technique to find impedance between planes
  - Capacitance calculation for via-to-plane effects
  - Concatenate S-parameters from all individual elements

Breaking the Problem



One via between a power plane: 2-port network



Via Configurations