

**Sources, Modes and Paths of  
Electrical Noise Generated  
by Switch Mode Power Supplies**

**February 21, 2008**

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**Dedicated to William S. Robinson - 'Bill'  
Sept 25, 1927 – Feb 21, 1998**



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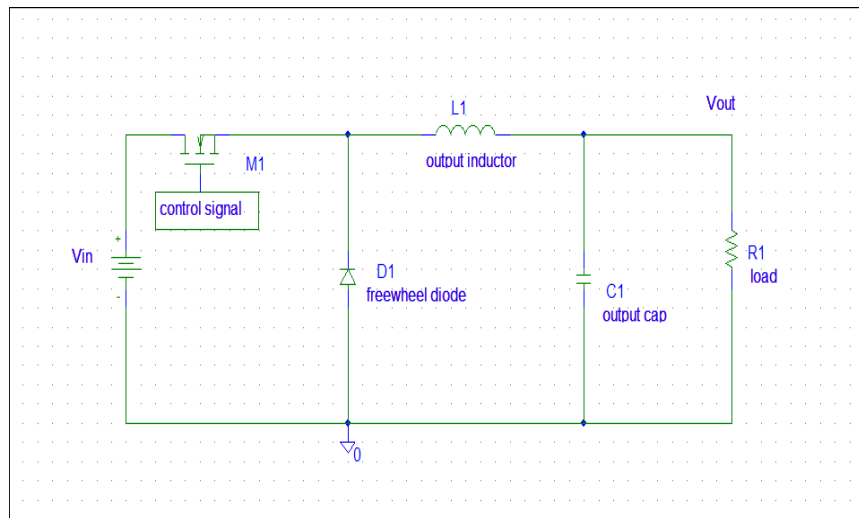
## Objectives

1. Introduce the fundamental mechanism of noise generation in switch-mode power supply circuits (SMPS).
2. Introduce and examine the impact of circuit and component parasitics on the generation and propagation of electrical noise in SMPS.
3. Discuss design considerations to minimize noise generation.
4. Discuss design considerations to minimize noise propagation
5. Examine PCB layout for switching power supplies

*This presentation will be more qualitative than quantitative.*

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## Ideal Buck Converter



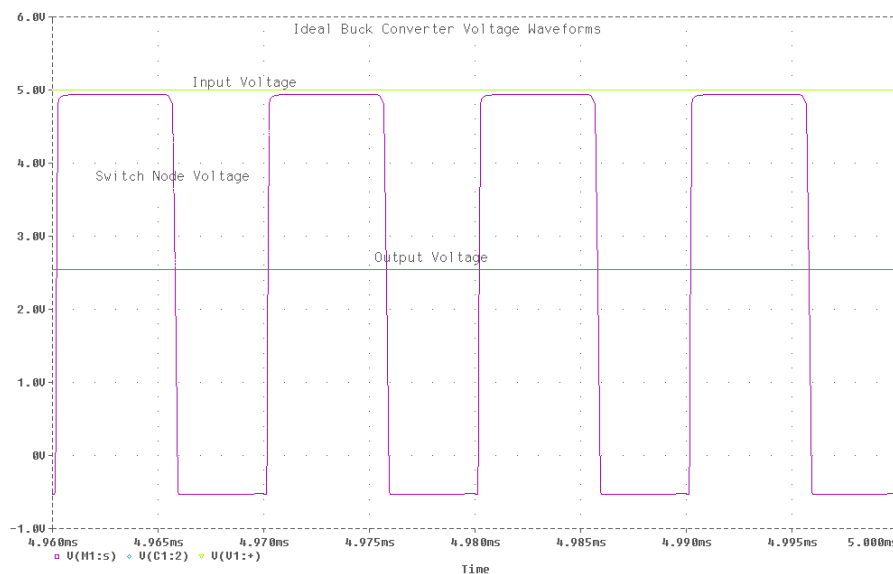
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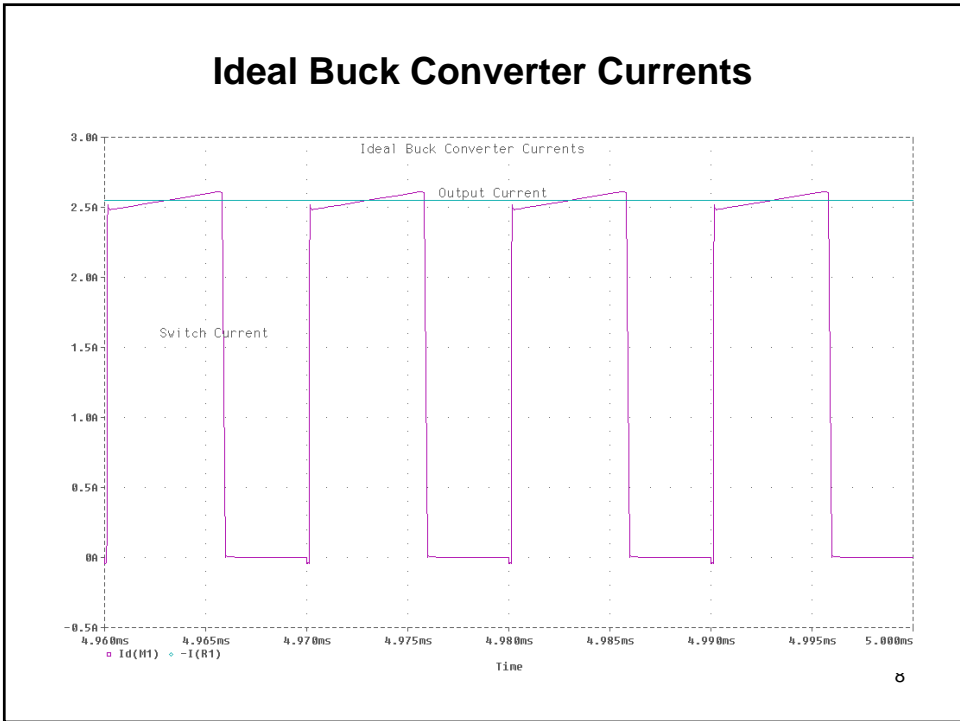
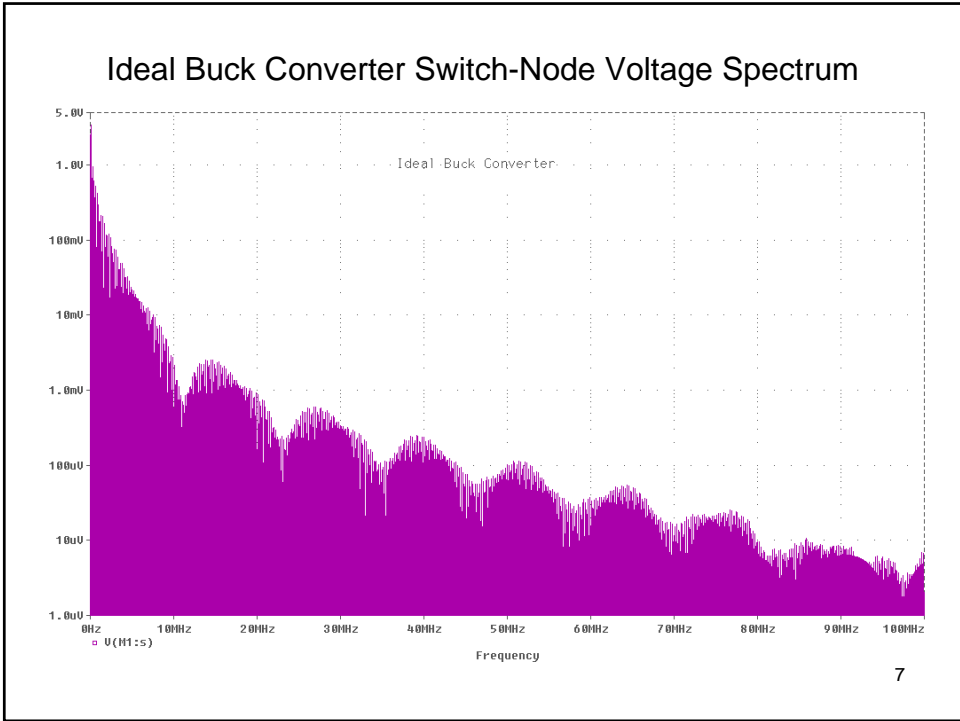
## Ideal Buck Converter Operation

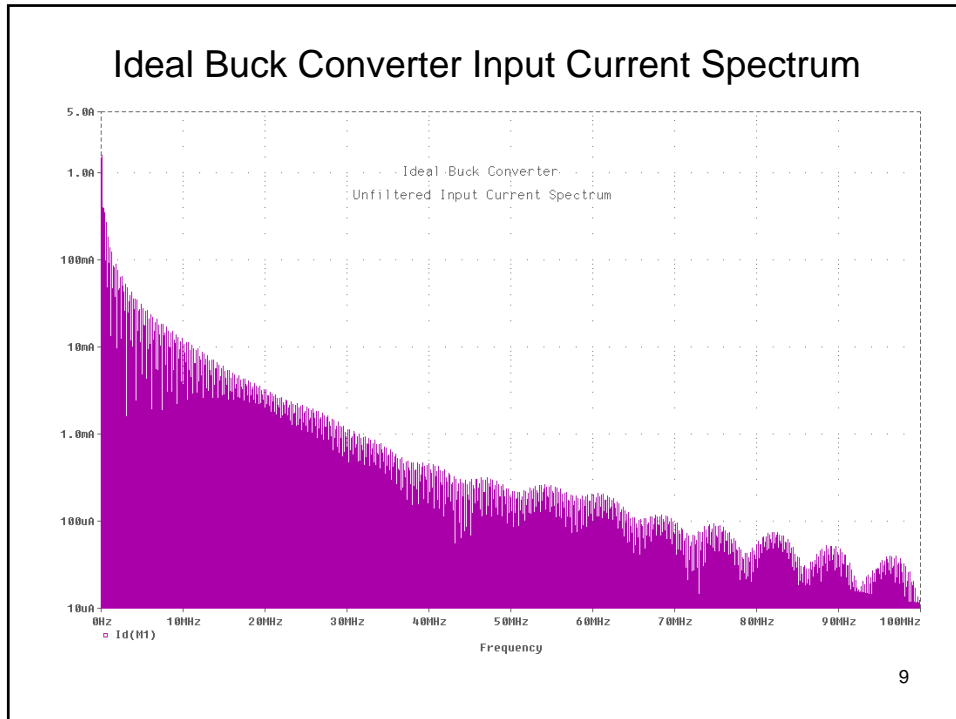
- An ideal buck converter would be formed with ideal components.
- When M1 is closed,  $V_{in}$  is impressed across output filter, charging L and C.
- When M1 is open L and C discharge into load returning through D1.
- Input current is chopped by switching, output current is smoothed by L and C.
- $V_{out} = (t_{on}/T) * V_{in} = D * V_{in}$  - - D is the duty cycle of M1
- These circuits are very commonly used in all classes of equipment for point of load voltage regulation

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## Ideal Buck Converter Voltage Waveforms

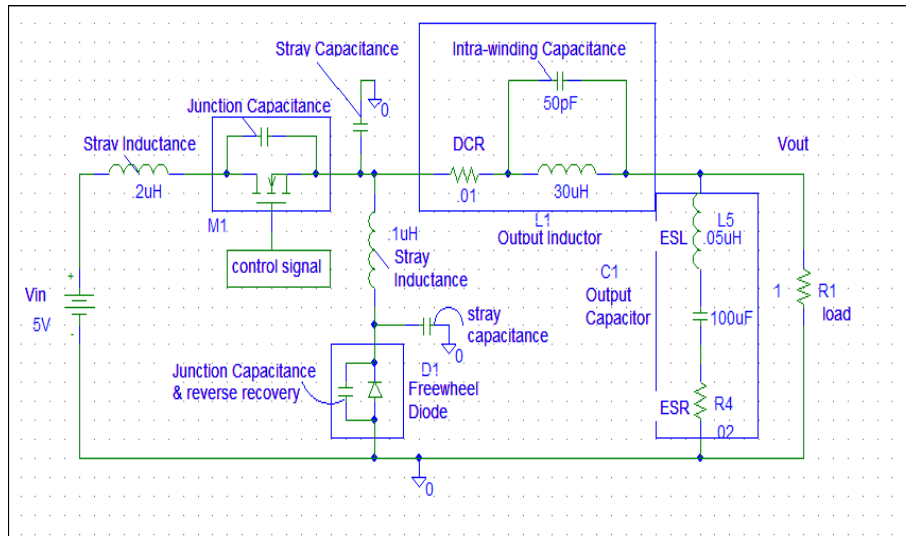






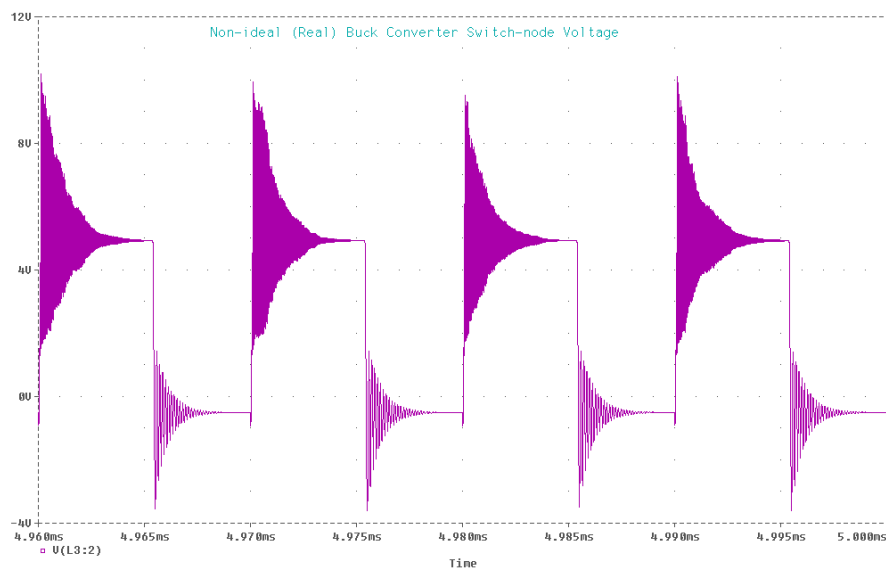
- ### Ideal Converter
- The lesson here is even an *ideal* switch-mode converter can create substantial EMI.
  - A switch mode converter with ideal components still requires careful PCB design.
  - EMI can get a lot worse when non-idealities are realized.
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## “Real” Buck Converter



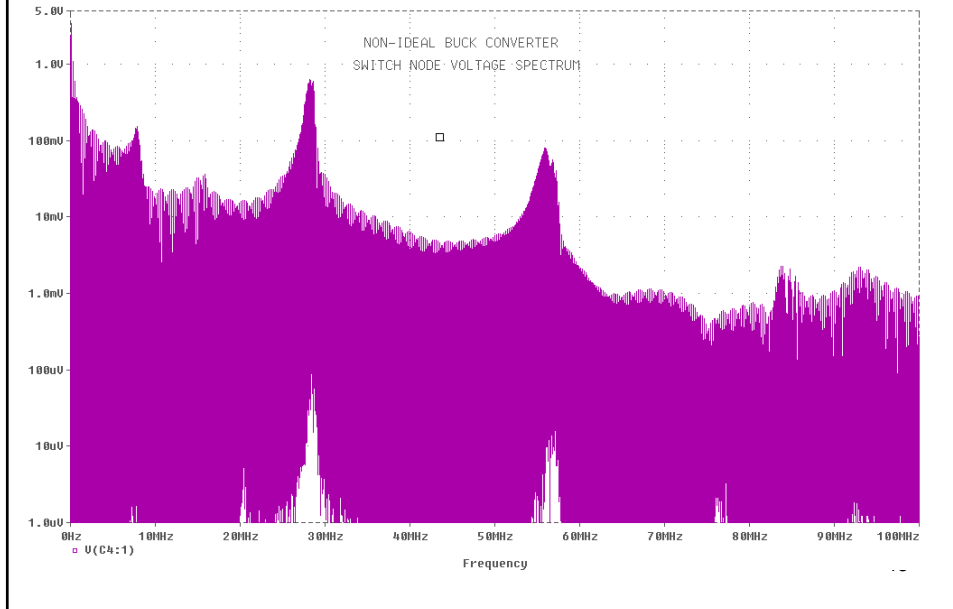
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## Real Buck Converter Switch-node Voltage

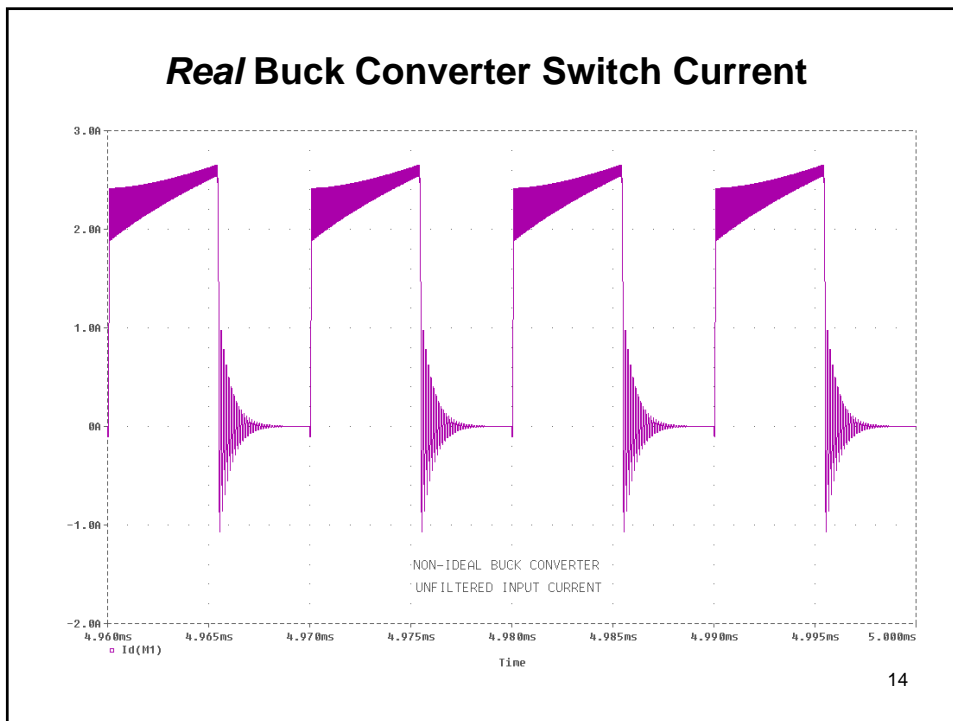


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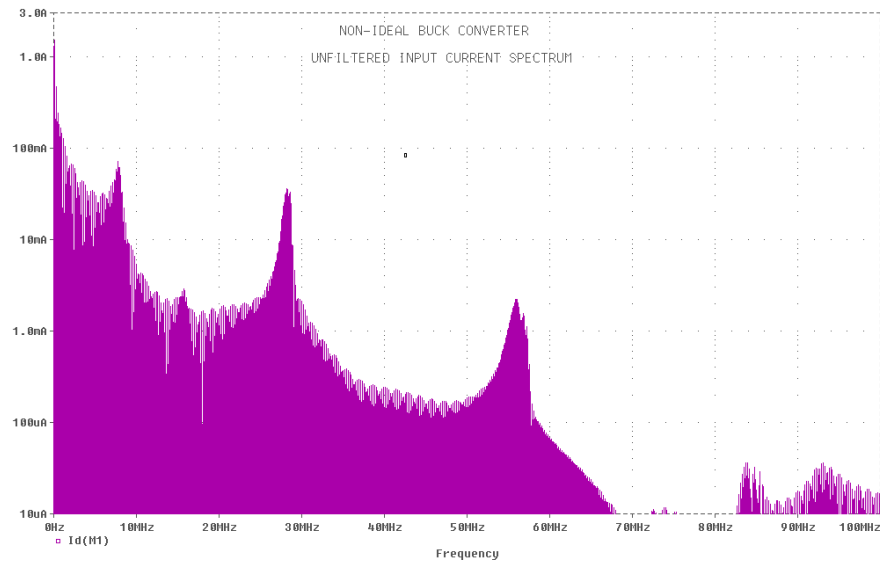
## Real Buck Converter Switch Node Voltage Spectrum



## Real Buck Converter Switch Current



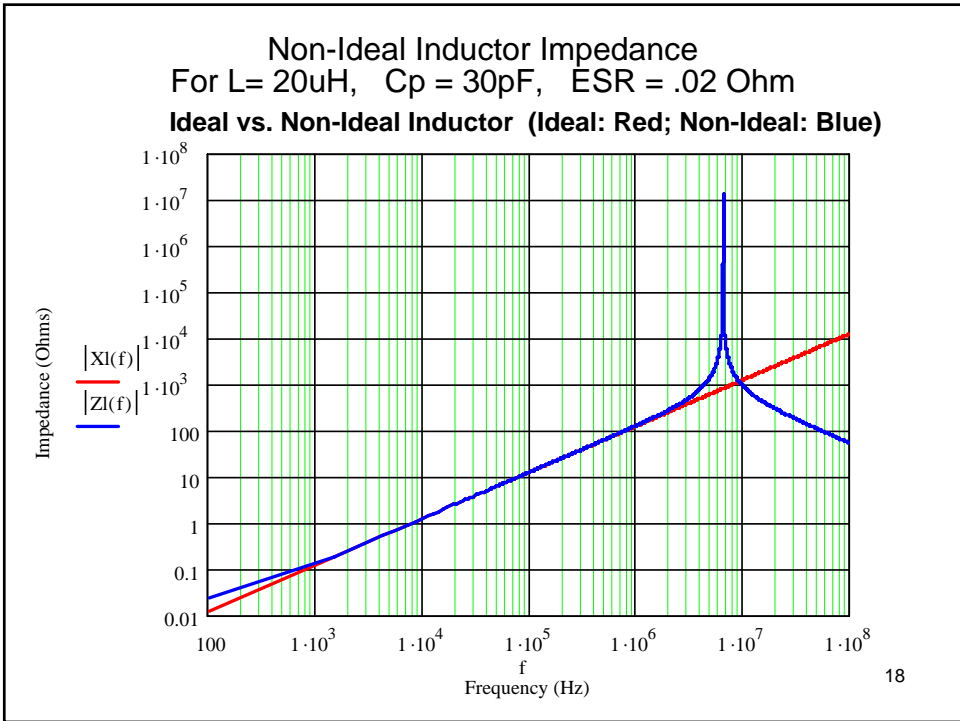
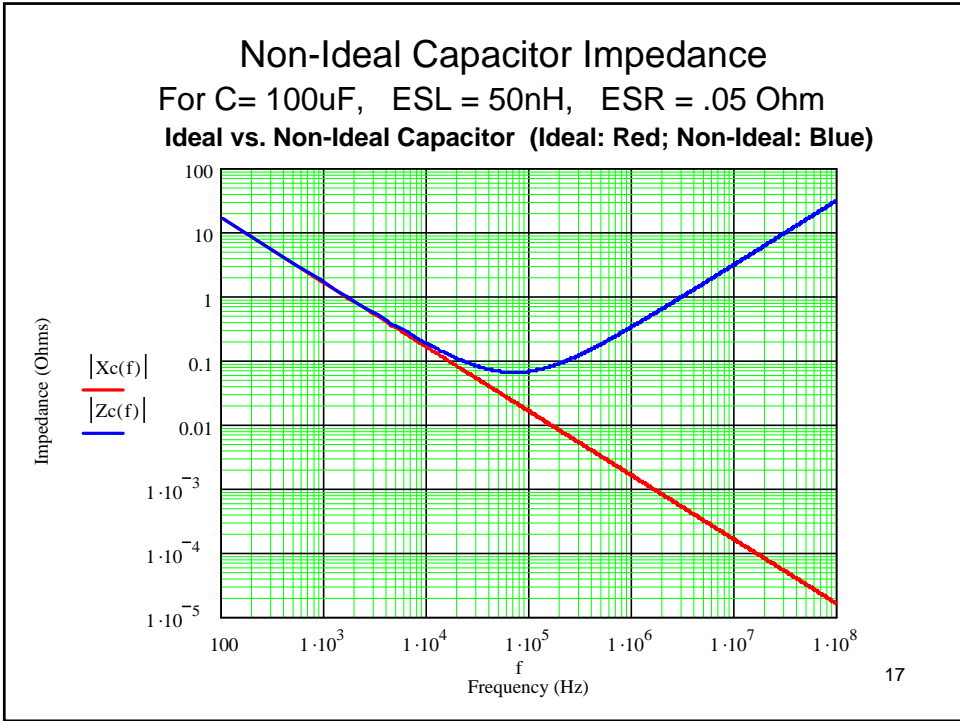
## Real Buck Converter Switch Current Spectrum

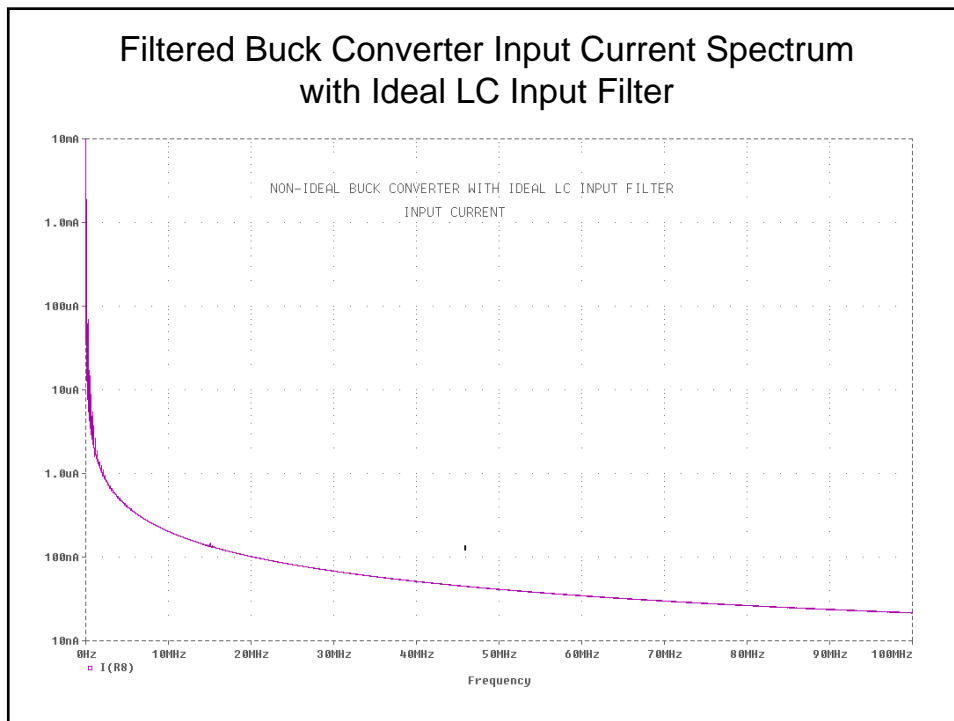
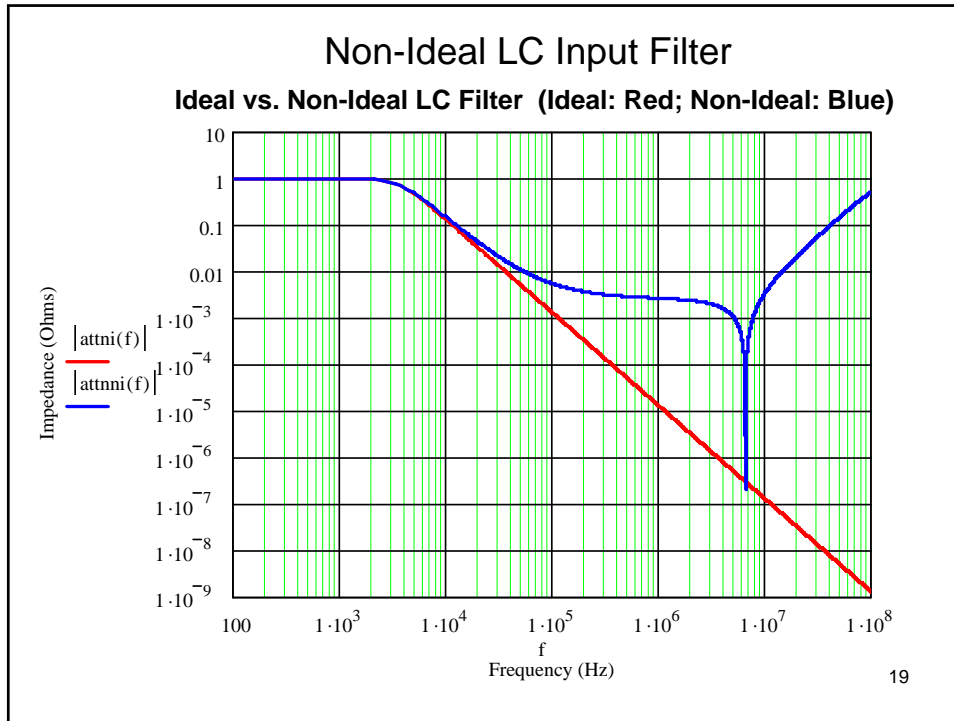


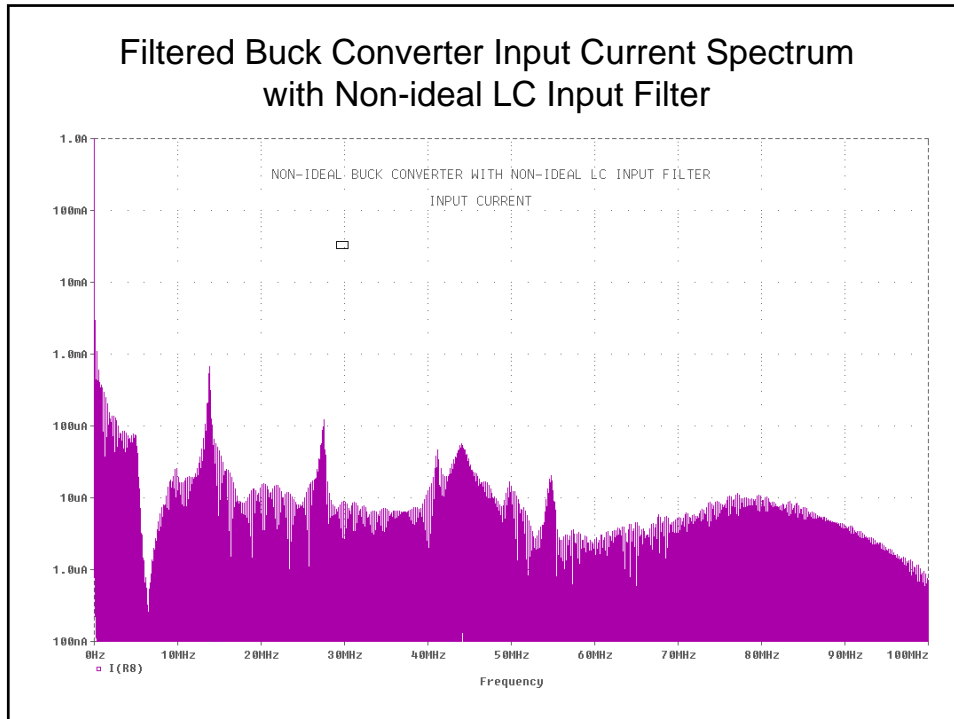
## Non-Ideal Converter Observations

- The **source** of electrical noise in the SMPS is the fundamental switch action exacerbated by circuit and component parasitics.
- Passive components have parasitics (inductance, capacitance, resistance) based on their physical construction.
- PCB board conductors also have parasitic inductance, capacitance: these parasitics can be harmful or they can be helpful –That is why PCB design is critical!
- Semiconductors have junction capacitance and lead inductance.
- Junction diodes have the reverse recovery characteristic.
- Parasitic quantities not only contribute to the generation of noise – they provide **paths** for the conduction of noise.
- These levels may not look high but EMI problems are low energy – according to Bruce Carsten:
  - More than 20nW at 1MHz will fail FCC Class A.
  - More than 1.26nW at 1MHz will fail FCC Class B.

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## PCB Layout and Troubleshooting Guidelines

- So, If you really had to implement a buck converter (or similar) or solve an EMI/EMC problem with one where do you start?
  1. Identify **high dv/dt** nodes
    - High dv/dt nodes capacitively couple to other conductors interfering with neighboring circuits and driving noise currents in unintended paths.
  2. Minimize the dv/dt to the extent possible
    - minimize slew rate of the excitation source
    - Use snubber circuits (damping networks) if necessary

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### PCB Layout and Troubleshooting

3. Shield with “quiet rail” plane to the extent that you can tolerate capacitive loading on the circuit.
  - SMT semiconductors used as high frequency power switches may require PCB area for heatsinking.
4. Keep high dv/dt nodes physically away from unfiltered lines that connect to the assembly.
  - Examples: input power, output power, control lines
5. Identify **high di/dt** loops
  - High di/dt loops create magnetic fields that will induce noise currents in neighboring circuits.
6. Keep high di/dt loops tight (compact) – that is minimize the area enclosed by the loop. Even changing layers with vias adds to enclosed area.

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### PCB Layout and Troubleshooting Guidelines

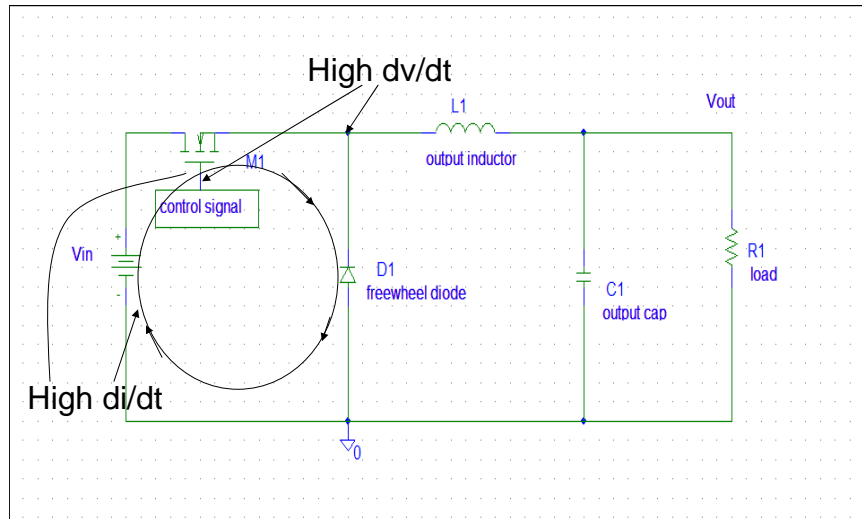
- Use planes where possible as return paths (this naturally provides minimum loop area)
- Be careful not to place sensitive circuits in the return path of high di/dt current .

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## Buck Converter

Where are the high  $dv/dt$  nodes and high  $di/dt$  loops?

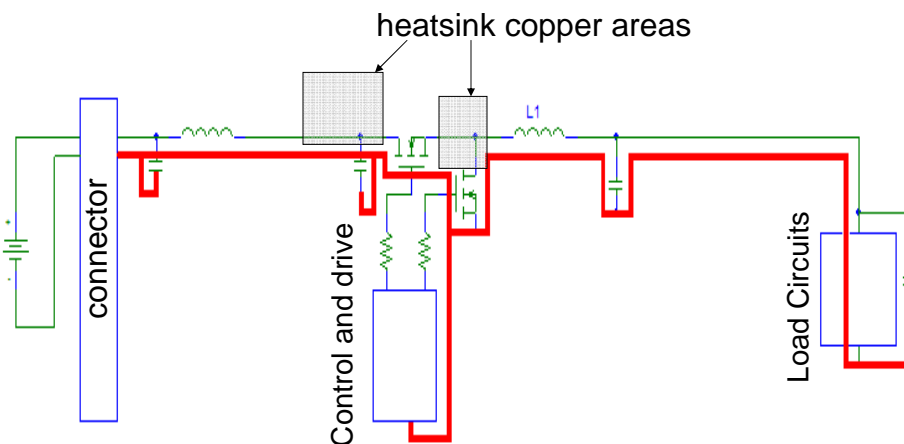
Look for the switches and non-linear elements



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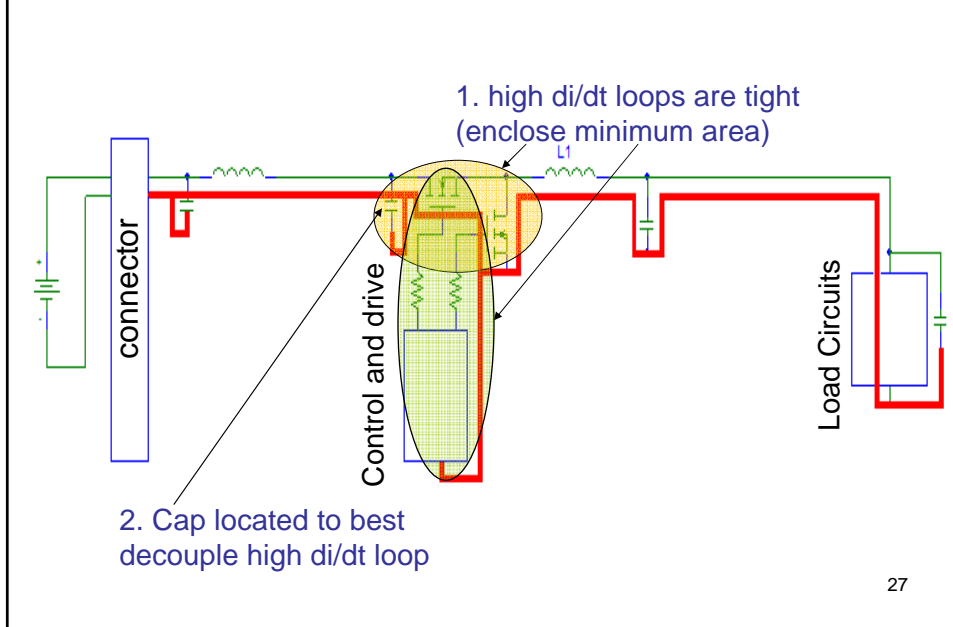
## Buck Converter Layout –good layout

What's good about it?

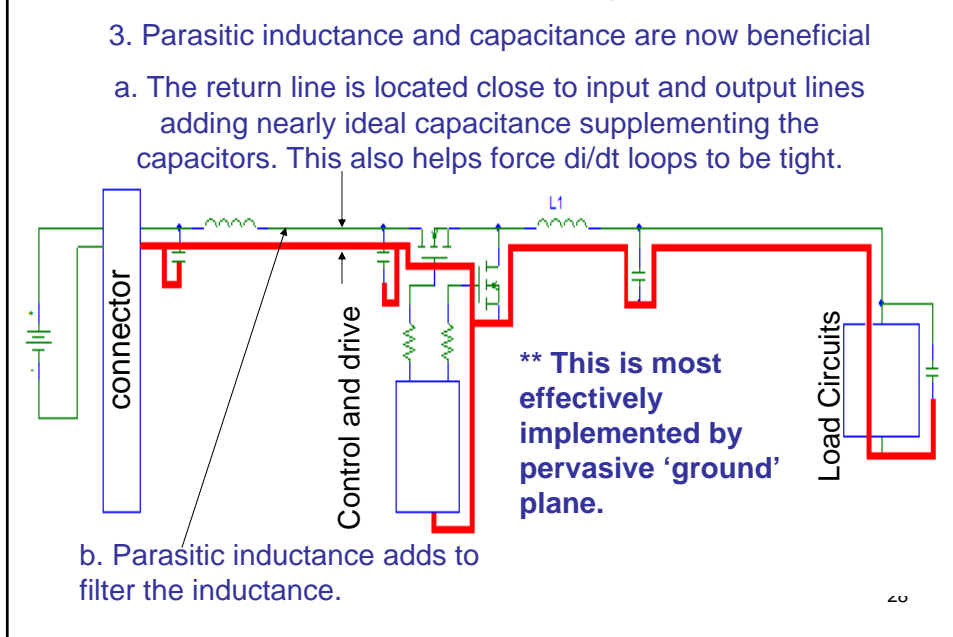


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## Buck Converter Layout –good layout

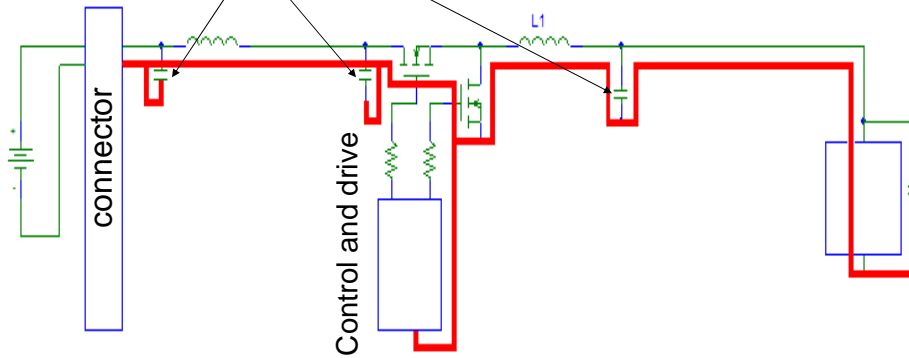


## Buck Converter Layout –good layout



## Buck Converter Layout –good layout

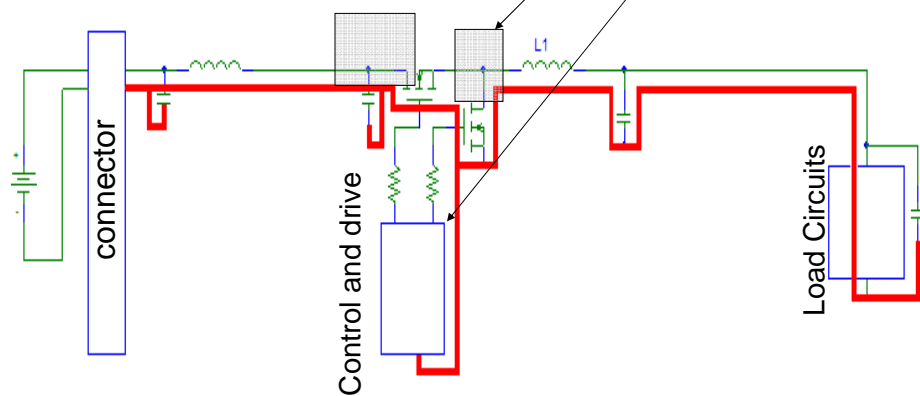
4. Caps are routed to minimize the series inductance.



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## Buck Converter Layout –good layout

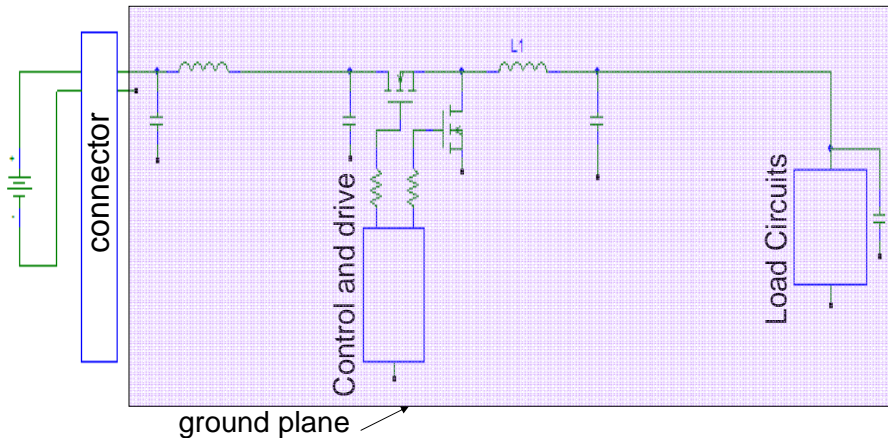
5. High dv/dt nodes kept away from entry and exit nodes



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## Buck Converter Layout –good layout

With 'ground' or 'quiet' plane



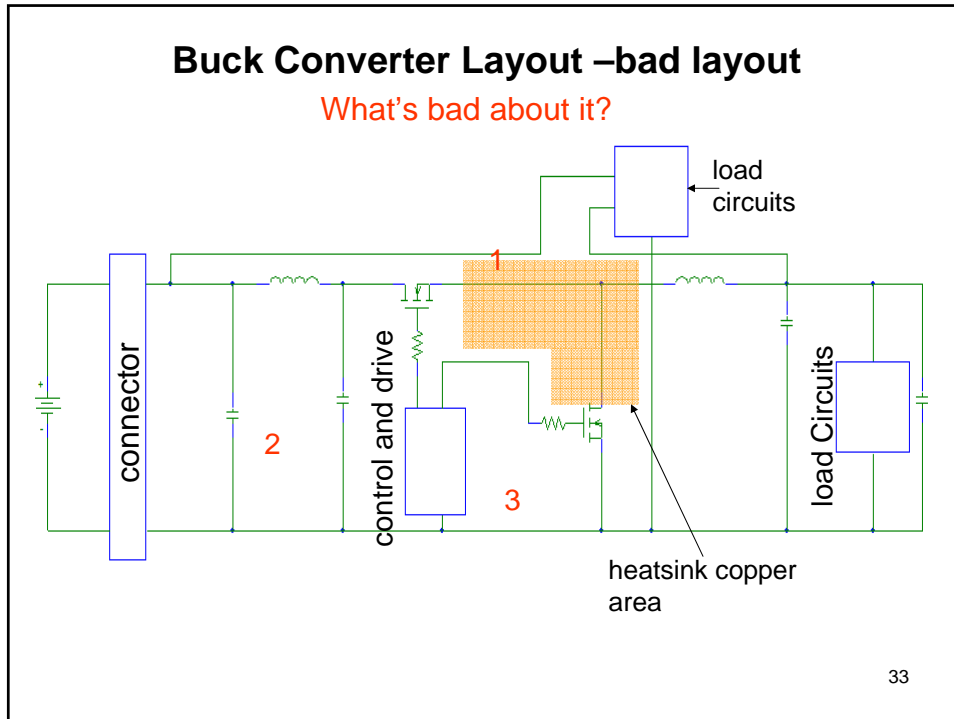
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## Advantages of Ground Plane

Ground planes provide:

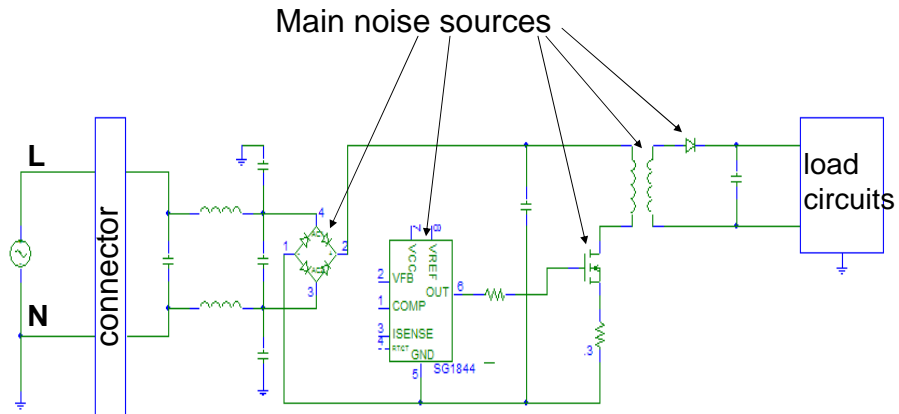
1. minimum  $di/dt$  loop area (conservation of energy)
2. provides distributed capacitance for enhanced decoupling (capacitive loading of switching nodes increases dissipation in the switches).
3. helps shield conductors on other PCB layers from high  $dv/dt$  nodes

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- ### Buck Converter Layout –bad layout
1. **Unfiltered input and output lines pass very close high dv/dt node.**
    - High dv/dt node is a large copper area – does it need to be this large?
    - Trade off between electric field source and heat spreading (temperature rise)
  2. **Connections to capacitors add series inductance.**
    - Capacitors are not located as close to the nodes they are decoupling as they could be.
  3. **High di/dt loops enclose a large area.** Yields
    - high magnetic fields
    - excess parasitic inductance which yields voltage spikes in response to high di/dt
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## AC Input Flyback Converter

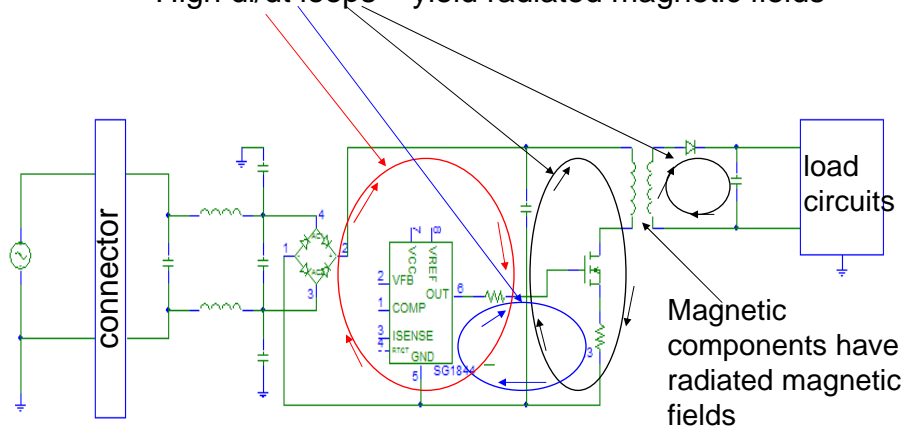


- Flyback is a very useful and common power supply circuit

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## AC Input Flyback Converter

High di/dt loops – yield radiated magnetic fields

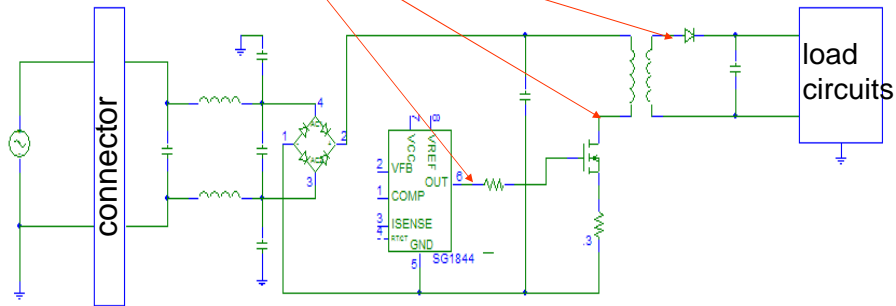


- PCB layout should minimize the area enclosed by high di/dt loops.

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## AC Input Flyback Converter

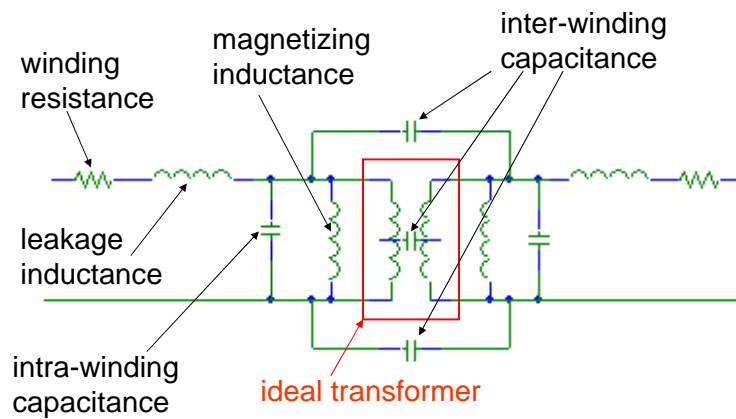
High  $dv/dt$  nodes – yield radiated electric fields



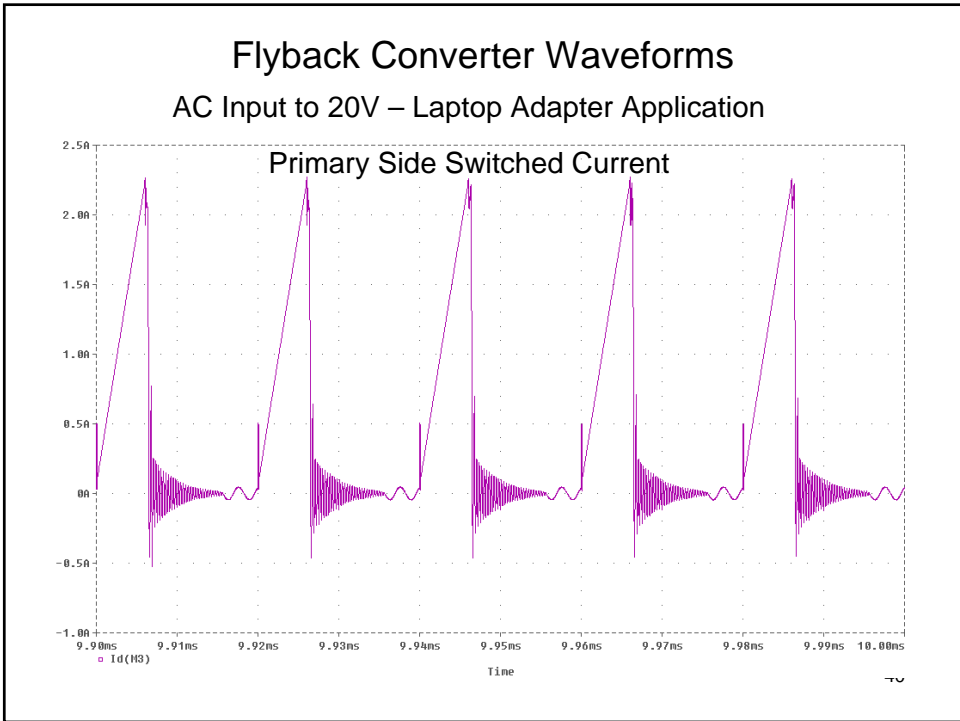
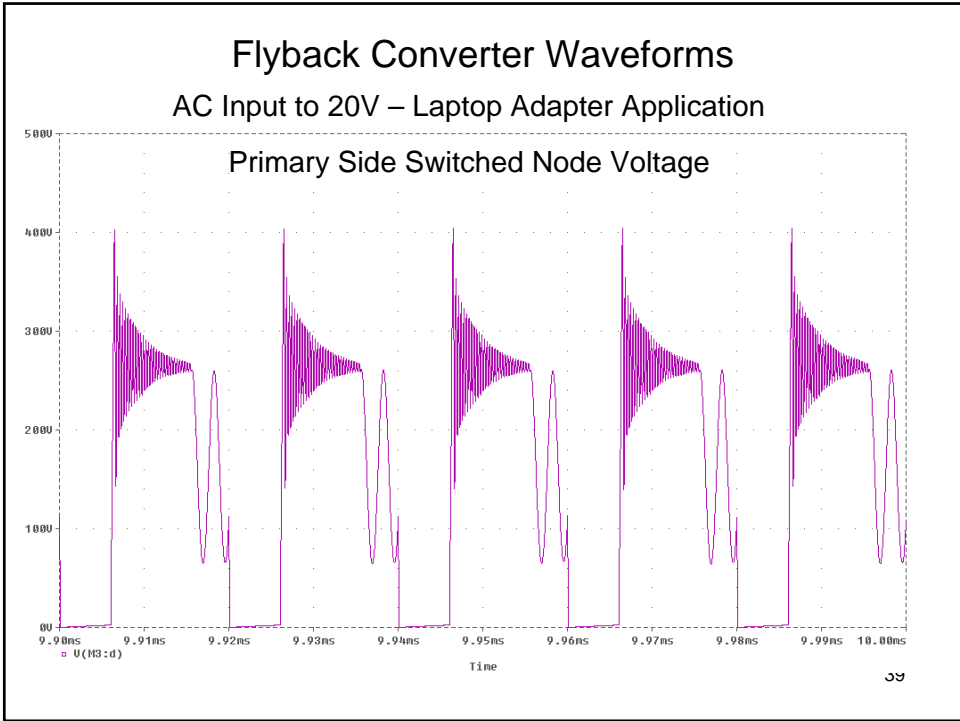
- minimize the area of high  $dv/dt$  nodes (to the extent possible)
- keep high  $dv/dt$  nodes away from unfiltered and sensitive lines

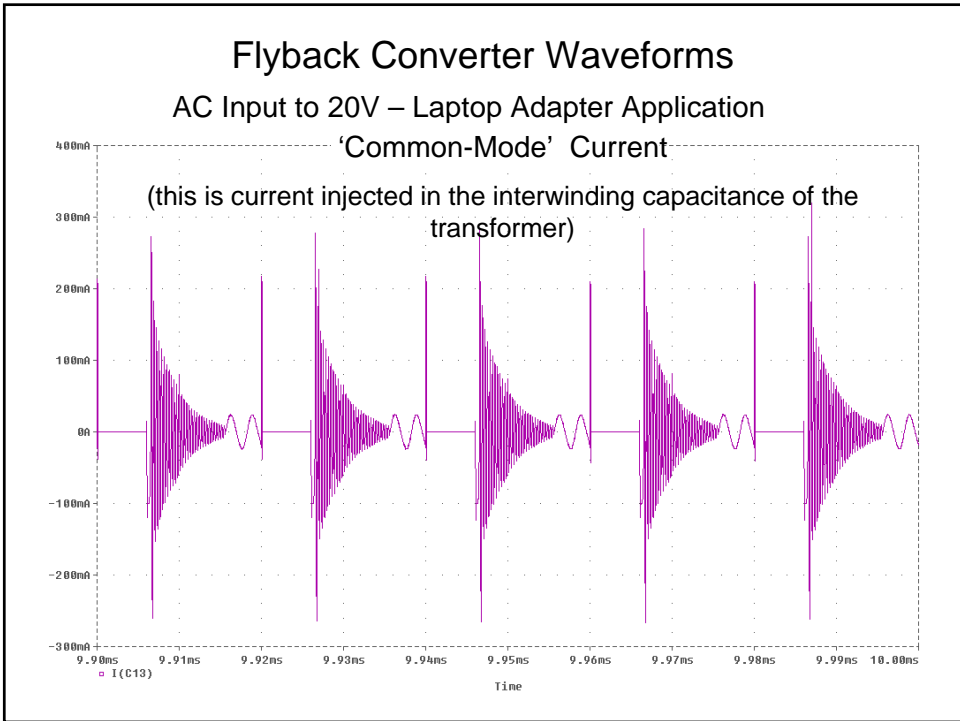
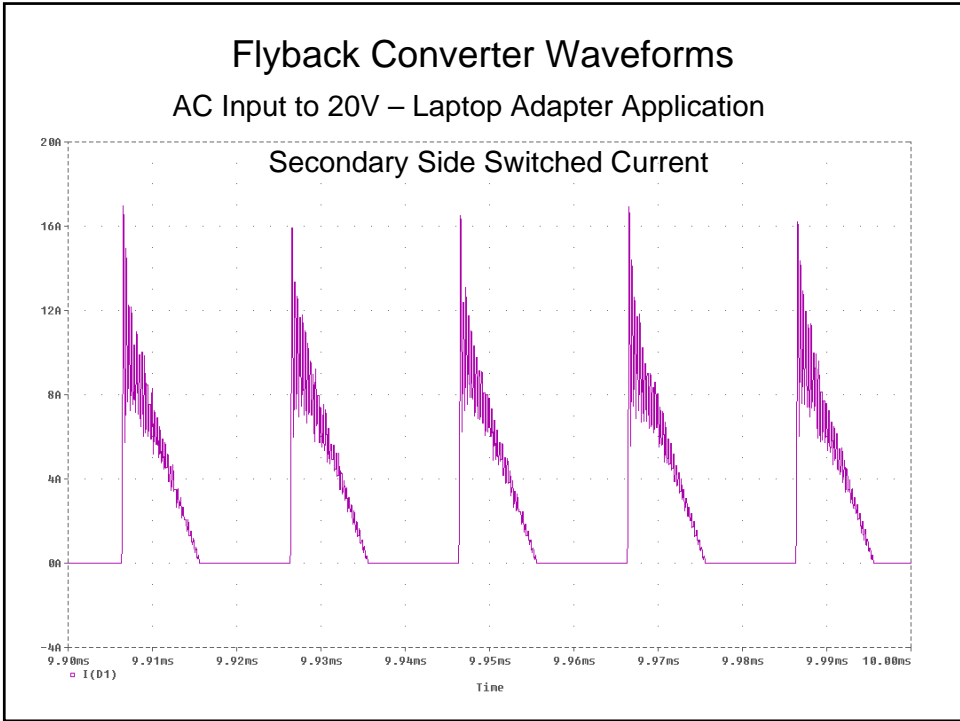
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## Transformer Parasitics

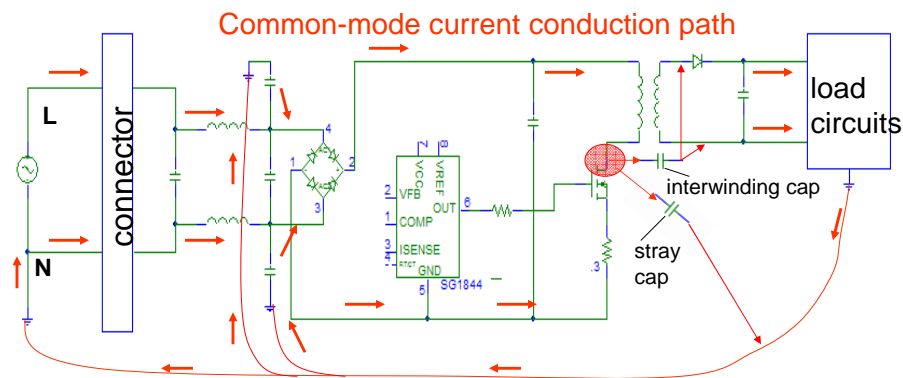


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## AC Input Flyback Converter



- all  $dv/dt$  nodes coupled to any stray or parasitic capacitance with an earth path create common-mode currents.
- common-mode currents are part of conducted emissions – usually the toughest part to solve.
- common mode currents also can cause radiated emission problems 43

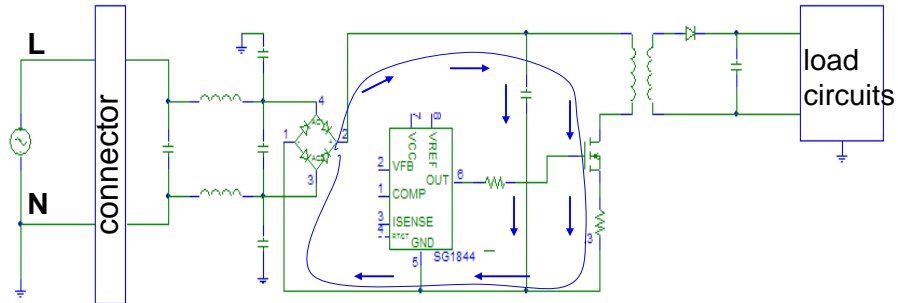
## Avoiding Common-Mode Induced EMC Problems

1. Minimize area enclosed by high  $di/dt$  loops.
2. Minimize area of high  $dv/dt$  nodes to minimize stray capacitive coupling.
3. Use “quiet rail” plane under high  $dv/dt$  nodes.
4. Use optimally-placed, Y-designated caps to provide CM currents a shunt return path to the primary.
5. Minimize transformer parasitics – tough to do
  - minimizing leakage inductance usually increases interwinding capacitance and vice versa.
6. Minimize  $dv/dt$  to the extent possible:
  - Limit the slew rate of power switches
  - Use snubbers to further reduce  $dv/dt$
  - Both of these can increase dissipation
7. Input filter must have lots of common-mode attenuation:
  - Use a common-mode choke and Y-caps.

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## AC Input Flyback Converter

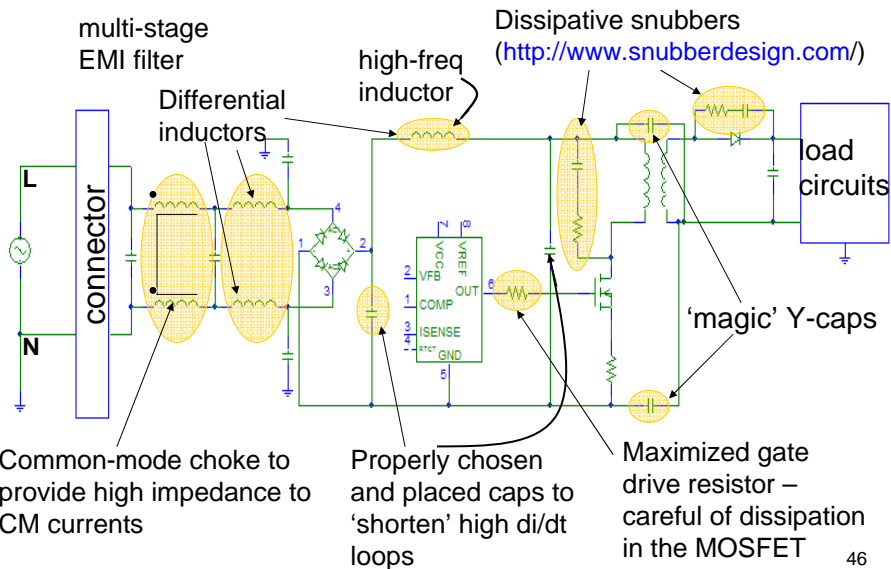
Differential-mode current conduction



1. Analyze spectral content of converter input current – by simulation, measurement, or approximation.
2. Determine attenuation requirements of filter.
3. Make sure the filter implementation and components have the frequency response you need.- you may need a multi-stage filter.

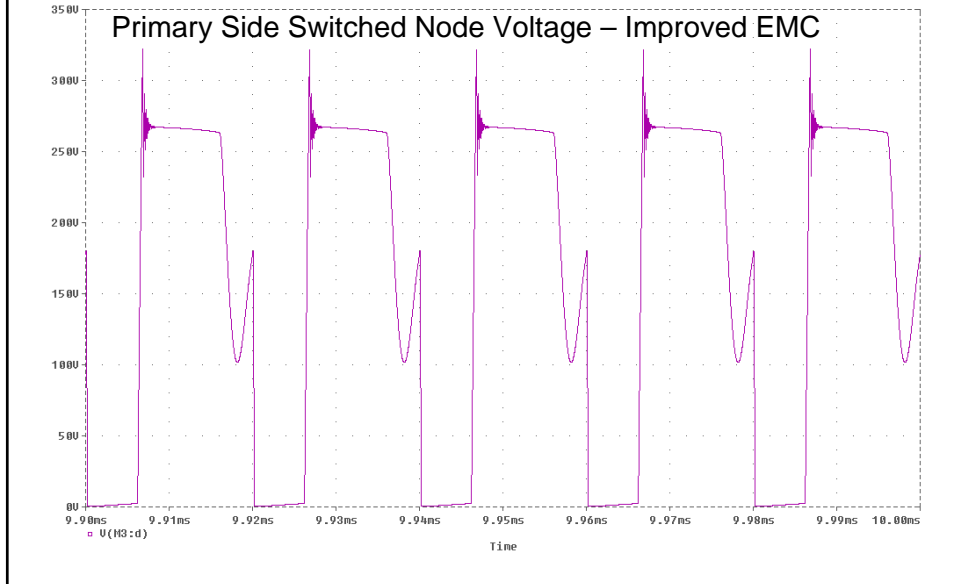
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## AC Input Flyback Converter with EMC Improvements



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## Flyback Converter Waveforms AC Input to 20V – Laptop Adapter Application



## Flyback Converter Waveforms AC Input to 20V – Laptop Adapter Application Primary Side Switch Current – Improved EMC



### **Common Mode Chokes vs. Single 'Differential' Inductors**

- CM choke is connected so that the input current and its return produce cancelling magnetic fields – thus there is no net magnetization due to differential currents.
- CM choke thus can be made with very high inductance (1mH-10mH) with relatively high differential current ratings.
- Leakage inductance of the CM choke appears as differential inductance to the filter (typically .3% to 1%) – this is beneficial to attenuating differential noise. –High permeability CM chokes may produce inferior results because they low leakage inductance
- Single inductors in each line do provide CM inductance but have to be sized to handle the full differential current. Single chokes of value L in input and return lines yields a CM inductance of L and a differential inductance of 2 L.
- Be careful of how large you choose differential input inductance to be; this increases the source impedance seen by the SMPS and can destabilize it (Middlebrook criterion)

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### **Notes on Combating Radiated Emission**

- The same techniques to minimize conducted emissions are beneficial to reducing radiated emissions:
  - Keep high di/dt loops tight (minimized area enclosed by the loop)
  - Minimize area of high dv/dt nodes
  - decrease slew rate of power switches as much as tolerable
  - Use 'quiet rail' planes under switching circuits (high di/dt loops and high dv/dt nodes)
  - Connect 'quiet rail' planes of isolated circuits (such as primary and secondary of AC input power supply) with capacitors (good high frequency characteristics) near the switching components.
  - Minimize leakage inductance in transformers – leakage inductance means stray magnetic fields.
  - Choose inductors with closed magnetic paths – especially in applications with large current swings (like in an AC input filter).
- Radiated emissions become conducted emissions and vice versa; both originate from the same source within a SMPS!

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### **Notes on Junction Diode Reverse Recovery**

- Junction diodes have stored charge (minority carriers) that have to be purged before the diode appears off (reverse-biased)
- A junction diode being 'hard switched' (from forward biased to high  $dv/dt$  reverse voltage) provides a reverse conduction path resulting in spikes of current that add to the high  $di/dt$  that is fundamental to SMPS operation.
- Different diodes have differing recovery times and shapes.
- The choice of diode can make a dramatic impact on SMPS EMI. Generally choose Schottky diodes if the voltage requirements are low enough. If higher voltage ratings are needed, choose ultra fast style or so-called "soft recovery" style junction diodes.
- The faster the recovery of the diode the less time to build current in leakage and stray inductance reducing voltage transients.
- Reducing the  $dv/dt$  driving the diode recovery also reduces voltage and current transients.
- Search "diode reverse recovery" on your favorite internet search engine and you will find lots of helpful references.

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