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Electrostatic Discharge –
The Phenomena, Design Guidance and Testing for Improving Product Immunity

Huntsville, Alabama
January 15, 2009

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Agenda

- ☞ The ESD Phenomena
  - ☞ Causes, Characteristics and Effects
- ☞ Design Guidance
  - ☞ Equipment Construction and PCB Layout
- ☞ Testing Considerations
  - ☞ Processes, Facilities and Equipment
- ☞ Summary - Q & A

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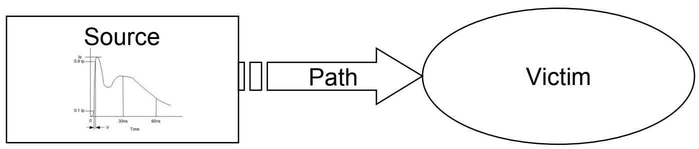
Phenomena

- Electromagnetic Interference Model



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Phenomena

- Why concern ourselves with Electrostatic Discharge in the first place?

  - Effects range from Nuisance to Catastrophic
  - Reliability and Time to Market
  - Electromagnetically Compatible Environment

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Phenomena

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Phenomena

- Electrostatic Discharge is described as the abrupt release of static charge from one object to another.
- When materials are brought into contact with one another and separated one material will release charge (electrons) while the other will accept this charge.
- The tendency to accept or release charge is dependant on many factors – including type of material, method and duration of contact.
- Once a charged surface is brought into proximity or contact with another surface that is of lower resistance to ground a sudden and intense transfer of energy will occur.

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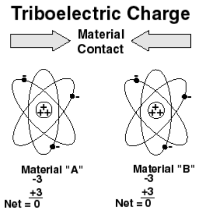
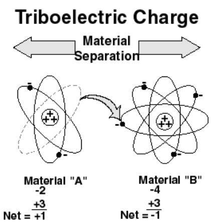
Phenomena





Typical Triboelectric Series

POSITIVE

1. Air
2. Human Skin
3. Asbestos
4. Glass
5. Mica
6. Human Hair
7. Nylon
8. Wool
9. Fur
10. Lead
11. Silk
12. Aluminum
13. Paper
14. Cotton
15. Wood
16. Steel
17. Sealing Wax
18. Hard Rubber
19. Mylar
20. Epoxy Glass
21. Nickel, Copper
22. Brass, Silver
23. Gold, Platinum
24. Polystyrene Foam
25. Acrylic
26. Polyester
27. Celluloid
28. Orlon
29. Polyurethane Foam
30. Polyethylene
31. Polypropylene
32. PVC (vinyl)
33. Silicon
34. Teflon

NEGATIVE

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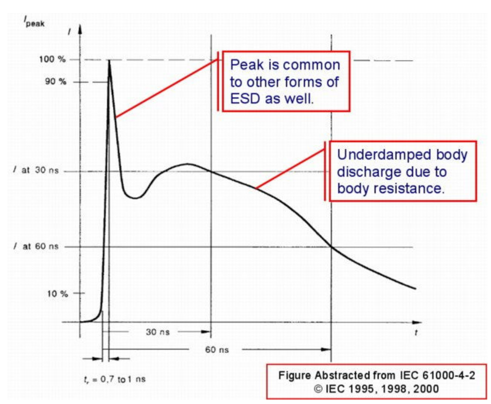
Phenomena

- Fast rise time, intense peak with relatively short duration.
- Can be many amps of current with very high voltages

Typical ESD Voltage Levels		
Means of Generation	10-25% RH	65-90% RH
Walking across carpet	35,000V	1,500V
Walking across vinyl tile	12,000V	250V
Worker at bench	6,000V	100V
Poly bag picked up from bench	20,000V	1,200V
Chair with urethane foam	18,000V	1,500V



Phenomena

- Effects of ESD –
  - Conduction – Currents flowing through circuitry causing breakdown and failure.
  - Secondary Arcing – Currents flowing through circuitry as a result of proximity to initial arc
  - Capacitive and Inductive coupling (E/H-Field) – Fields are produced as a result of current flowing through discharge path; these fields induce voltage and currents into adjacent circuitry through coupling

Phenomena

- Conduction and Secondary Arcing–
- Assumptions:
  - 10nH/cm of inductance on circuit trace
  - 1 cm trace
  - 10A of current in 1ns of time
  - Leads to 100V/cm of voltage along the trace
    - $V=L\ dI/dT$
  - 5pf of capacitance from signal trace to return path (ground)
  - 1000 V charge in 1 ns
  - Leads to 5A of current injected on the signal
    - $I = C\ dV/dT$

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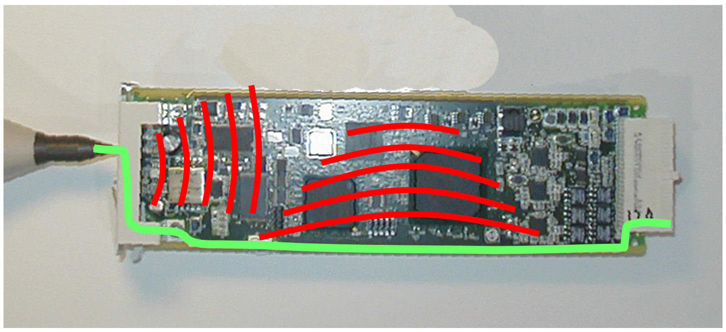
Phenomena

- Fields Example –



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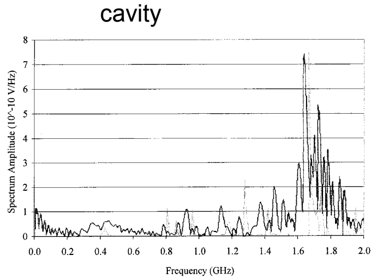
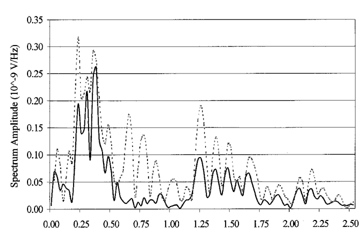
Phenomena

- Capacitive and Inductive Coupling –
  - Introduction of a 2kV ESD event into a test fixture resonant cavity



Differential mode



Common mode

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Phenomena

- Effects on Hardware –
  - Performance
    - Data errors, loss of stored data
    - Loss of Sync
    - Change of state
    - Reset, loss of power
  - Damage

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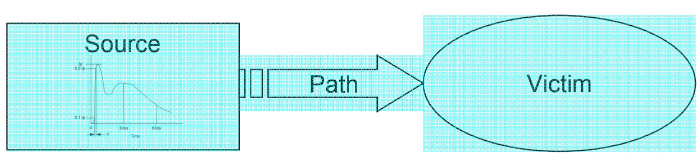
Design



- Approach for EMI resolution –
  - Logical, systematic and consistent evaluation
  - Prevent the occurrence of the ESD Event
  - Removal or reduction of the coupling path
  - Increasing the inherent immunity of the product

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Design

- Prevent Occurrence – Control Products and Handling

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Design

- 33% of the problem solved, right? – So now what …?
  - Removal or reduction of the coupling path
  - Increasing the inherent Immunity of the product
    - Mechanical/Construction
    - PCB layout
    - Component Selection and placement
    - Testing Considerations

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Design

- General –
  - Susceptibility to an ESD event can have a variety of sources not always related to the product
  - Start with the big picture and narrow the search
  - Examine the nature of the failure for indicators of the source
  - Changes that exist from one product to another – new products, product revisions or devices
  - Strive for repeatable processes to reduce ‘false’ failures
  - A proper grounding scheme is the basic tool for ESD Immunity

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Design

- Mechanical/Construction issues –
  - Planned, Low impedance path - Route away from sensitive circuitry or cabling as much as possible – use distance to your advantage
  - Wider is better – High Frequency energy takes the path of least inductance - on the outer portion of the conductor (skin effect). Increasing the available surface area will improve the path performance
  - Dependable Ground connections – Clips, Mounting holes, stand-offs and long support tabs
  - Plastic housings or lack of Earth Ground connections require special consideration

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Design

- Mechanical/Construction issues –
  - Masking of painted mating surfaces including mounting tabs and screw holes (DB9 connectors) –allow for maximum misalignment in assembly
  - Protect Displays (LCD/LED) or other with Mylar film or with distance – recess displays.
  - Use of Light pipes or other non-conductive materials may be used to provide isolation of potentially sensitive circuitry
    - This may have some advantages in material costs both in the construction material and less parts required for filtering
  - Protect other components near the faceplate or surfaces where charge may be present – switches, reset buttons etc…use of filter components

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Design

- Mechanical

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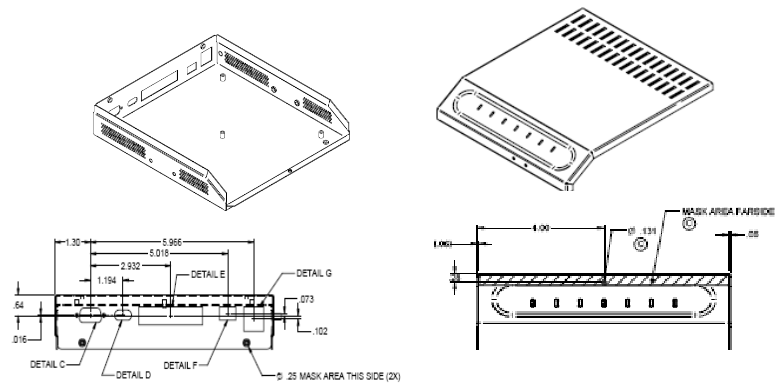
Design

- Mechanical



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Design

- Mechanical

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Design

- Routing and Construction of the Ground trace
  - Routed away from potentially sensitive circuitry - clear path to frame ground
    - Power Supply Section
    - Away from Reset and Data lines
    - Avoid parallel routing
  - As low impedance as possible
    - Wide traces included on as many layers as possible; 50-100mils wide with 50-100mils separation
    - Trace vias added to connect ESD trace often
    - No 'neck-down' of trace – connect pins on all layers
    - Not a complete circle

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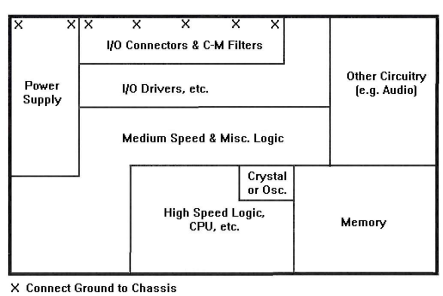
Design

- General Part and Circuit Placement
  - Compartmentalization – use logical processes for determining layout
  - Care must be taken in placement of logic devices and reset parts/circuitry to minimize susceptibility and maximize immunity
    - Avoid card edges, move inward as much as possible
    - Devices that are smaller, more complex or operate at lower voltages tend to be more susceptible
    - Use capacitors, inductors and ferrites to dissipate energy on sensitive circuits



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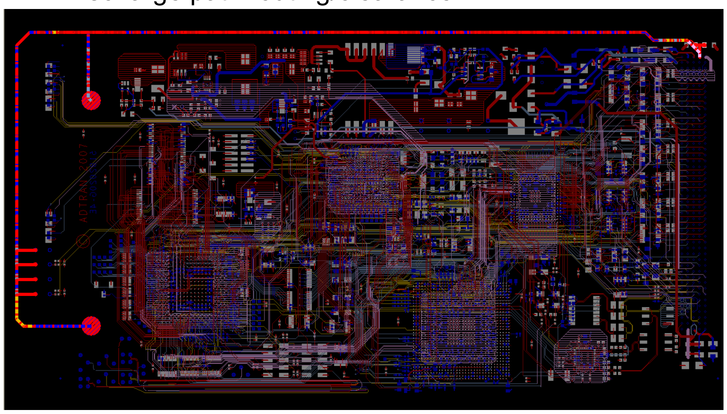
Design

- – Discharge path routing/clearance



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Design

- Reset Circuitry
  - Use simple routing
    - Close to logic inputs
    - Use short traces, route with 1st priority after clock lines or other critical nets
    - Away from faceplates, board edges and static discharge path - avoid parallel routing
    - Avoid crossing moats in planes – large voltage swings can occur during ESD events
    - Operate off the highest voltage possible – lower voltage circuits tend to be more sensitive to ESD
  - Use capacitors (typically .1uf) on each reset line ferrites may be used in addition for particularly sensitive parts.

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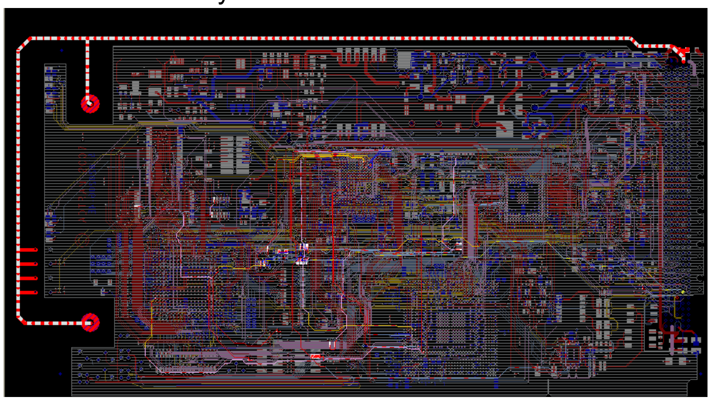
Design

- – Reset Circuitry



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Design

- Critical nets and Debug Circuitry
  - Avoid routing critical traces parallel to Frame Ground (Discharge path)
    - Faceplates, chassis surfaces are part of Frame Ground
    - Proper spacing
    - Use 90 degree angle for placement
  - Debug Circuitry/Header connectors
    - Great for development – can be painful in testing
      - Mind part placement rules for location of Debug headers
      - Remove debug headers from test samples – energy can couple to leads
      - Use no load 0 ohm resistors at sources to eliminate stubs on board – keep in mind for other nets; test points etc…

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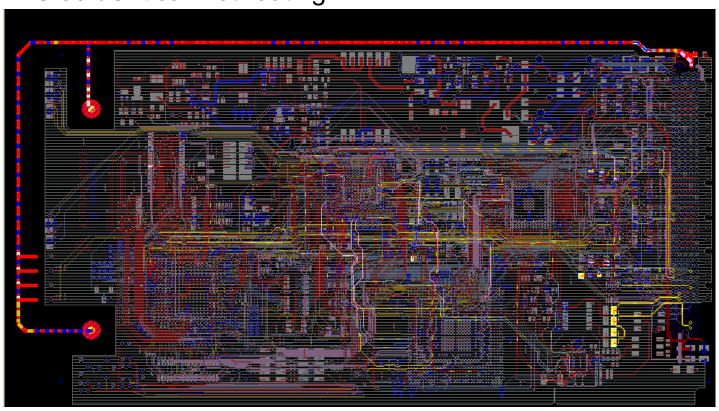
Design

- Clock/Critical Net routing



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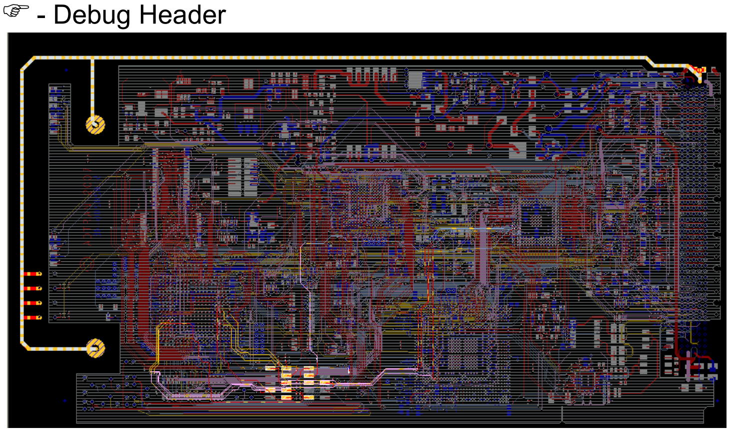
Design

- \- Debug Header



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Design

- Ground and Power Planes
  - Digital Ground planes and Power planes may serve as shields or insulators from ESD
  - More Power and Ground fill available results in lower overall inductance – voltages developed by ESD will be lower and more easily dissipated – wider is still better
  - Taking advantage of imbedded capacitance by having well coupled Power and Ground planes will not only improve high frequency emissions - overall ESD performance should be improved. A great deal of High Frequency energy is produced in an ESD event
  - Planes should be recessed as much as possible from potentially charged surfaces, mounting holes, connections or intended discharge path

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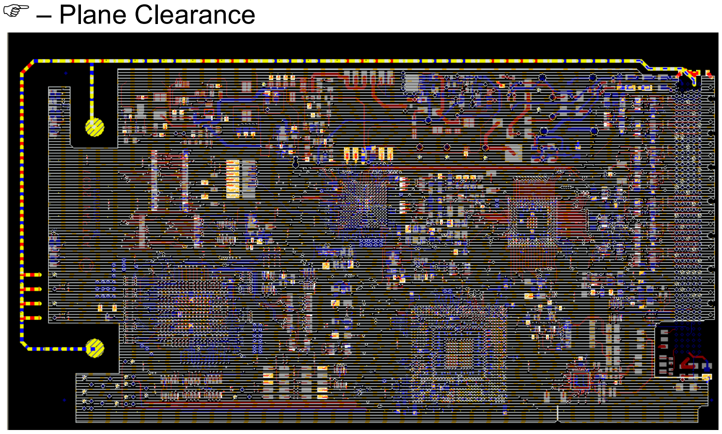
Design

- – Plane Clearance



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Testing

- IEC EN 61000-4-2
  - Describes testing and measurement techniques for Commercial Electrostatic Discharge Immunity Tests
    - Defines a variety of parameters including:
      - Test Equipment
      - Physical arrangement of Equipment Under Test, Support Equipment and cabling
      - Laboratory conditions for testing
      - Conduct of the test

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Testing

- Test Equipment –
- Variety of shapes, sizes and manufacturers
- Intended to simulate the Human Body Model (and others)
- Most commonly 150pf/330Ω $\underline{+}$10%
- Require calibration and proper use






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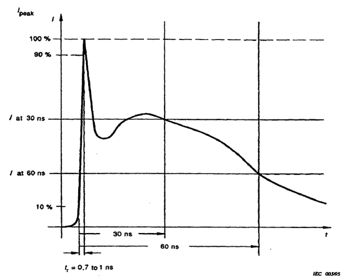
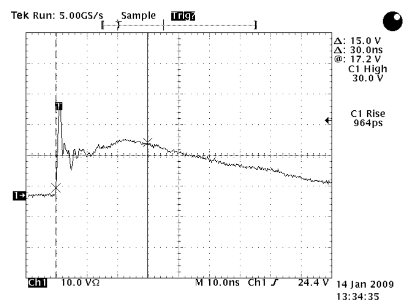
Testing





- Comparison of 61000-4-2 waveform to measured waveform

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Testing

- ESD testing is easily affected by outside influences –
  - Tolerances associated with test equipment
  - Test setup anomalies including:
    - Improper bonding/test arrangement
    - Improper application of Discharges
    - Temperature and Humidity

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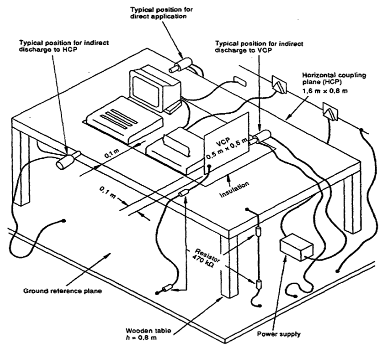
Testing

- ☞ Things Mama didn't tell us -
- ☞ Table-top testing
  - ☞ Bleed resistors
  - ☞ Insulating Material
  - ☞ Coupling of cables to table top



Dimensions in metres

Figure 5 – Example of test set-up for table-top equipment – Laboratory tests

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Testing

- ☞ More things Mama didn't tell us -
- ☞ Floor-standing testing
  - ☞ Arrangement of Generator return cable
  - ☞ EUT cable arrangement
  - ☞ Don't hold the VCP with your hand!

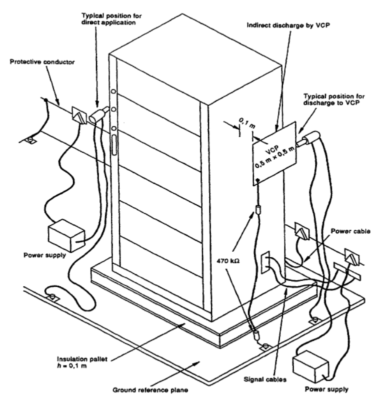

Figure 6 – Example of test set-up for floor standing equipment, laboratory tests

Testing

- Approach for Debug – Who Me?
  - Setup issues associated with the Equipment under Test and Associated Support Equipment (Could be the Test Lab – I'm off the hook)
  - Setup issues associated the test generation side of things including Climatic conditions (those Lab guys again)
  - OK – I guess it's the product
    - Since we've already followed all the rules what next?

Testing

- Since we're looking at the product now – start painting with a wide brush
  - Evaluate for deviations from the design guidelines – verify and mitigate if possible
  - Consider Software/Functionality issues
  - Examine the characteristics of the problem
  - Isolate Operationally – software/hardware/other
  - Isolate Physically
    - Probe position – discharge application
    - Near field probing using decreasing levels
    - Once sensitive circuits are located, treat accordingly
    - Leave Rube Goldberg modifications in place until the problem is solved then back out changes individually for effect

Summary – Q & A

- Summary –
  - Begin with sound design and installation practices
  - If you're still in trouble the use of a logical, systematic and consistent evaluation of all of the possible contributing factors will eventually drill down to the root cause
  - Given the characteristics of the problem, start with a wide perspective
  - Don't give up -

???

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