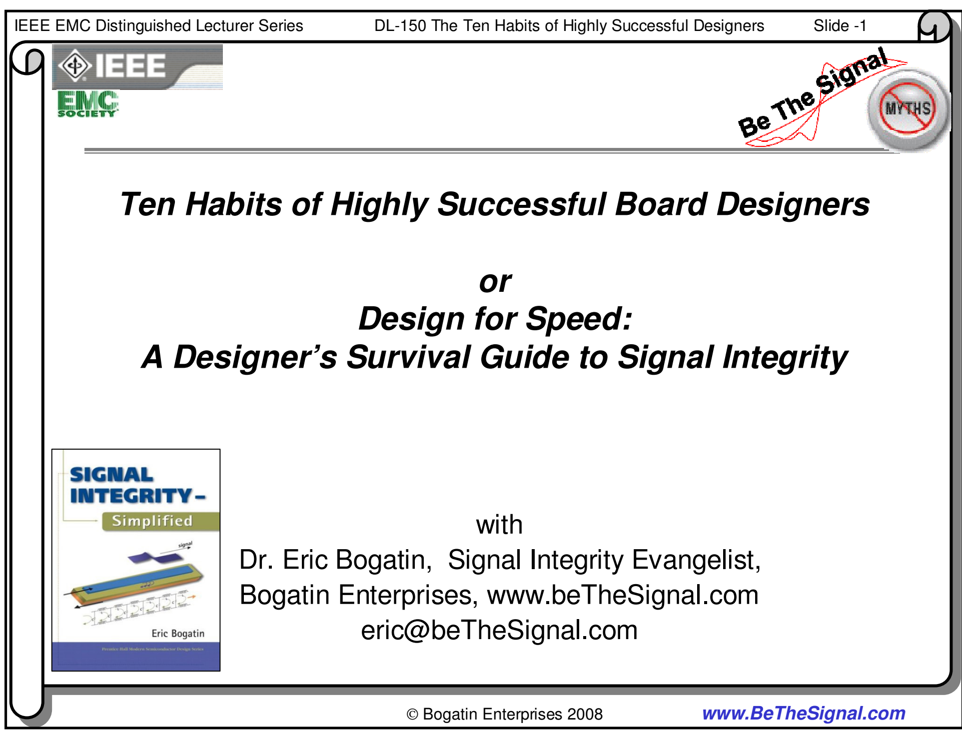
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DL-150 The Ten Habits of Highly Successful Designers
Slide -1
IEEE
EMC SOCIETY
Be The Signal
MYTHS
Ten Habits of Highly Successful Board Designers
or
Design for Speed:
A Designer's Survival Guide to Signal Integrity
SIGNAL INTEGRITY –
Simplified
Eric Bogatin
with
Dr. Eric Bogatin, Signal Integrity Evangelist,
Bogatin Enterprises, www.beTheSignal.com
eric@beTheSignal.com
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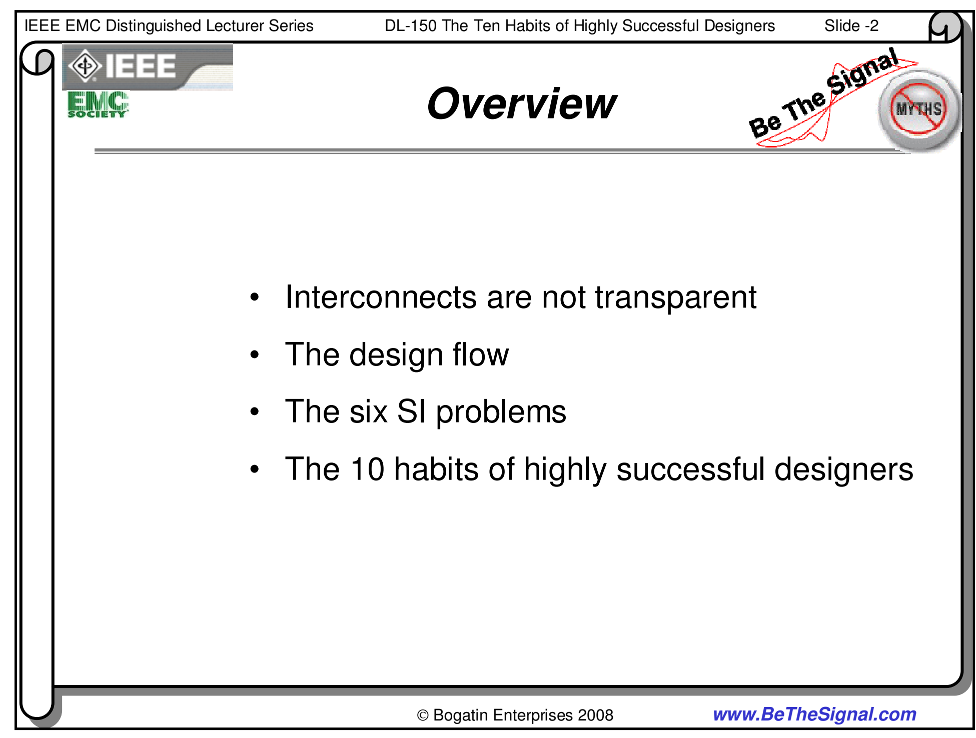
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DL-150 The Ten Habits of Highly Successful Designers
Slide -2
IEEE
EMC SOCIETY
Overview
Be The Signal
MYTHS
• Interconnects are not transparent
• The design flow
• The six SI problems
• The 10 habits of highly successful designers
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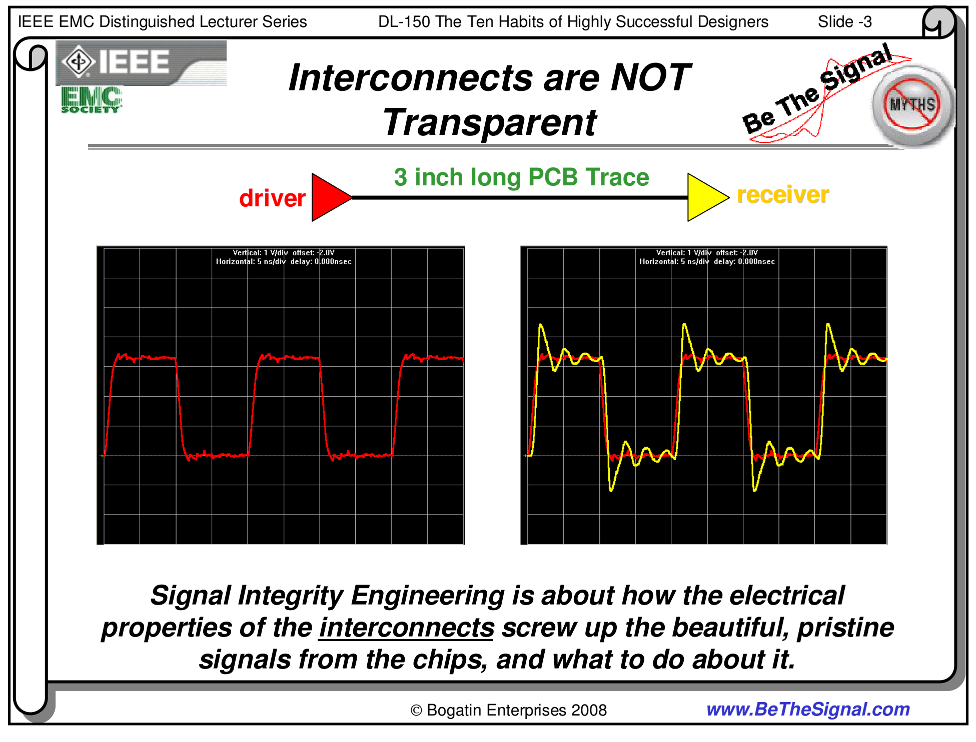
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Slide -3
Interconnects are NOT Transparent
Be The Signal
MYTHS
driver
3 inch long PCB Trace
receiver
Signal Integrity Engineering is about how the electrical properties of the interconnects screw up the beautiful, pristine signals from the chips, and what to do about it.
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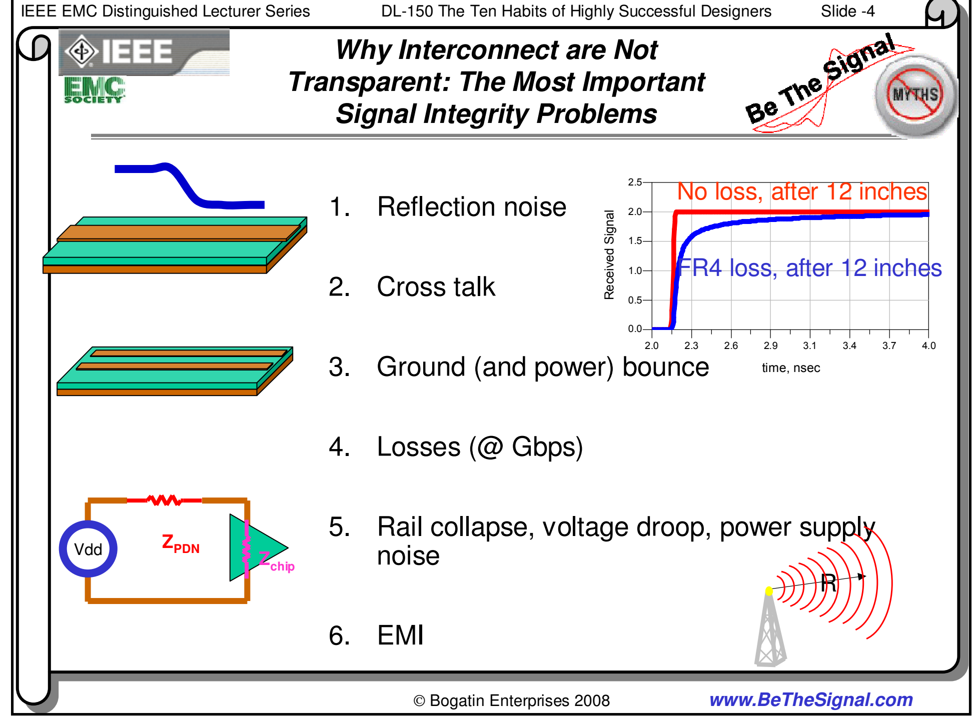
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Slide -4
Why Interconnect are Not Transparent: The Most Important Signal Integrity Problems
Be The Signal
MYTHS
1. Reflection noise
2. Cross talk
3. Ground (and power) bounce
4. Losses (@ Gbps)
5. Rail collapse, voltage droop, power supply noise
6. EMI
No loss, after 12 inches
FR4 loss, after 12 inches
Received Signal
time, nsec
Vdd
Z PDN
Z chip
R
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IEEE
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Hope Can't be Part of the Design Strategy in High-Speed Products
Be The Signal
MYTHS
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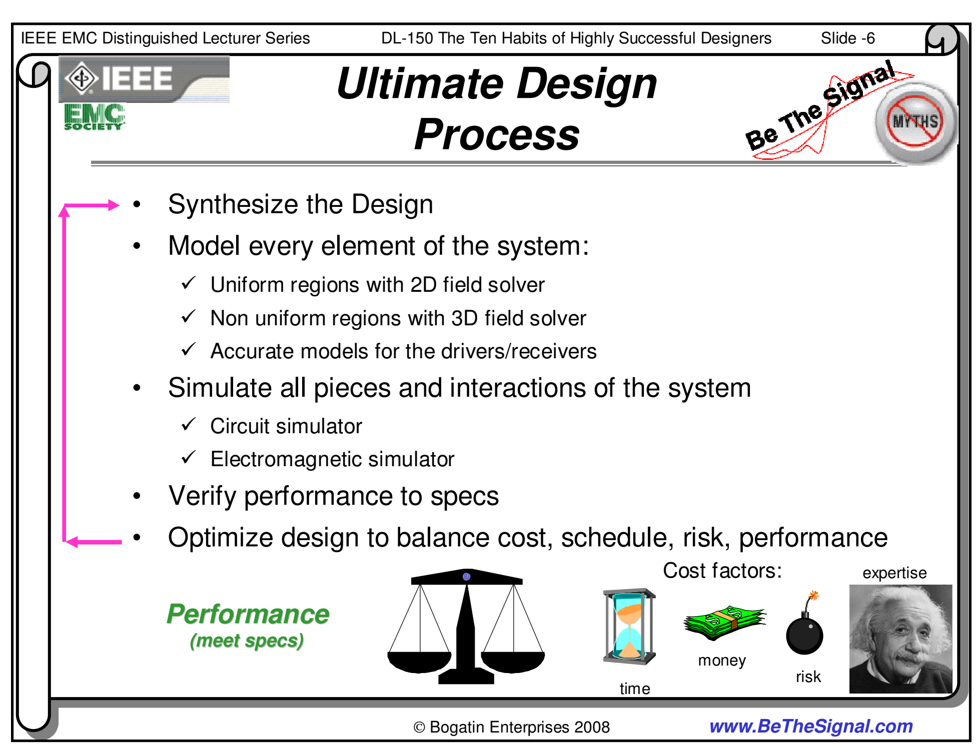
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DL-150 The Ten Habits of Highly Successful Designers
Slide -6
IEEE
EMC SOCIETY
Ultimate Design Process
Be The Signal
MYTHS
Synthesize the Design
Model every element of the system:
Uniform regions with 2D field solver
Non uniform regions with 3D field solver
Accurate models for the drivers/receivers
Simulate all pieces and interactions of the system
Circuit simulator
Electromagnetic simulator
Verify performance to specs
Optimize design to balance cost, schedule, risk, performance
Performance
(meet specs)
Cost factors:
time
money
risk
expertise
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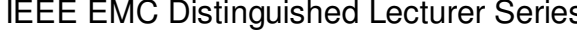

A Practical Design Process

- Design with good habits that result in a robust design
  - ✓ Watch out for the six problems
  - ✓ Identify their root cause
  - ✓ Establish design guidelines (habits) to minimize the problems based on their root cause
  - ✓ Rely on your intuition, based on the essential principles, to guide you in design tradeoffs
  - ✓ Minimize risk using appropriate analysis tools given the budget: expertise, $$, risk, time

"… the more you know, the luckier you get"

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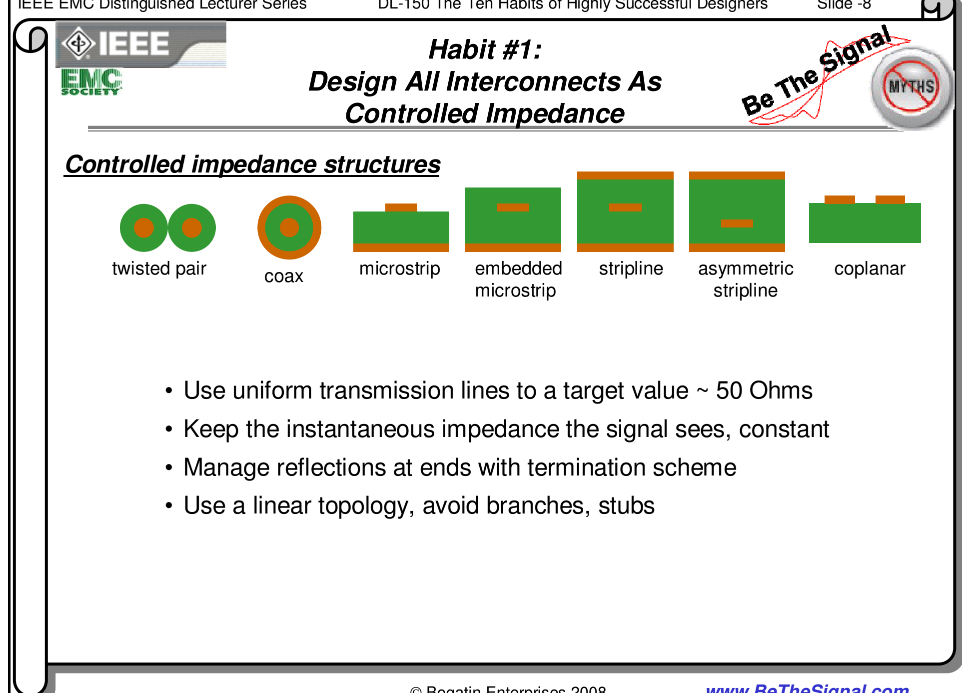

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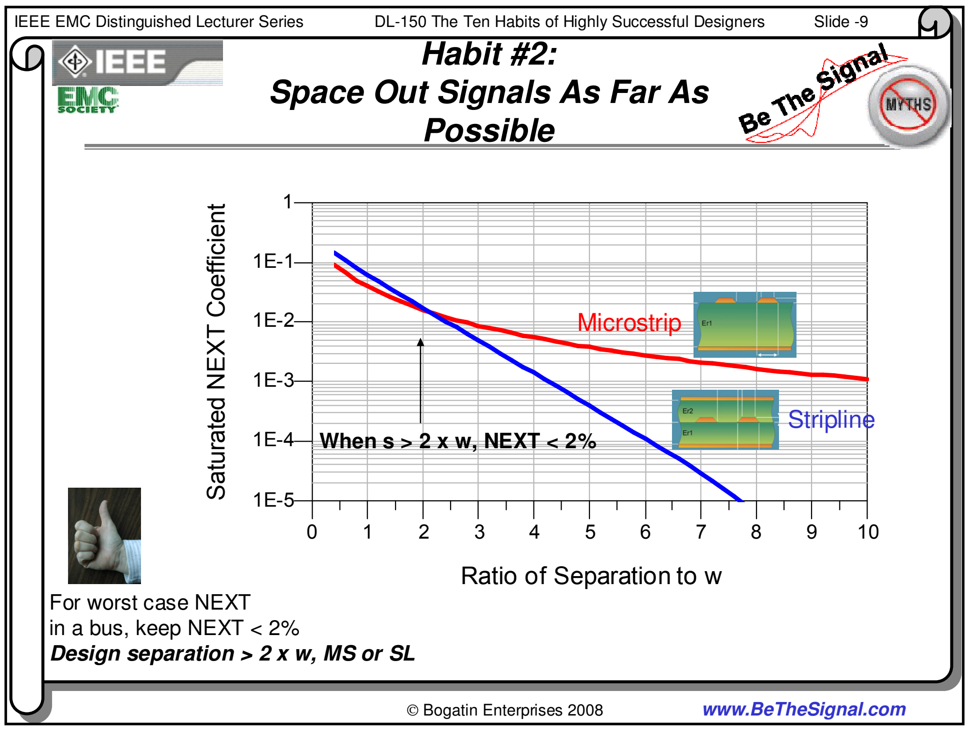
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Slide -9
Habit #2:
Space Out Signals As Far As Possible
Be The Signal
MYTHS
Saturated NEXT Coefficient
1
1E-1
1E-2
1E-3
1E-4
1E-5
0
1
2
3
4
5
6
7
8
9
10
Ratio of Separation to w
Microstrip
Stripline
When s > 2 x w, NEXT < 2%
For worst case NEXT
in a bus, keep NEXT < 2%
Design separation > 2 x w, MS or SL
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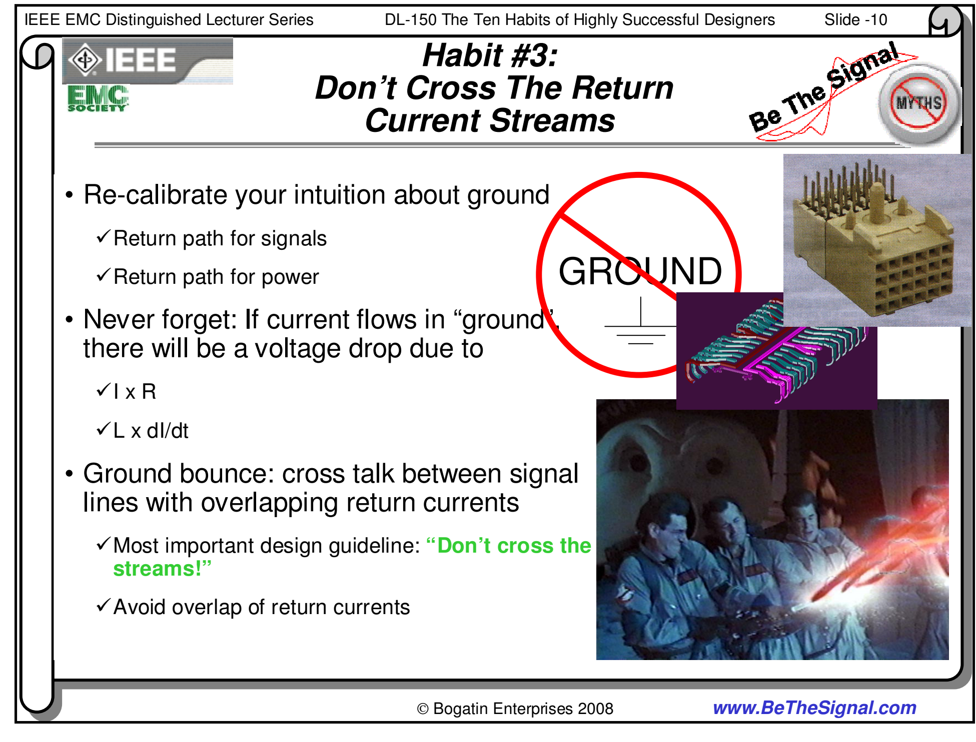
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Slide -10
Habit #3:
Don't Cross The Return Current Streams
Be The Signal
MYTHS
• Re-calibrate your intuition about ground
✓Return path for signals
✓Return path for power
• Never forget: If current flows in "ground", there will be a voltage drop due to
✓I x R
✓L x dI/dt
• Ground bounce: cross talk between signal lines with overlapping return currents
✓Most important design guideline: "Don't cross the streams!"
✓Avoid overlap of return currents
GROUND
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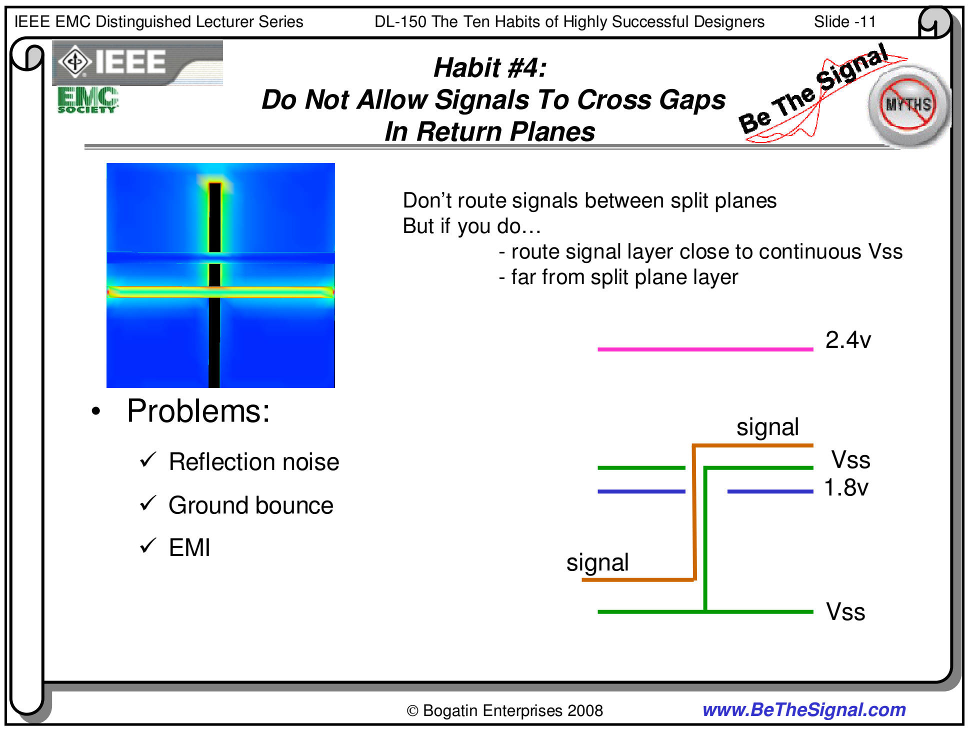
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Slide -11
IEEE
EMC SOCIETY
Habit #4:
Do Not Allow Signals To Cross Gaps
In Return Planes
Be The Signal
MYTHS
Don't route signals between split planes
But if you do…
- route signal layer close to continuous Vss
- far from split plane layer
2.4v
Problems:
Reflection noise
Ground bounce
EMI
signal
Vss
1.8v
signal
Vss
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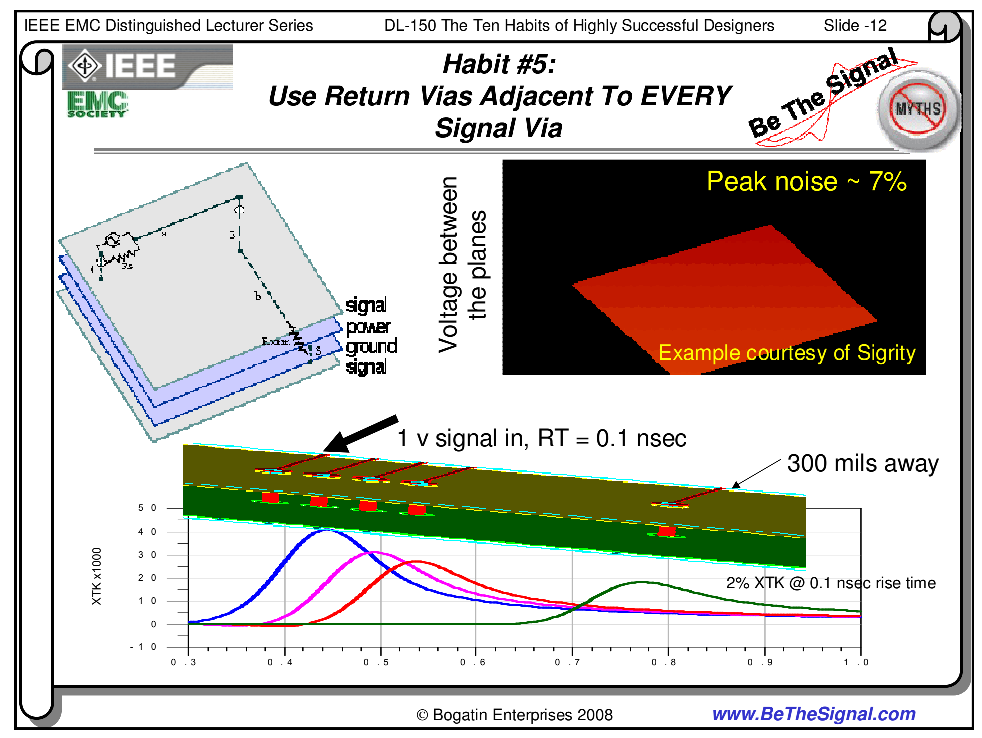
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Slide -12
IEEE
EMC SOCIETY
Habit #5:
Use Return Vias Adjacent To EVERY
Signal Via
Be The Signal
MYTHS
signal
power
ground
signal
Voltage between the planes
Peak noise ~ 7%
Example courtesy of Sigrity
1 v signal in, RT = 0.1 nsec
300 mils away
XTK x1000
2% XTK @ 0.1 nsec rise time
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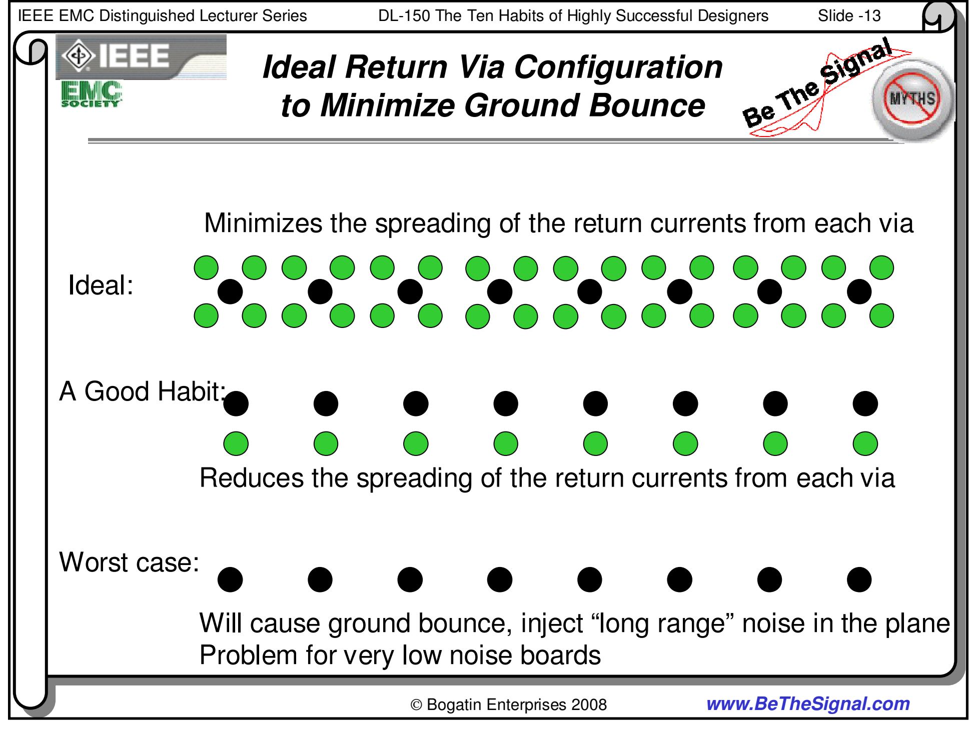
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Slide -13
Ideal Return Via Configuration
to Minimize Ground Bounce
Be The Signal
MYTHS
Minimizes the spreading of the return currents from each via
Ideal:
A Good Habit:
Reduces the spreading of the return currents from each via
Worst case:
Will cause ground bounce, inject “long range” noise in the plane
Problem for very low noise boards
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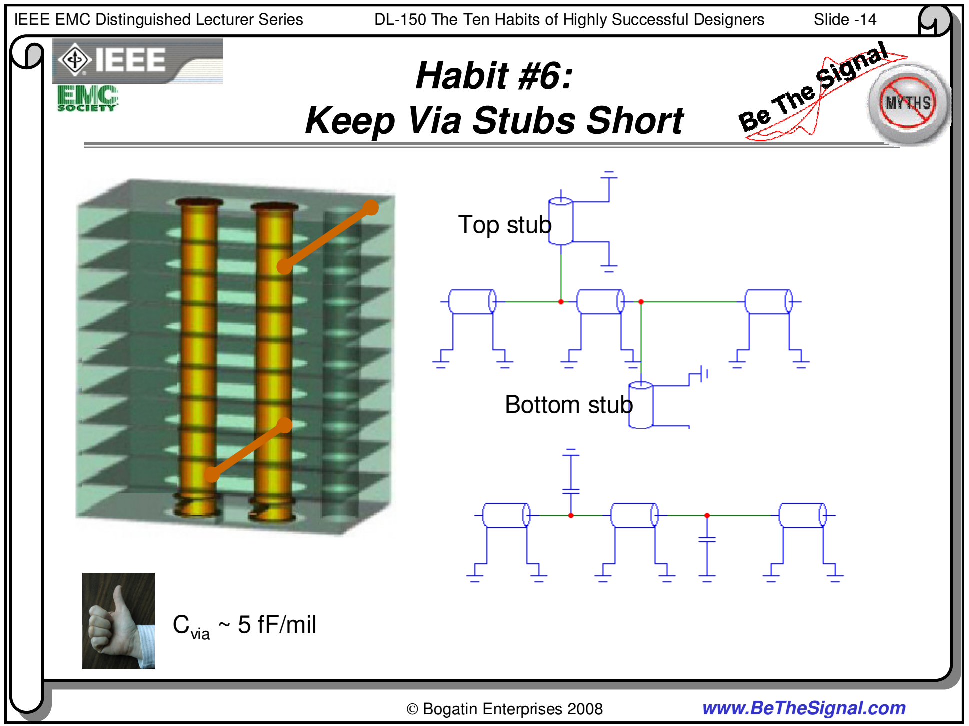
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Slide -14
Habit #6:
Keep Via Stubs Short
Be The Signal
MYTHS
Top stub
Bottom stub
C_{via} ~ 5 fF/mil
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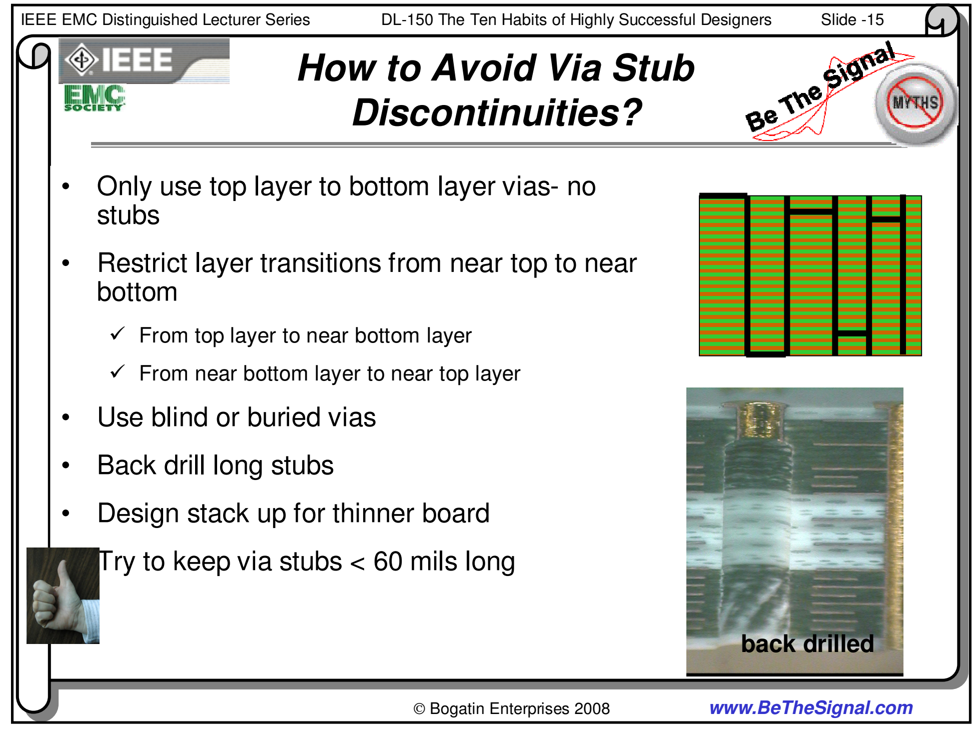
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Slide -15
IEEE
EMC SOCIETY
How to Avoid Via Stub Discontinuities?
Be The Signal
MYTHS
Only use top layer to bottom layer vias- no stubs
Restrict layer transitions from near top to near bottom
From top layer to near bottom layer
From near bottom layer to near top layer
Use blind or buried vias
Back drill long stubs
Design stack up for thinner board
Try to keep via stubs < 60 mils long
back drilled
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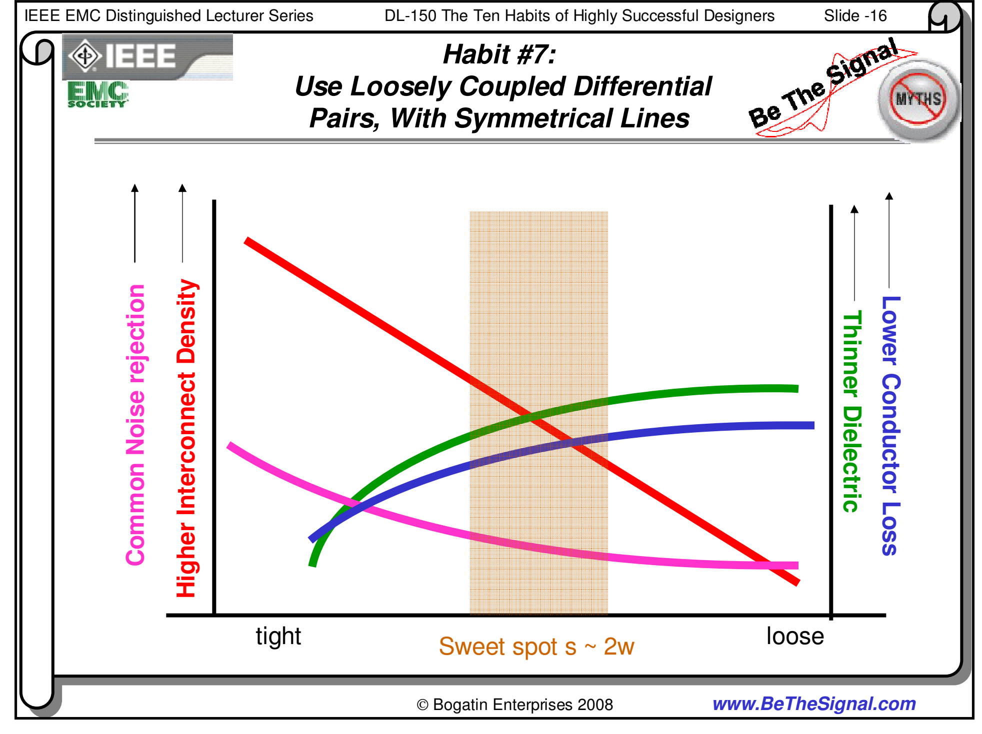
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Slide -16
IEEE
EMC SOCIETY
Habit #7:
Use Loosely Coupled Differential Pairs, With Symmetrical Lines
Be The Signal
MYTHS
Common Noise rejection
Higher Interconnect Density
Thinner Dielectric
Lower Conductor Loss
tight
Sweet spot s ~ 2w
loose
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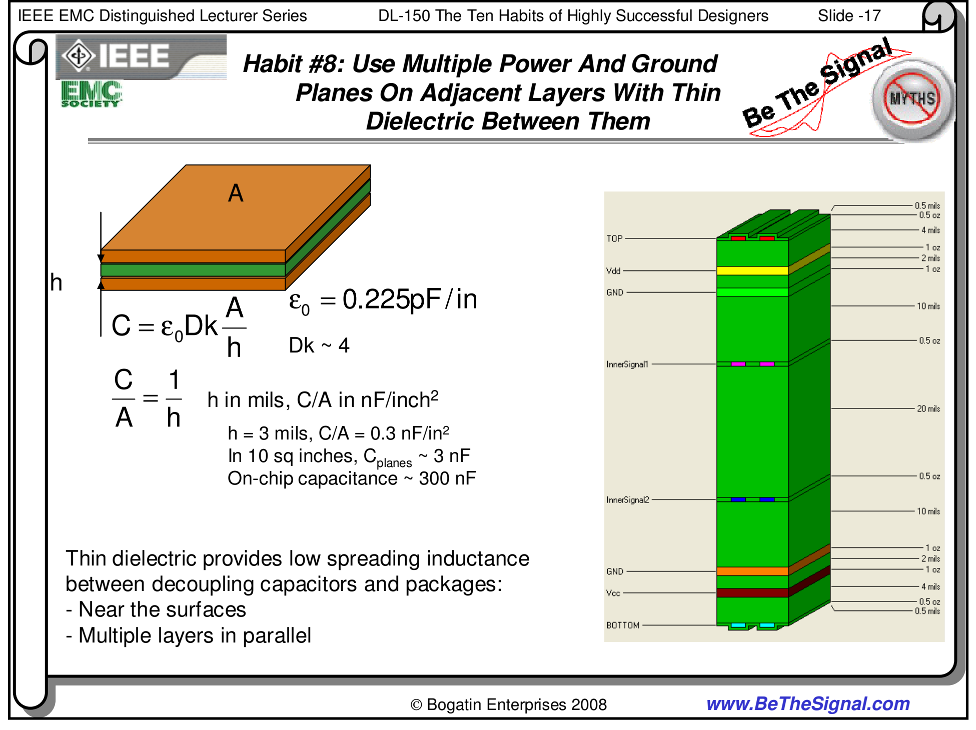
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Slide -17
Habit #8: Use Multiple Power And Ground Planes On Adjacent Layers With Thin Dielectric Between Them
Be The Signal
MYTHS
A
h
$C = \varepsilon_0 Dk \frac{A}{h}$
$\varepsilon_0 = 0.225 pF/in$
Dk ~ 4
$\frac{C}{A} = \frac{1}{h}$
h in mils, C/A in nF/inch²
h = 3 mils, C/A = 0.3 nF/in²
In 10 sq inches, C_{planes} ~ 3 nF
On-chip capacitance ~ 300 nF
Thin dielectric provides low spreading inductance between decoupling capacitors and packages:
- Near the surfaces
- Multiple layers in parallel
TOP
Vdd
GND
InnerSignal1
InnerSignal2
GND
Vcc
BOTTOM
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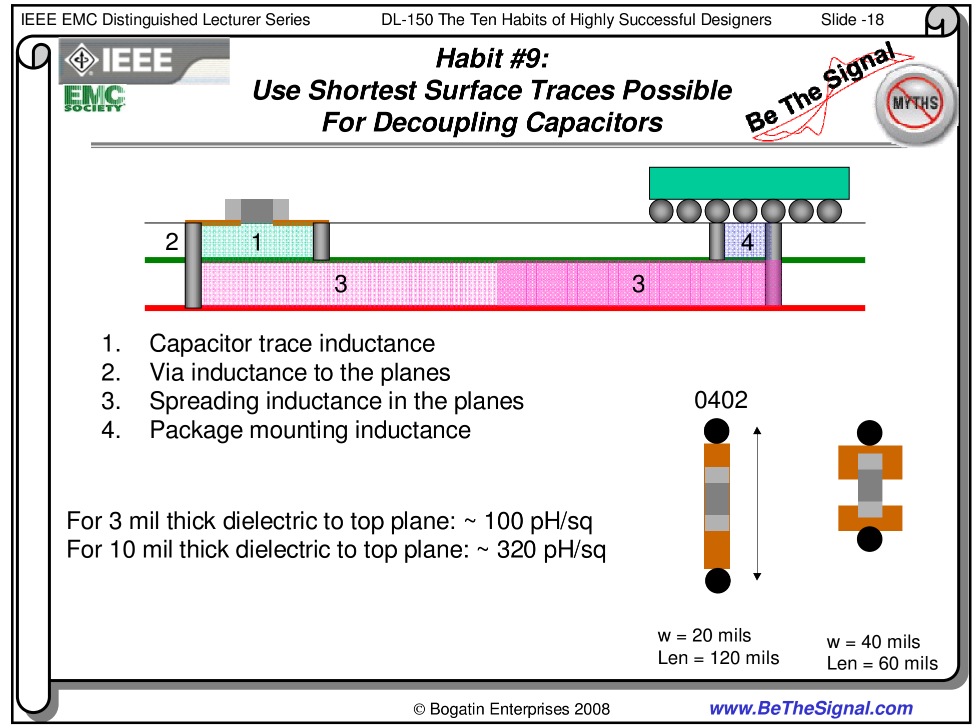
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Slide -18
Habit #9: Use Shortest Surface Traces Possible For Decoupling Capacitors
Be The Signal
MYTHS
2
1
3
3
4
1. Capacitor trace inductance
2. Via inductance to the planes
3. Spreading inductance in the planes
4. Package mounting inductance
For 3 mil thick dielectric to top plane: ~ 100 pH/sq
For 10 mil thick dielectric to top plane: ~ 320 pH/sq
0402
w = 20 mils
Len = 120 mils
w = 40 mils
Len = 60 mils
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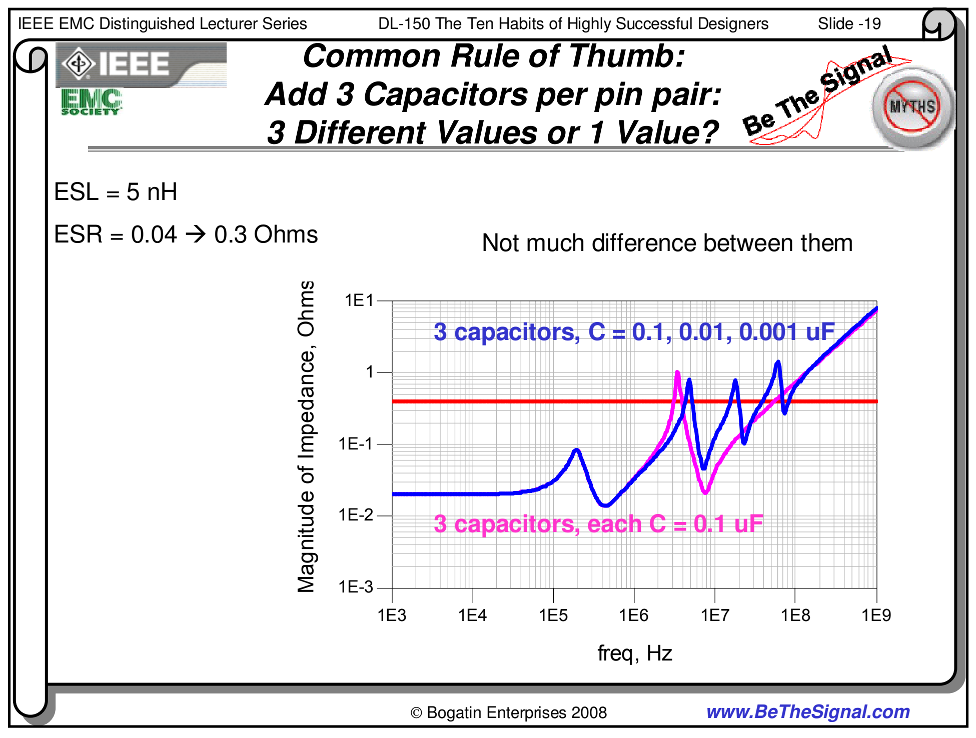
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Slide -19
IEEE
EMC SOCIETY
Common Rule of Thumb:
Add 3 Capacitors per pin pair:
3 Different Values or 1 Value?
Be The Signal
MYTHS
ESL = 5 nH
ESR = 0.04 → 0.3 Ohms
Not much difference between them
3 capacitors, C = 0.1, 0.01, 0.001 uF
3 capacitors, each C = 0.1 uF
Magnitude of Impedance, Ohms
1E1
1
1E-1
1E-2
1E-3
1E3
1E4
1E5
1E6
1E7
1E8
1E9
freq, Hz
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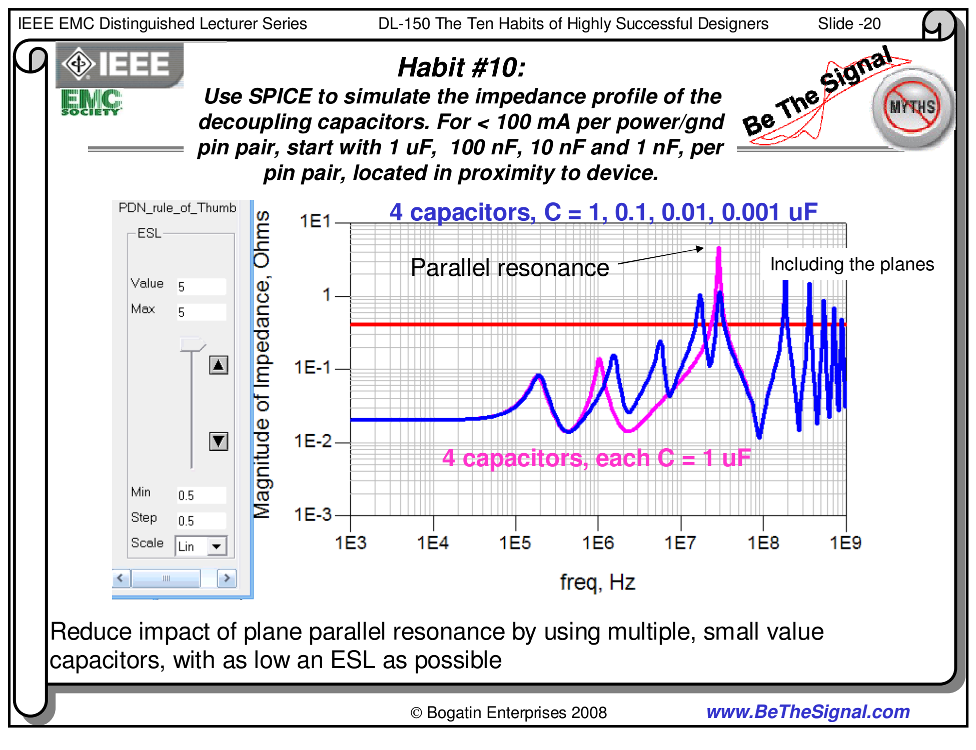
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Slide -20
IEEE
EMC SOCIETY
Habit #10:
Use SPICE to simulate the impedance profile of the decoupling capacitors. For < 100 mA per power/gnd pin pair, start with 1 uF, 100 nF, 10 nF and 1 nF, per pin pair, located in proximity to device.
Be The Signal
MYTHS
PDN_rule_of_Thumb
ESL
Value 5
Max 5
Min 0.5
Step 0.5
Scale Lin
4 capacitors, C = 1, 0.1, 0.01, 0.001 uF
Parallel resonance
Including the planes
4 capacitors, each C = 1 uF
Magnitude of Impedance, Ohms
1E1
1
1E-1
1E-2
1E-3
1E3
1E4
1E5
1E6
1E7
1E8
1E9
freq, Hz
Reduce impact of plane parallel resonance by using multiple, small value capacitors, with as low an ESL as possible
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The Ten Habits of Highly Successful Designers

1. Design all interconnects as controlled impedance
2. Space out signals as far as possible
3. Don’t cross the return current streams
4. Do not allow signals to cross gaps in return planes
5. Use return vias adjacent to EVERY signal via
6. Keep via stubs short
7. Use loosely coupled differential pairs, with symmetrical lines
8. Use multiple power and ground planes on adjacent layers with thin dielectric between them
9. Use shortest surface traces possible for decoupling capacitors
10. Use SPICE to simulate the impedance profile of the decoupling capacitors. For < 100 mA per power/gnd pin pair, start with 1 uF, 100 nF, 10 nF and 1 nF, per pin pair, located in proximity to device.

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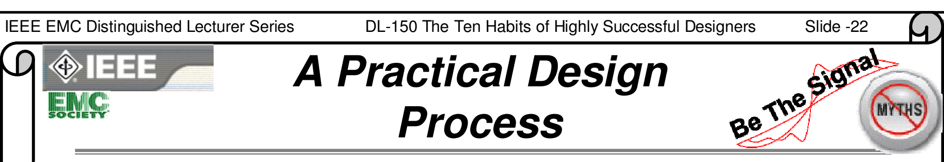

A Practical Design Process

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  - ✓ Identify their root cause
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