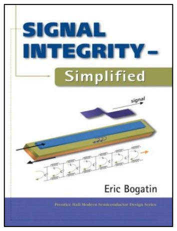
Be The Signal

Ten Habits of Highly Successful Board Designers

or
Design for Speed:
A Designer's Survival Guide to Signal Integrity



SIGNAL INTEGRITY – Simplified

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with
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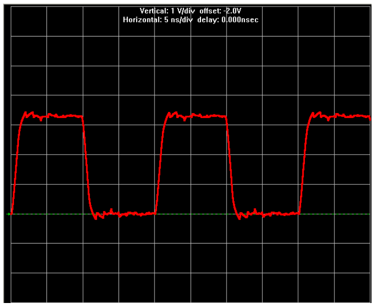
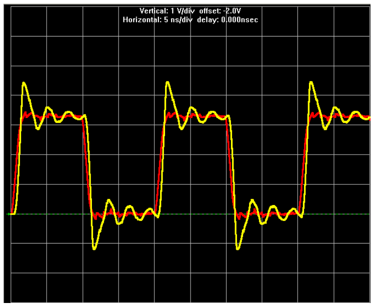
Overview

Be The Signal

- Interconnects are not transparent
- The design flow
- The six SI problems
- The 10 habits of highly successful designers

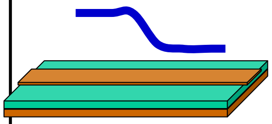
Interconnects are NOT Transparent

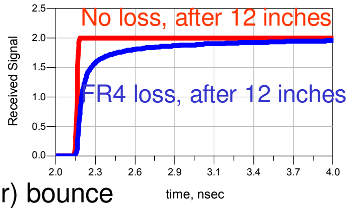




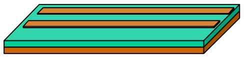
Signal Integrity Engineering is about how the electrical properties of the interconnects screw up the beautiful, pristine signals from the chips, and what to do about it.

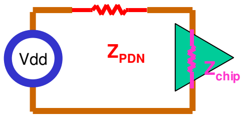
Why Interconnect are Not Transparent: The Most Important Signal Integrity Problems

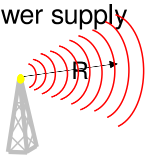




1. Reflection noise
2. Cross talk
3. Ground (and power) bounce
4. Losses (@ Gbps)
5. Rail collapse, voltage droop, power supply noise
6. EMI





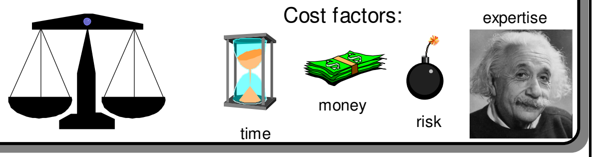


Hope Can't be Part of the Design Strategy in High-Speed Products

Ultimate Design Process

- Synthesize the Design
- Model every element of the system:
  - ✓ Uniform regions with 2D field solver
  - ✓ Non uniform regions with 3D field solver
  - ✓ Accurate models for the drivers/receivers
- Simulate all pieces and interactions of the system
  - ✓ Circuit simulator
  - ✓ Electromagnetic simulator
- Verify performance to specs
- Optimize design to balance cost, schedule, risk, performance

Performance
(meet specs)



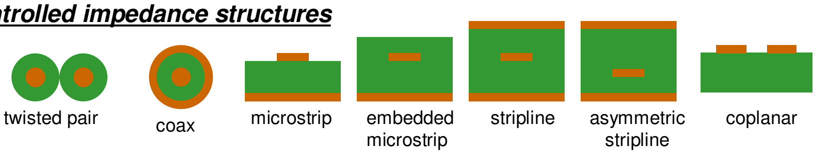
A Practical Design Process

- Design with good habits that result in a robust design
  - ✓ Watch out for the six problems
  - ✓ Identify their root cause
  - ✓ Establish design guidelines (habits) to minimize the problems based on their root cause
  - ✓ Rely on your intuition, based on the essential principles, to guide you in design tradeoffs
  - ✓ Minimize risk using appropriate analysis tools given the budget: expertise, $$, risk, time

"… the more you know, the luckier you get"

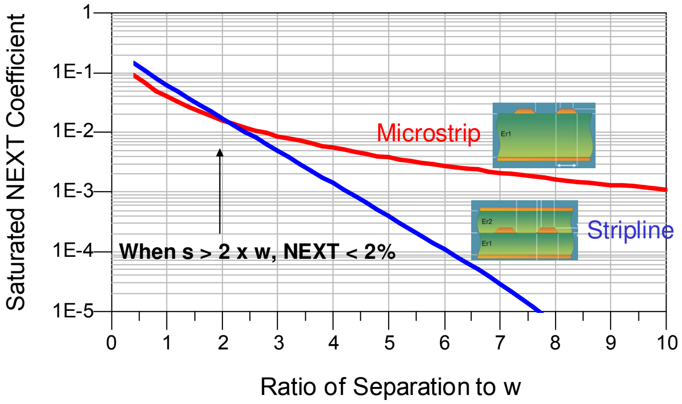
Habit #1: Design All Interconnects As Controlled Impedance

Controlled impedance structures



- Use uniform transmission lines to a target value ~ 50 Ohms
- Keep the instantaneous impedance the signal sees, constant
- Manage reflections at ends with termination scheme
- Use a linear topology, avoid branches, stubs

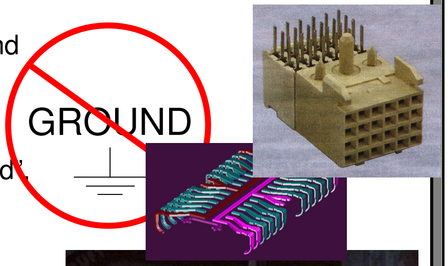
Habit #2: Space Out Signals As Far As Possible



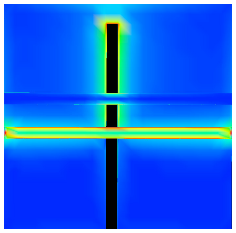
For worst case NEXT
in a bus, keep NEXT < 2%
Design separation > 2 x w, MS or SL

Habit #3: Don't Cross The Return Current Streams

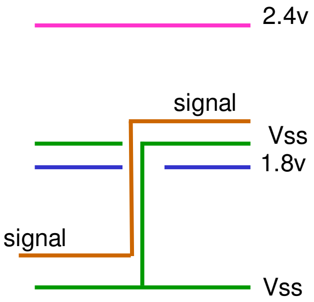
- Re-calibrate your intuition about ground
  - ✓Return path for signals
  - ✓Return path for power
- Never forget: If current flows in "ground", there will be a voltage drop due to
  - ✓I x R
  - ✓L x dI/dt
- Ground bounce: cross talk between signal lines with overlapping return currents
  - ✓Most important design guideline: **"Don't cross the streams!"**
  - ✓Avoid overlap of return currents



Habit #4:
Do Not Allow Signals To Cross Gaps In Return Planes

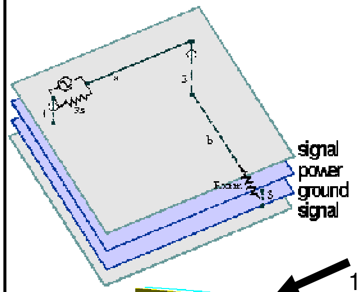


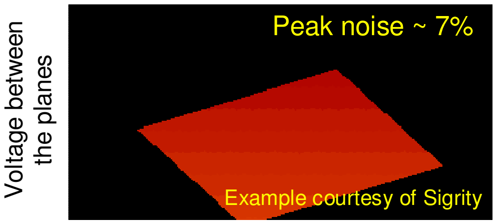
Don’t route signals between split planes
But if you do…
- route signal layer close to continuous Vss
- far from split plane layer



- Problems:
  - ✓ Reflection noise
  - ✓ Ground bounce
  - ✓ EMI

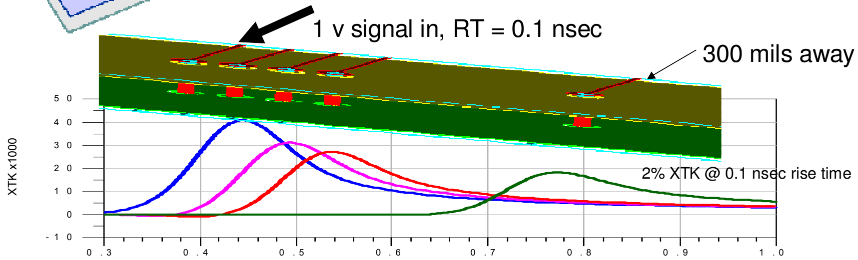
Habit #5:
Use Return Vias Adjacent To EVERY Signal Via





Peak noise ~ 7%

Example courtesy of Sigrity



1 v signal in, RT = 0.1 nsec

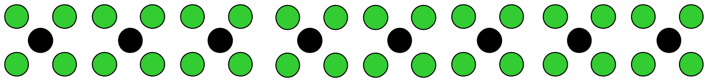
300 mils away

2% XTK @ 0.1 nsec rise time

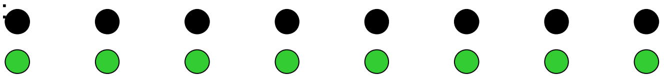
Ideal Return Via Configuration to Minimize Ground Bounce

Minimizes the spreading of the return currents from each via

Ideal:



A Good Habit:

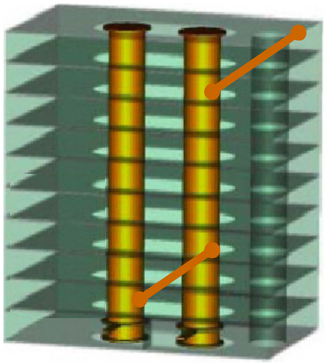


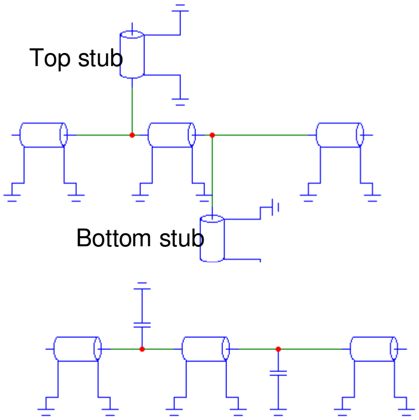
Reduces the spreading of the return currents from each via

Worst case:

Will cause ground bounce, inject “long range” noise in the plane
Problem for very low noise boards

Habit #6:
Keep Via Stubs Short



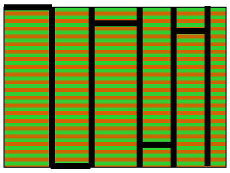


C_{via} ~ 5 fF/mil

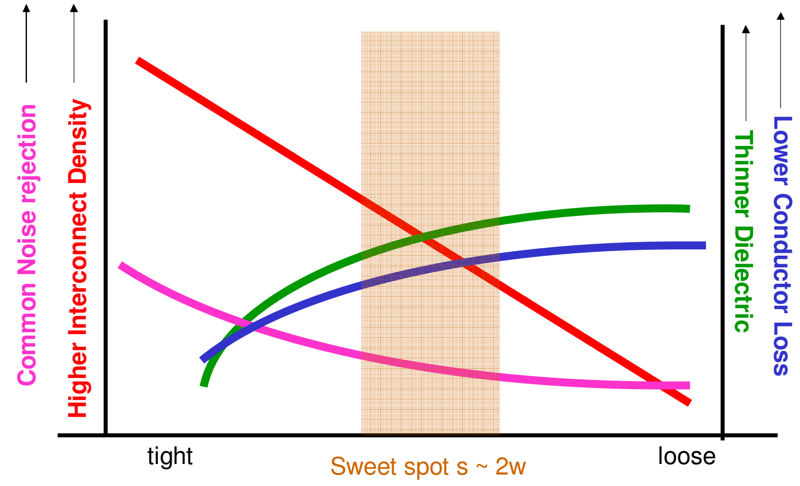
How to Avoid Via Stub Discontinuities?

- Only use top layer to bottom layer vias- no stubs
- Restrict layer transitions from near top to near bottom
  - ✓ From top layer to near bottom layer
  - ✓ From near bottom layer to near top layer
- Use blind or buried vias
- Back drill long stubs
- Design stack up for thinner board

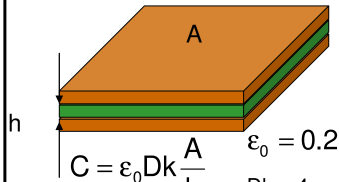
Try to keep via stubs < 60 mils long



Habit #7: Use Loosely Coupled Differential Pairs, With Symmetrical Lines



Habit #8: Use Multiple Power And Ground Planes On Adjacent Layers With Thin Dielectric Between Them



$$C = \varepsilon_0 Dk \frac{A}{h}$$

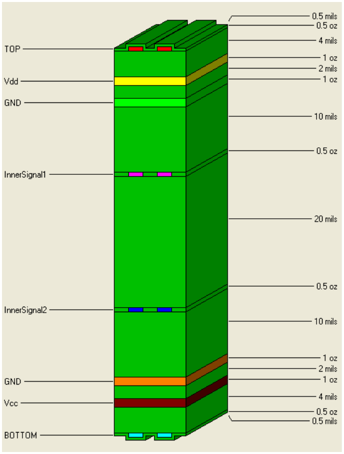
$$\varepsilon_0 = 0.225\text{pF}/\text{in}$$

Dk ~ 4

$$\frac{C}{A} = \frac{1}{h}$$

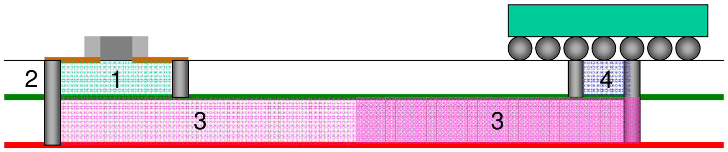
h in mils, C/A in nF/inch^2

h = 3 mils, C/A = 0.3 nF/in^2
In 10 sq inches, C_{planes} ~ 3 nF
On-chip capacitance ~ 300 nF

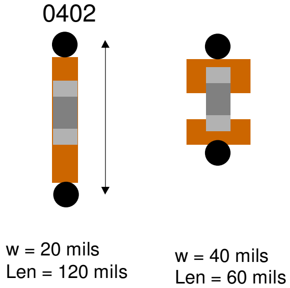


Thin dielectric provides low spreading inductance between decoupling capacitors and packages:
- Near the surfaces
- Multiple layers in parallel

Habit #9: Use Shortest Surface Traces Possible For Decoupling Capacitors



1. Capacitor trace inductance
2. Via inductance to the planes
3. Spreading inductance in the planes
4. Package mounting inductance



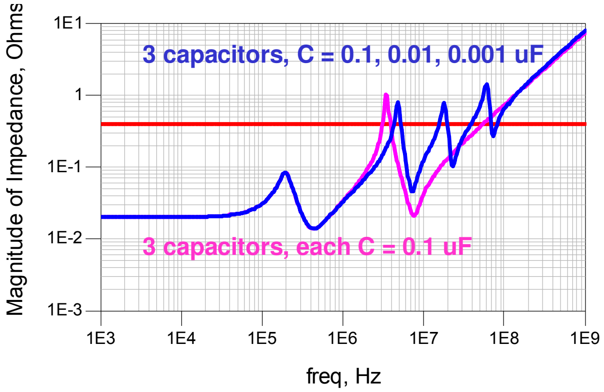
For 3 mil thick dielectric to top plane: ~ 100 pH/sq
For 10 mil thick dielectric to top plane: ~ 320 pH/sq

Common Rule of Thumb: Add 3 Capacitors per pin pair: 3 Different Values or 1 Value?

ESL = 5 nH

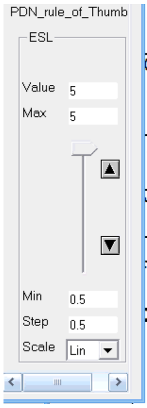
ESR = 0.04 → 0.3 Ohms

Not much difference between them



Habit #10:

Use SPICE to simulate the impedance profile of the decoupling capacitors. For < 100 mA per power/gnd pin pair, start with 1 uF, 100 nF, 10 nF and 1 nF, per pin pair, located in proximity to device.


PDN_rule_of_Thumb

ESL

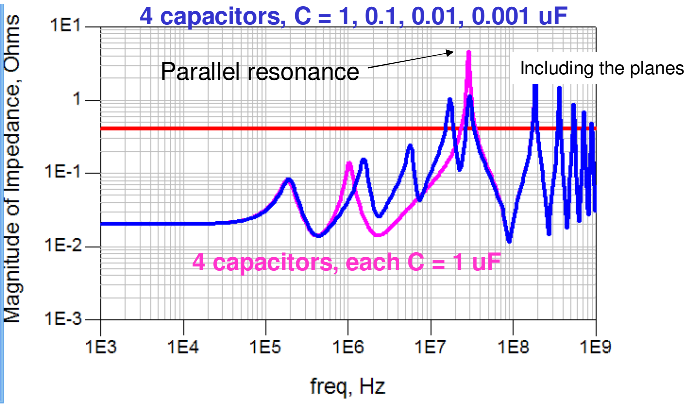
Value 5

Max 5

Min 0.5

Step 0.5

Scale Lin



Reduce impact of plane parallel resonance by using multiple, small value capacitors, with as low an ESL as possible

The Ten Habits of Highly Successful Designers

1. Design all interconnects as controlled impedance
2. Space out signals as far as possible
3. Don’t cross the return current streams
4. Do not allow signals to cross gaps in return planes
5. Use return vias adjacent to EVERY signal via
6. Keep via stubs short
7. Use loosely coupled differential pairs, with symmetrical lines
8. Use multiple power and ground planes on adjacent layers with thin dielectric between them
9. Use shortest surface traces possible for decoupling capacitors
10. Use SPICE to simulate the impedance profile of the decoupling capacitors. For < 100 mA per power/gnd pin pair, start with 1 uF, 100 nF, 10 nF and 1 nF, per pin pair, located in proximity to device.

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