MICROSYSTEMS AND NANOSYSTEMS: MANUFACTURING CHALLENGES AND OPPORTUNITIES

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Outlines

- Introduction
- History of the Nano World
- Materials and Processing Challenges
- Disruptive Technologies
- Energy Conversion Area
- Chip and Packaging Manufacturing Innovation
- New Computer Architecture
- Innovative Design
- Platform Integration
- New Business Opportunities
- Conclusion

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Microsystems

- Microminiaturized and integrated systems based on microelectronics, photonics, RF, micro-electro-mechanical systems (MEMS) and packaging technologies.

- Source: http://www.eppic-faraday.com/glossary.html

Nanosystems

- The nanosystem may consist one or more of the following functional components: electronic, optical, magnetic, mechanical, chemical, biological, energy sources, and various type of the sensing devices.
- At least one of these functional devices must be in 0.1-100 nm dimensions.

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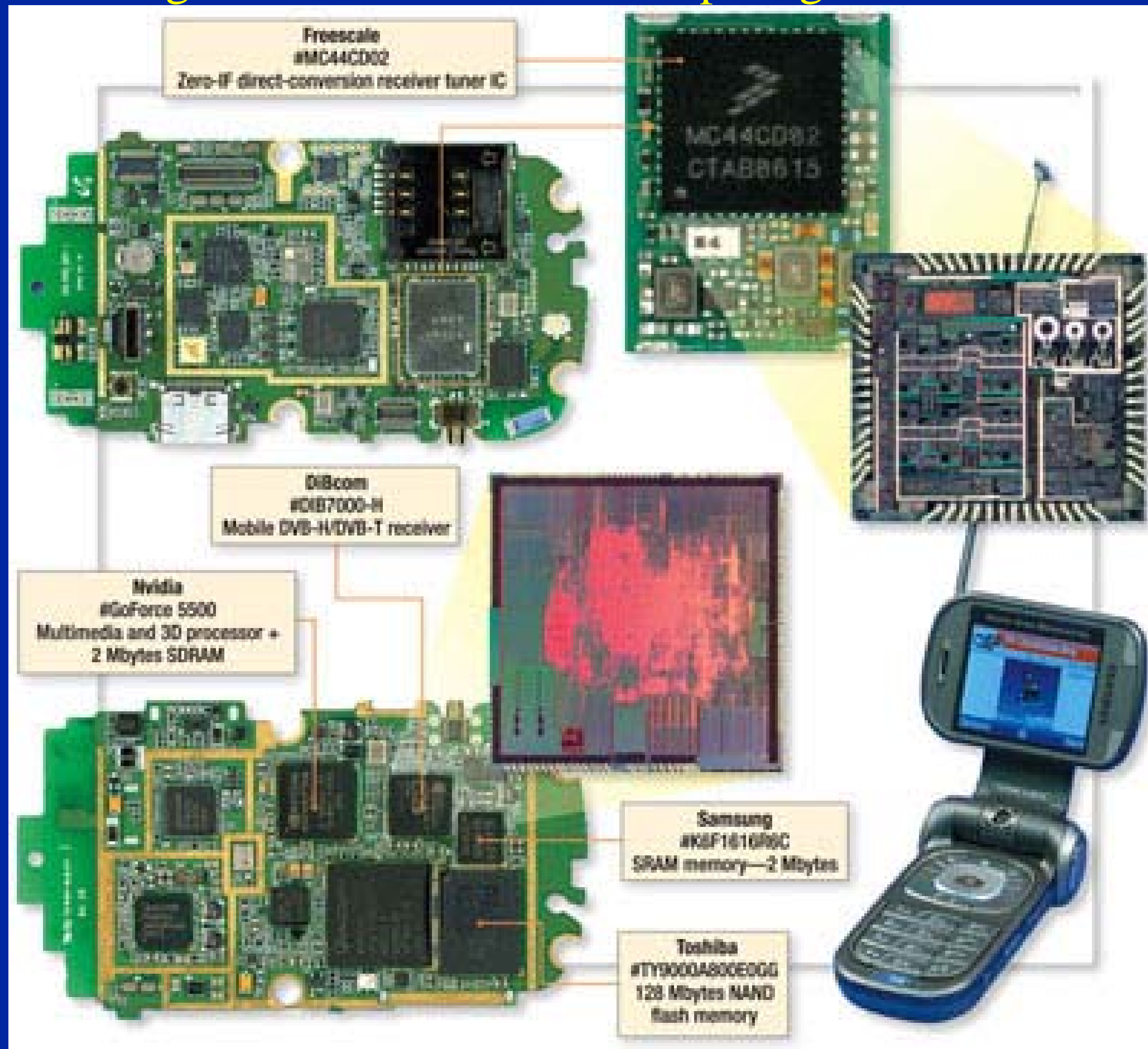
Example of Nanosystem

Samsung's Mobile Phone Dials up Digital TV



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INTRODUCTION OF THE NANO WORLD

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How Small?

- Length: 4.05×10^{-35} m (Planck Distance)
- Time: 1.35×10^{-43} s (Planck Time)
- Planck scale number set the ultimate limits on the performance of computers
- Black Holes as the potential material
- Source: N. Gershenfeld "The Physics of Information Technology", Cambridge Press

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Real World

- Current: 1.0×10^{-15}A
- Time: 1.0×10^{-15} s (~ 1.0×10^{-18} s)
- One Atom (0.1 nm diameter)

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Life: Perspective

Matter	Dimension (nm)
Atom	0.1
DNA Width	2
Protein	5-50
Virus	75-100
Materials internalized by cells	< 100
Bacteria	1,000-10,000
White Blood Cell	10,000

Nanoelectronics

- Manufacturing of 45 nm Feature size silicon integrated circuits will start in early 2008
- Know how to use materials in dimension of about 45 nm X 90 nm are available for any kind of devices to be manufactured today

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Unique Opportunities

- Global Agriculture industry ~ $1.9 Trillion
- Global Electronics industry ~ $1.5 Trillion $
- Global Power Generation Industry ~ $1.1 Trillion and will grow to $2.25 Trillion in the next two decades
- Drug Industry ~ 0.5 Trillion $
- Agriculture industry has flat or very small growth
- It is possible that in the next one or two decades Electronics industry may be bigger than Agriculture Industry

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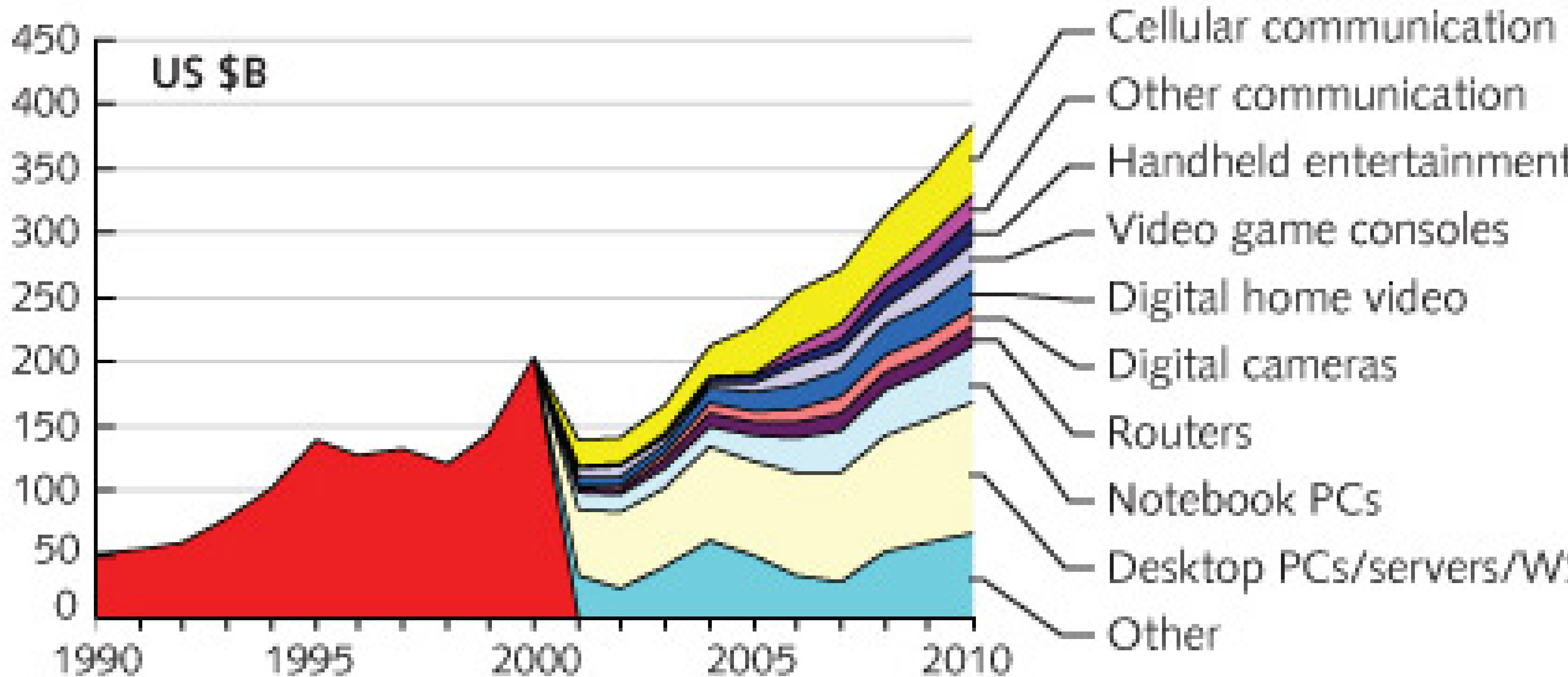
Semiconductor Market



Open Question

- From 45 nm Feature size devices today to devices down to 0.1 nm ??
- Old Way: Top Down Approach (Lithography)
- New Way: Bottom Up (One atom or few atoms at one time)
- UNIQUE OPPORUNITIES TO FIND PATHWAYS BY OLD , NEW OR COMBINED WAYS TO MANUFACTURE FUTURE INFORMATION PROCESSING NANO SYSTEMS

Eternal Laws of Nature

- Laws of Physics can not be changed with any amount of resources (time & money)
- Materials as small as a single atom also follows the laws of thermodynamics

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Focus on Fundamentals

- "A diode is not capable of gain and so it cannot serve as an active circuit element"
- Ref: James D. Meindl , " Microelectronic Circuit Elements", Scientific Americans, vol. 237 # 3, pp. 70-81, 1977
- In mid 80s as Project Director of multi-million $ DARPA funded research project we worked only on 3 terminal devices and rejected offers to develop 2 terminal based logic devices
- Smart ways : "Phase Shift Mask leading & other optical corrections" leading to sub-wavelength photolithography

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Fundamental Understanding

Centimeter:	Gravity, friction, combustion
Millimeter:	Gravity, friction, combustion, Electrostatic
Micrometer:	Electrostatic, van der Walls, Brownian
Nanometer:	Electrostatic, van der Walls, Brownian, Quantum
Angstrom:	Quantum mechanics

HISTORY OF NAO WORLD

ORIGIN OF NANO WORLD

- Vedas are the oldest books known to mankind
- Nano World is based on atoms
- Idea of atom documented in Vedas
- "In the end of chaotic state the physical forces were endowed with the energy to assume the form of creation. There did get rise the multitude of atoms full of motion."

  RIG VEDA 10-72.6

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In the Beginning - 4,000 BCE

Nano World of the 20th Century

- Nano-size carbon black particles have gone into tires for 100 years as a reinforcing additive, long before the prefix "nano" ever created a stir.
- A vaccine, which often consists of one or more proteins with nanoscale dimensions, is also qualified as nanomaterial

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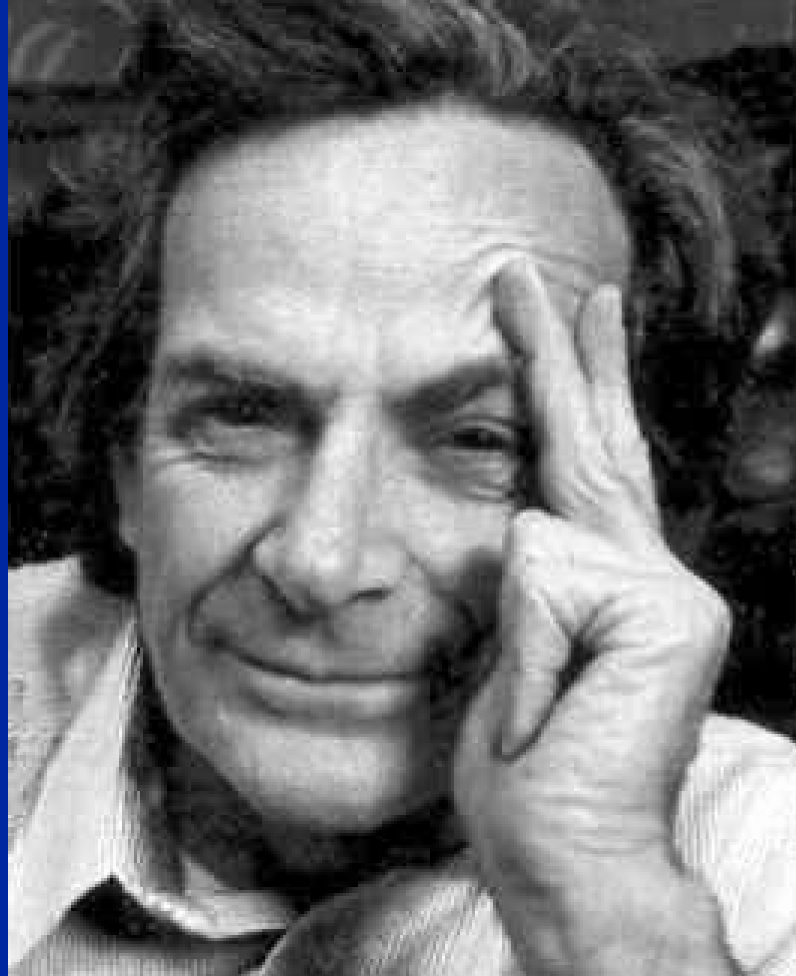
Richard P. Feynman



Feynman's Vision

- *"The principles of physics, as far as I can see, do not speak against the possibility of maneuvering things atom by atom. It is not an attempt to violate any laws; it is something, in principle that can be done; but in practice, it has not been done because we are too big."*
- -Richard Feynman, 1959, at Caltech
- **There's plenty of room at the bottom**

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My Own First Hand Experience of the Nano World

1-2 nm thick gate dielectric based MOS device as Solar Cells

Ph. D. Thesis , McMaster University, 1979

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Scanning Tunneling Microscope

- Binning and Rohrer invented Scanning tunneling microscope (STM) in 1982
- STM can only scan conductive samples
- They invented atomic force microscope (AFM) in 1985
- They won Nobel Prize in Physics in 1986

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Nano-positioning

The ability to precisely position a device with a precision measured in nanometers depends on

- encoder resolution
- controller resolution
- amplifier noise
- D/A resolution and
- stability

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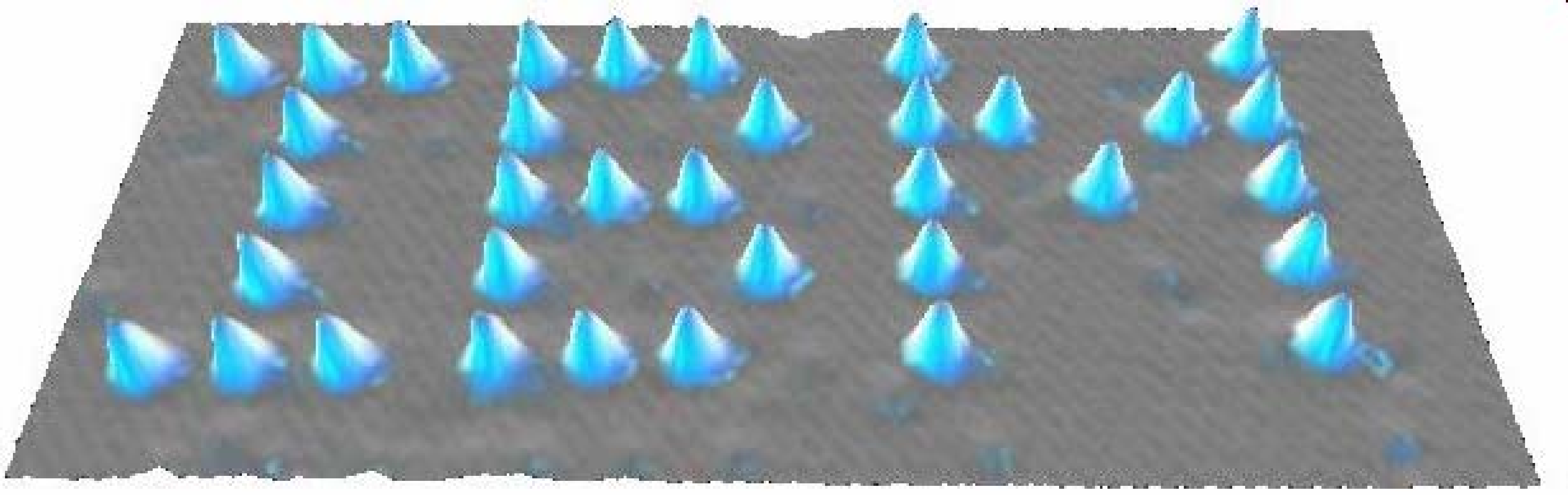
IBM - 1985



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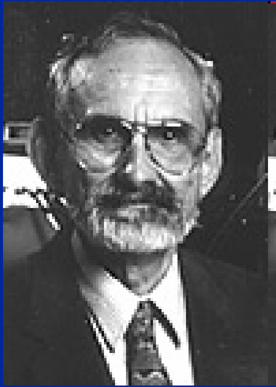
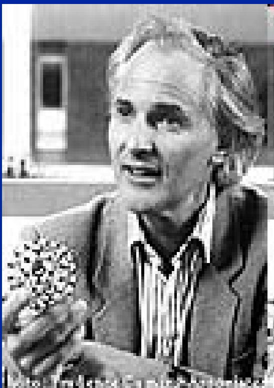
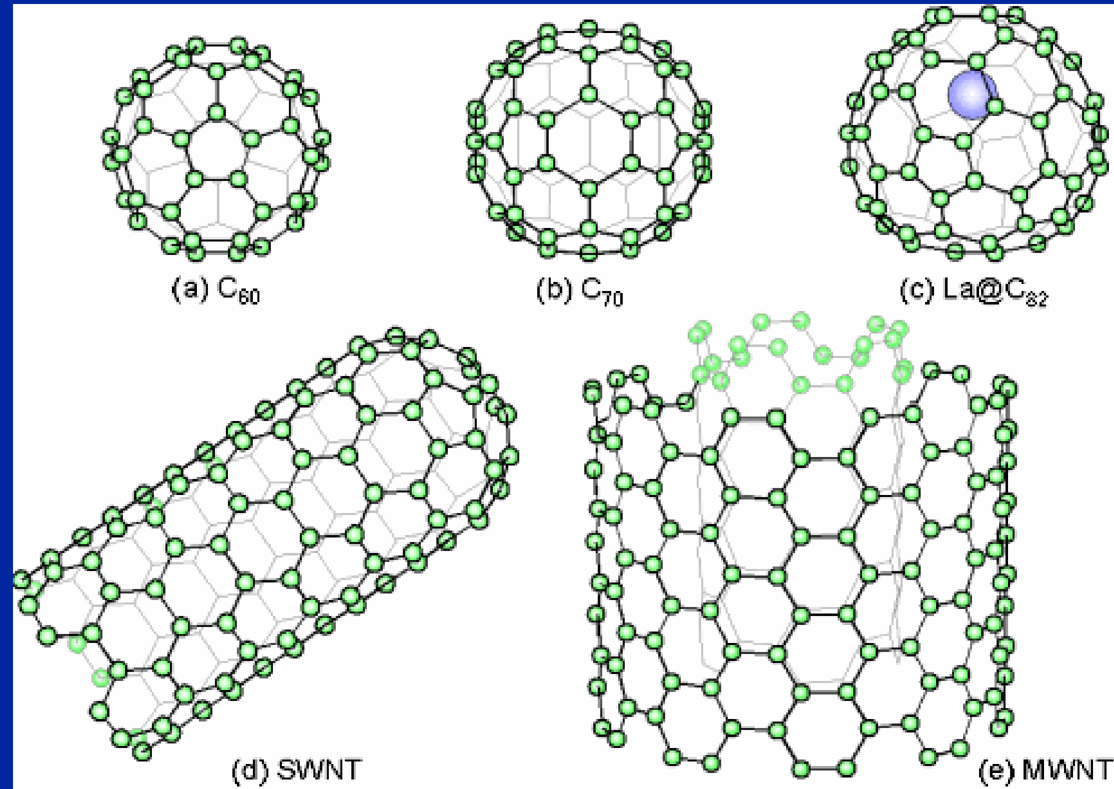
Fullerenes – 1985 (1996)


Robert F. Curl Jr.

Richard E. Smalley


Sir Harold W. Kroto



What is new in the Nano World?

- Using better signal to noise ratio instruments many new phenomena have been observed
- Opaque substances become transparent (copper)
- Inert materials become catalysts (platinum)
- Stable materials turn combustible (aluminum)
- Solid turn into liquid at room temperature (gold)
- Source: Semiconductor International , Jan 2007,

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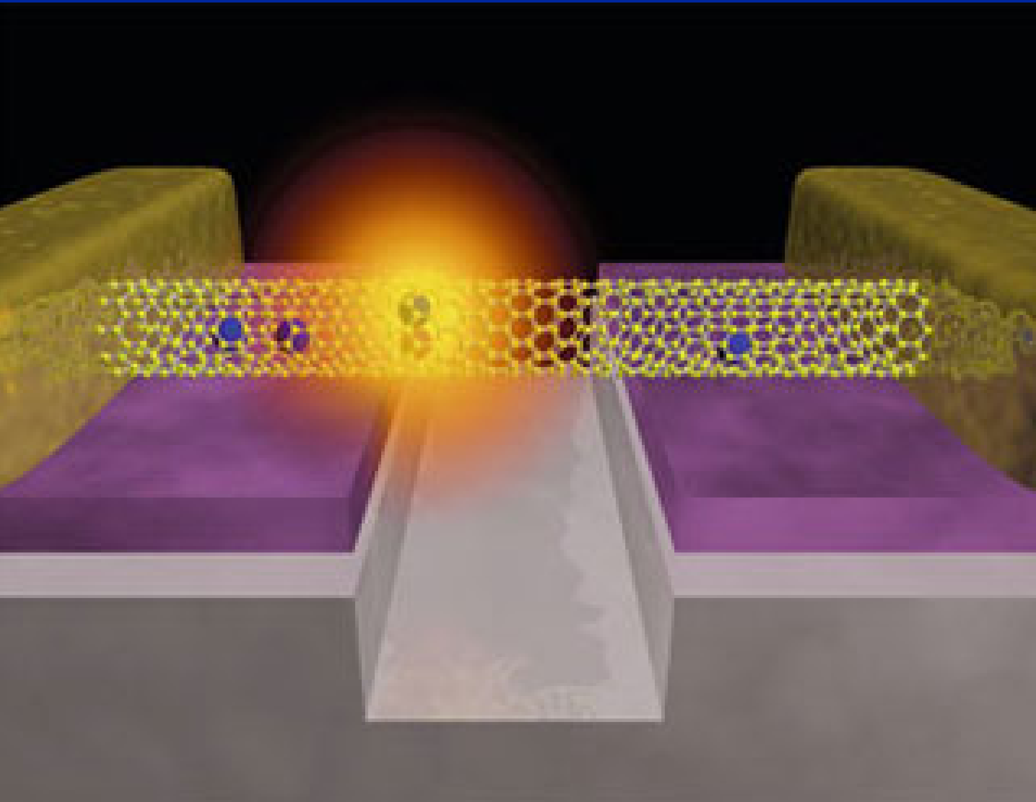
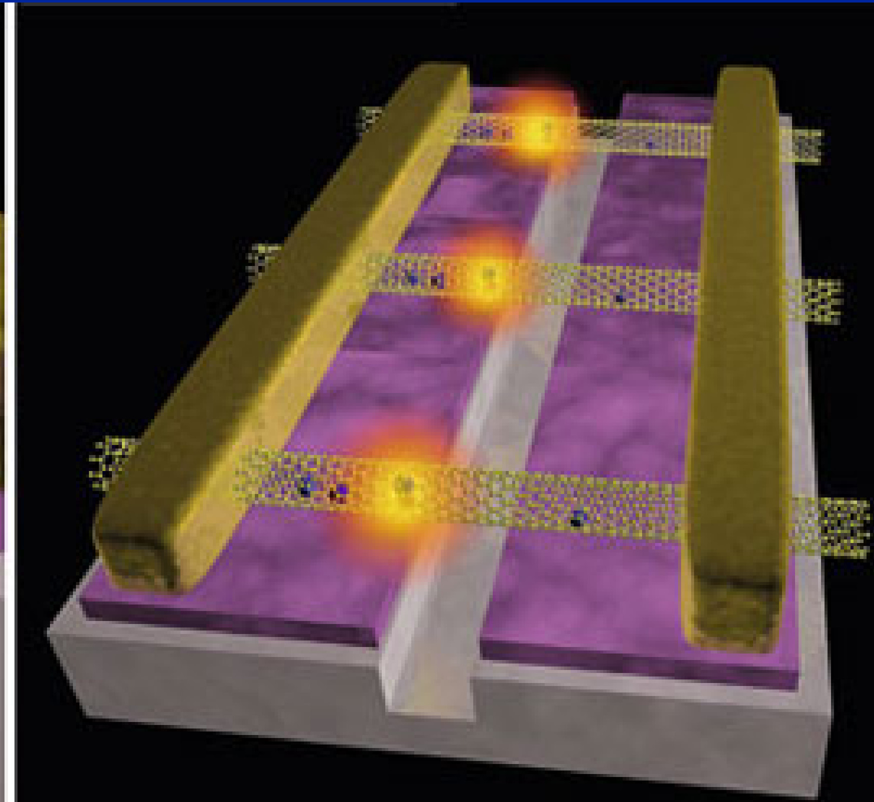
Carbon Nanotube (Semi. Int. Jan 2007, IBM Work)





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MATERIALS AND PROCESSING CHALLENGES

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Self Assembly

Understand and control the intra-molecular quantum behavior of specifically designed and synthesized molecules using a surface to localize and stabilize them.

To interconnect, assemble and test nano devices and nano-machines starting from atomic or molecular parts

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Self Assembly (cont..)

- The meanings of "Self Assembly" have been taken wrongly
- All you see around is selective chemistry
- True self assembly process involve programmed cell death or apoptosis(M. T. Heemels, *Nature*, 407, 769,2000).

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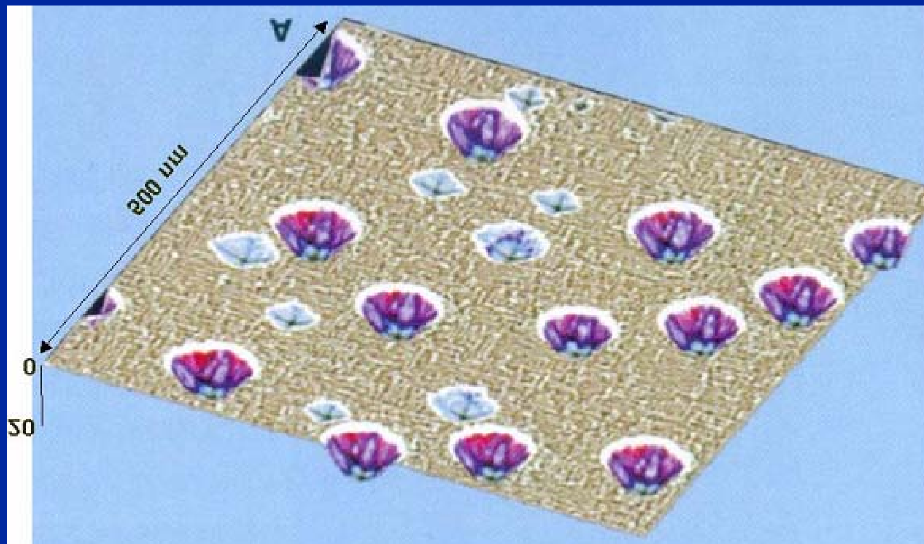
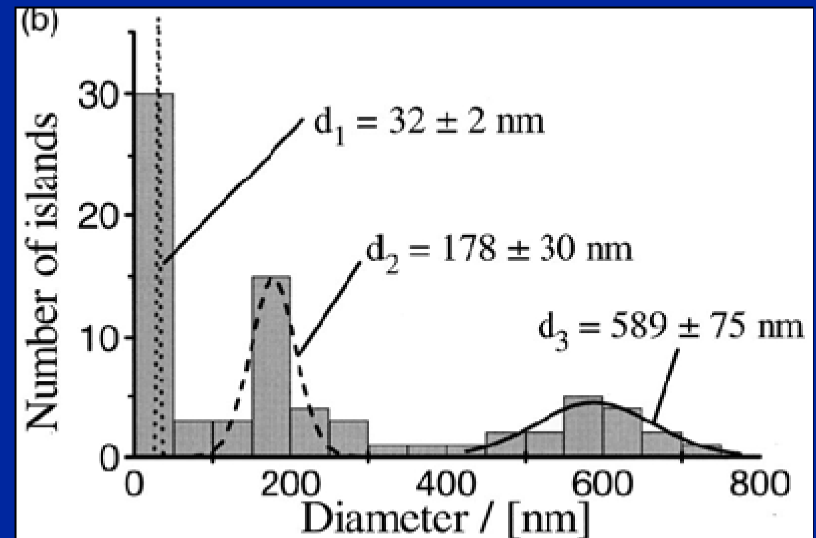
Size Distribution Problem (N. Motta, J. Phys.)





Challenges in Self Directed Assembly (Future Fab Int. Jan 2007)

Metric	Requirement
Defects and defect management strategies	Comparable to current systems
Low Frequency LER	~1.5 nm 3σ
Long Range CD Control	~1.2 nm 3σ
Resolution	11 nm
Essential shapes	Dense and Isolated L/S, circles, hexagonal arrays, jogs
Overlay and registration	5.1 nm 3σ
Throughput	1 W/Min
Etch and pattern transfer	~Novolak
Placement and orientation	Under development
Multiple Sizes-Pitches/Layer Overall Performance	2-3/layer
Other	

Table 2. Near-term Materials Performance Requirements for Directed Self-Assembly

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R. Singh Proc. IBM Conf. on SiO2, 1978

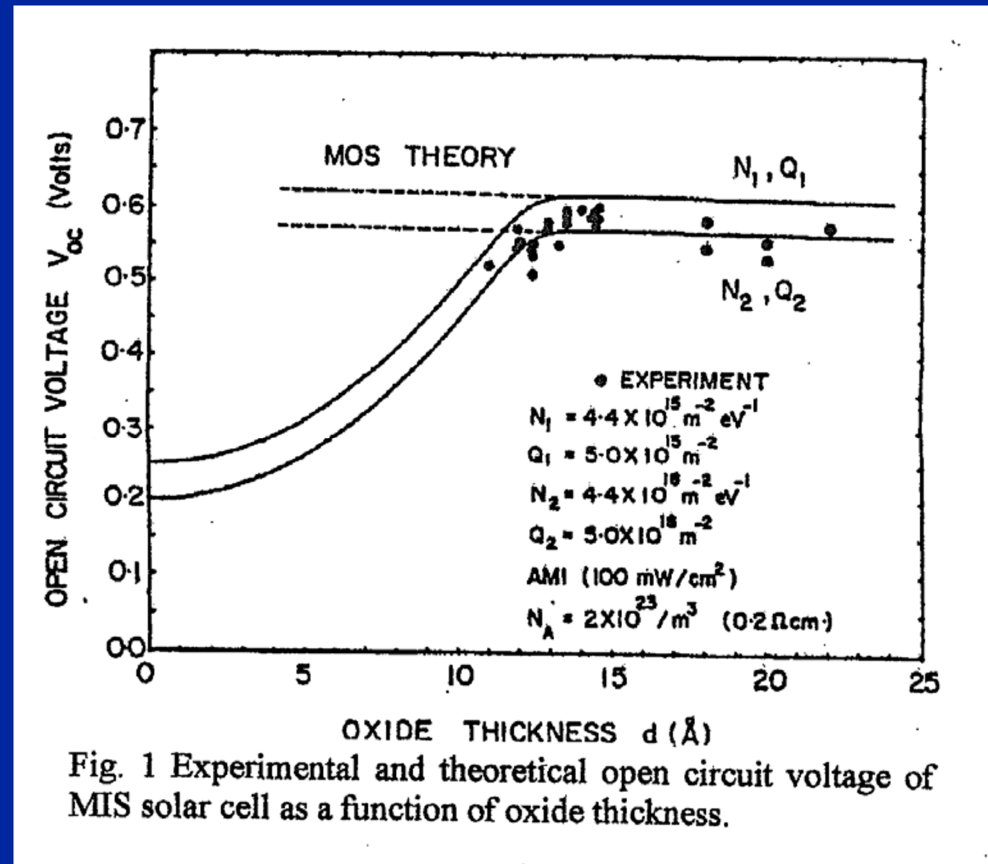
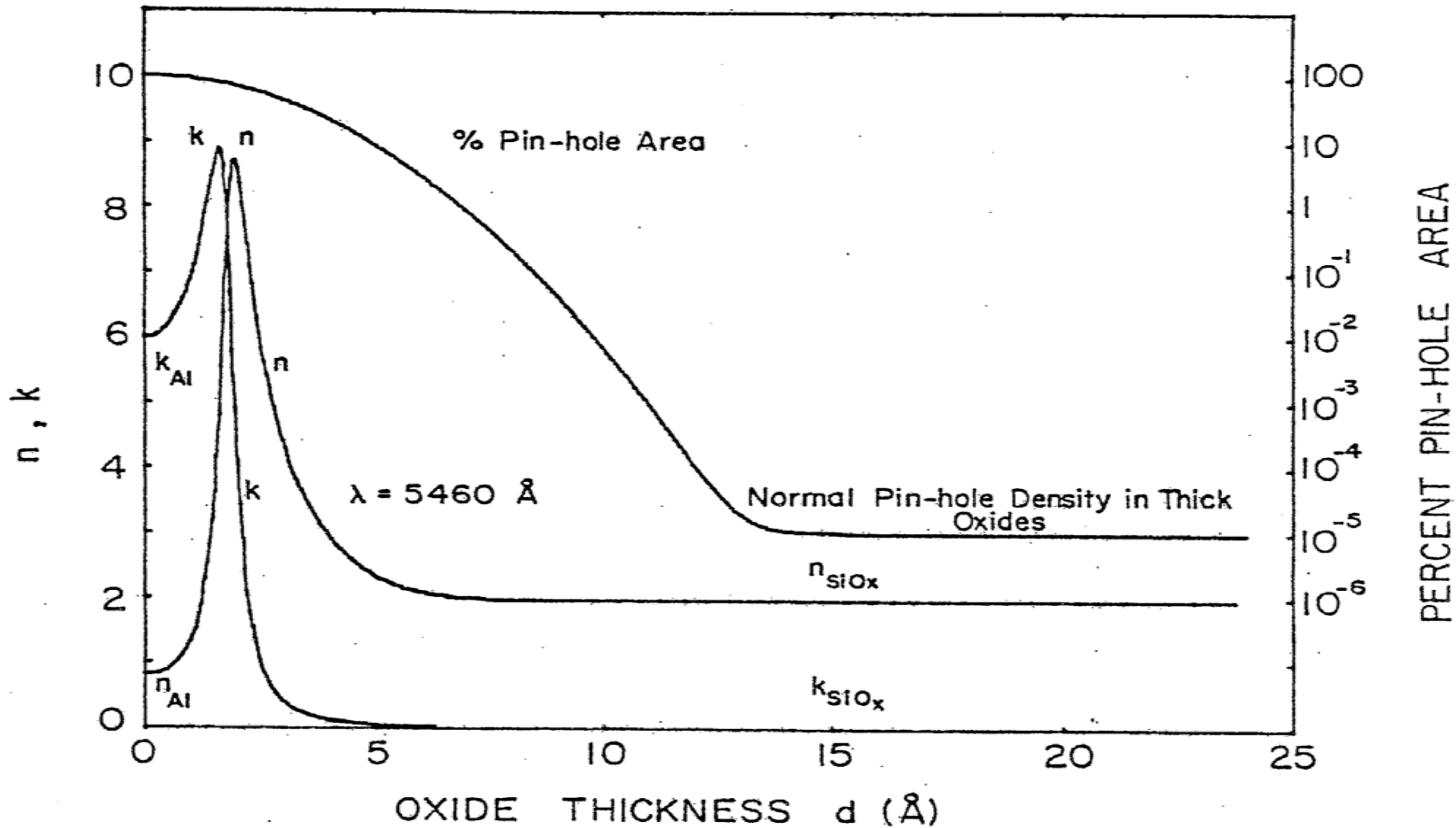
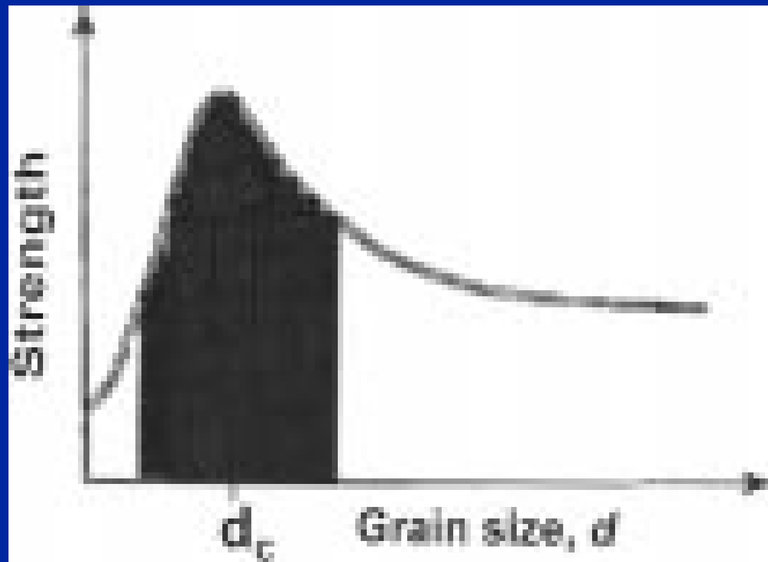


Fig. 1 Experimental and theoretical open circuit voltage of MIS solar cell as a function of oxide thickness.

R. Singh Proc. IBM Conf. on SiO2, 1978



Variation of the Strength of a Metal



- Variation of the strength a metal with grain size as the variable. Optimum value ~3-5 nm grain size
- Ref. : A. Lodha & R. Singh, IEEE Trans. Semi. Mfg., 14,281, 2001

Semiconductor Fabtech, 20th Edition, p. 104, 2006

IG

Dominance of silicon CMOS based semiconductor manufacturing beyond international technology roadmap and for many more decades to come

R. Singh, **P. Chandran**, **M. Grujicic**, **K.F.Poole**, **U. Vingnani**, **S.R. Ganapathi**, **A. Swaminathan**, **P. Jagannathan**, & **H. Iyer**, Clemson University, South Carolina, USA

Thermal Conductivity of Silicon

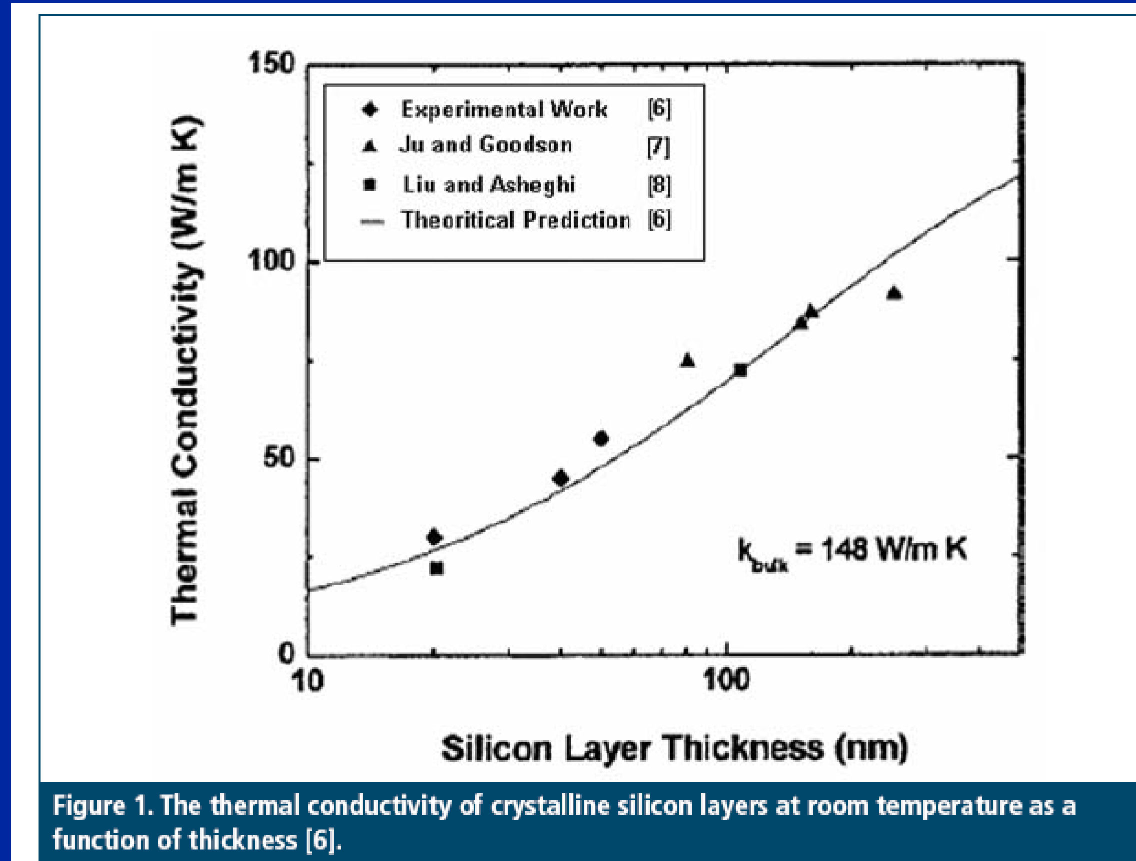


Figure 1. The thermal conductivity of crystalline silicon layers at room temperature as a function of thickness [6].

Thermal Conductivity of Nanowires

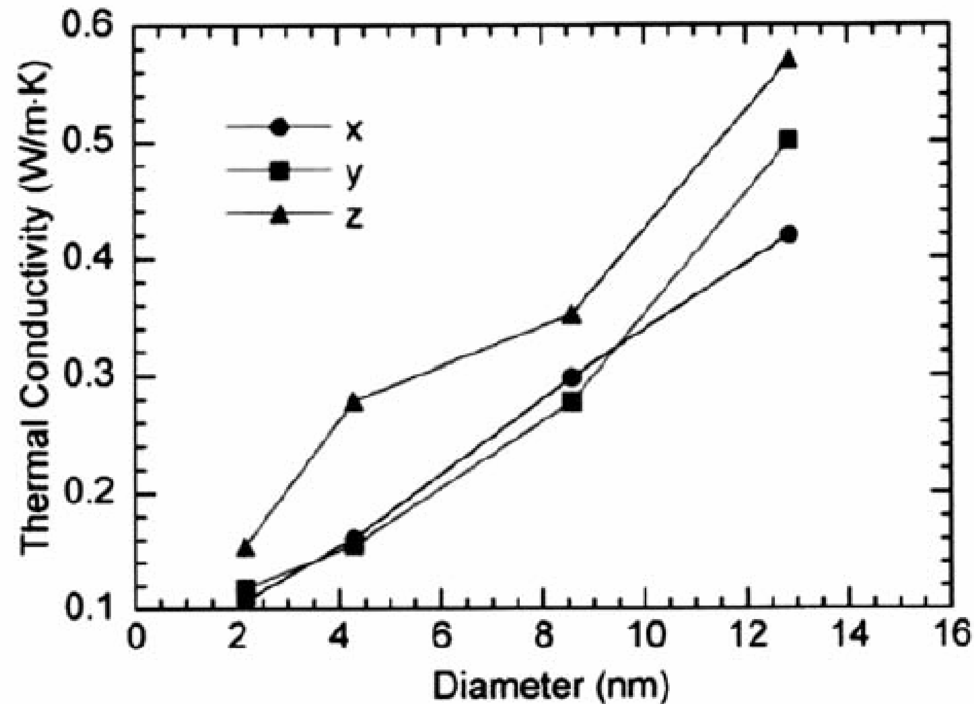


Figure 2. Thermal conductivities of nanowires in radial (x and y) and axial z directions [7].

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Thermal Conductivities and Heat Sink

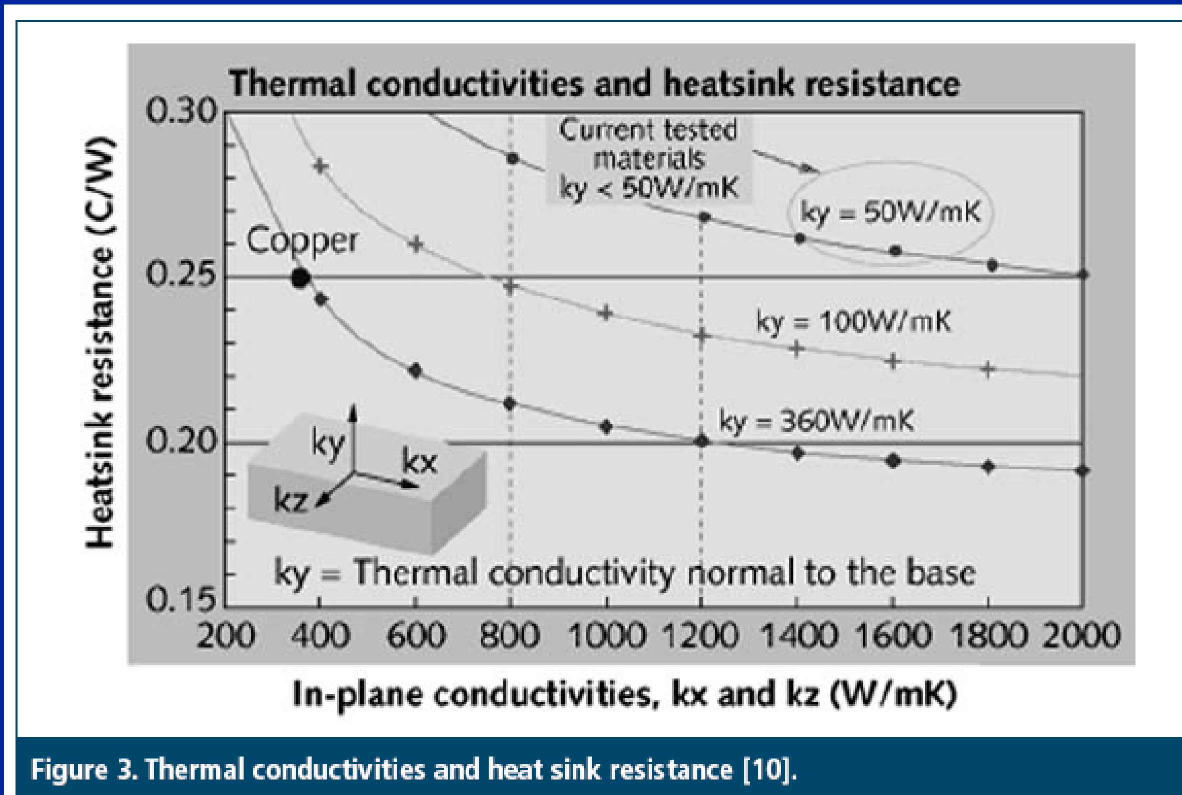
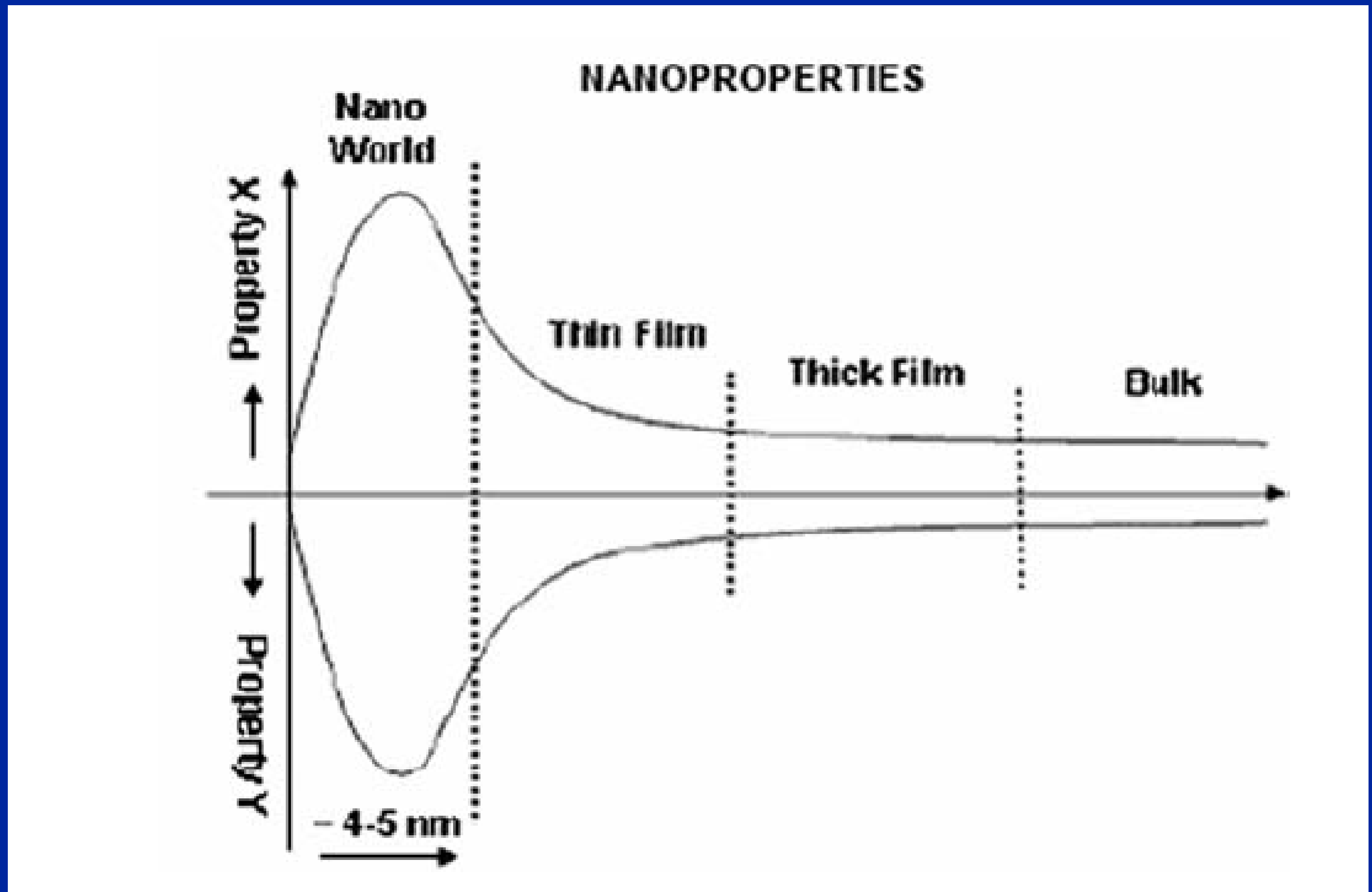


Figure 3. Thermal conductivities and heat sink resistance [10].

Properties of Nano-films



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Our Manufacturing Mantra

- MICROSTRUCTURE HOMOGENITY: Best Values of Performance, Reliability & Yield
- Minimize magnitude and variations of local and global thermal and residual stresses of each layer of material
- Use point sources for fluid and energy delivery in every tool
- R. Singh, V. Parihar, K. F. Poole and K. Rajkanan, "Semiconductor Manufacturing in the 21st Century", Semiconductor Fabtech, 9th Edition, pp. 223-232, 1999
- R. Singh & K. F. Poole, US Patent No.: US 6,569,249 B1, Date of Issue: May 27, 2003

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RIDAY, OCTOBER 15, 2004

THE WAL

TECHNOL

ntel Gives Up on Speed Milestone

Maker Won't Offer
ium 4 at 4 Gigahertz,
ses on Cache Memory

By Don Clark

l Corp. is scrapping plans to hit a ofile performance milestone for ship microprocessor, the latest in s of course changes and miscues big chip maker.

nologies to its product line, including putting the equivalent of multiple processors on a single chip, Mr. Mulloy said.

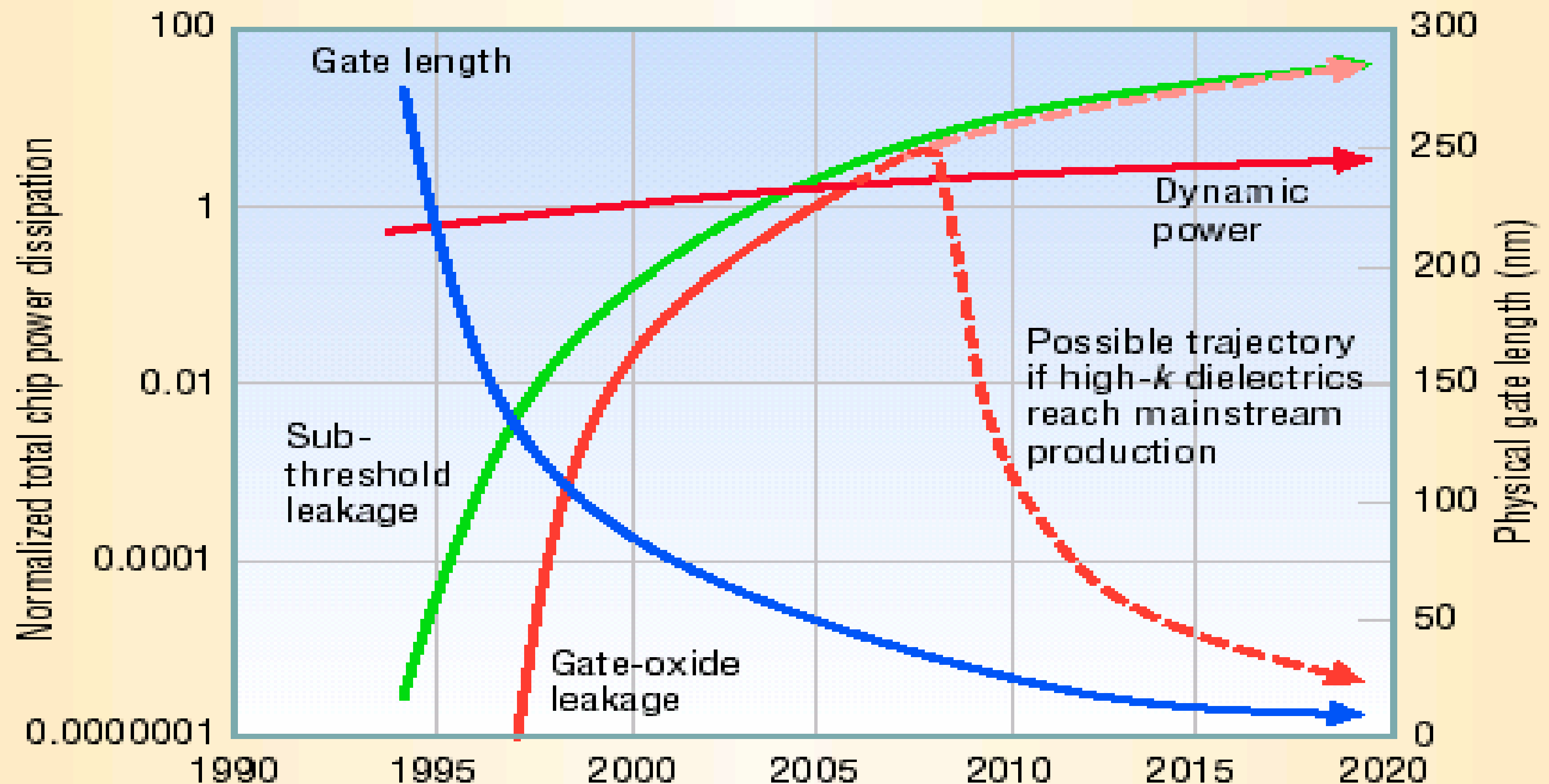
The chips affected by the schedule change are known by the code name Prescott, and are Intel's first products for desktop PCs to be manufactured using a process that creates circuits with dimensions of 90 nanometers—or billionths of a meter—down from 130 nanometers for earlier chips. Such changes in manufacturing generations have allowed companies to lower production cost and power consumption, while boosting a chip's

ucts, which put the equivalent of t more processors on a single chip.

The increased urgency is part cause Intel's Prescott design cons more power than prior models, d the move to 90-nanometer techn The Pentium 4 operating at 3.6 giga draws up to 115 watts, compared w watts for models operating at 3.2 hertz and below.

Rick Whittington, an analyst at & Co., said Intel needs to move quic counter competition from Advance cro Devices Inc., whose Athlon 64

Impact of high-K gate dielectrics on power dissipation



Wall Street, January 27, 2007

Intel Alters Computer-Chip Recipe

Change in Materials Seeks Increased Speed And Power Efficiency

By DON CLARK

Intel Corp. is on the verge of a significant change in the way it makes computer chips, an advance in manufacturing technology that competitors are vowing to match.

The Silicon Valley company was to announce Saturday that it will replace materials it has used for decades in its next production process, which is scheduled to begin churning out chips during the second half of this year. Intel claims the change will bring big gains in chip speed while controlling power consumption, continuing a pace of progress that has helped boost the capabilities of personal computers and other products.

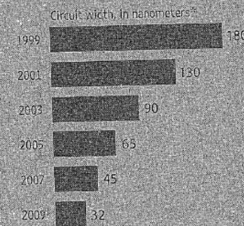
But rivals aren't conceding that Intel has an advantage. **International Business Machines** Corp., for example, on Saturday was to announce a similar shift in manufacturing technology by early 2008. **Texas Instruments** Inc. says it expects to make the change at roughly the same time.

Since the 1960s, companies have raced to shrink the size of transistors, the elements on chips that switch on and off or store data to carry out basic electronic functions. Making transistors smaller simultaneously increases their speed and data-storage capacity while lowering manufacturing cost.

The most advanced chips in production now have transistors and other circuitry with dimensions of 65 nanometers, or billionths of a meter. Getting to the next technology generation—which will shrink circuit dimensions to 45 nanometers—presents new obstacles. At those microscopic sizes, electrical current can begin to leak uncontrollably from transistors, causing problems such as rapidly draining the batteries of laptop computers.

Companies have long discussed the need to adopt new materials to head off the problem. But exactly when they would make the difficult transition wasn't clear.

Intel, whose revenue makes it the world's biggest chip maker, is now disclosing that it will use two new materials for making transistors when its factories begin gearing up production of 45-nanometer chips this year. They will replace silicon dioxide and polycrystalline silicon—materials derived from the widely found element silicon that is the basic ingredient in most chips.



The company is identifying one of the new materials as hafnium, a silvery element sometimes used in the control rods in nuclear reactors. Intel said it is also adding two metals in making transistors, but isn't disclosing what they are for competitive reasons.

Mark Bohr, who holds the title senior Intel fellow and helps lead manufacturing-technology development, said the new production process can squeeze twice the number of transistors into the same space. That would allow chip designers to either make their products smaller—sharply reducing manufacturing cost—or boost the number of transistors per chip.

Designers can use the manufacturing technology to make transistors operate more than 20% faster, or to sharply reduce one form of electrical current leakage, he said. The production process also causes a tenfold reduction in current leakage from another part of a transistor, he added.

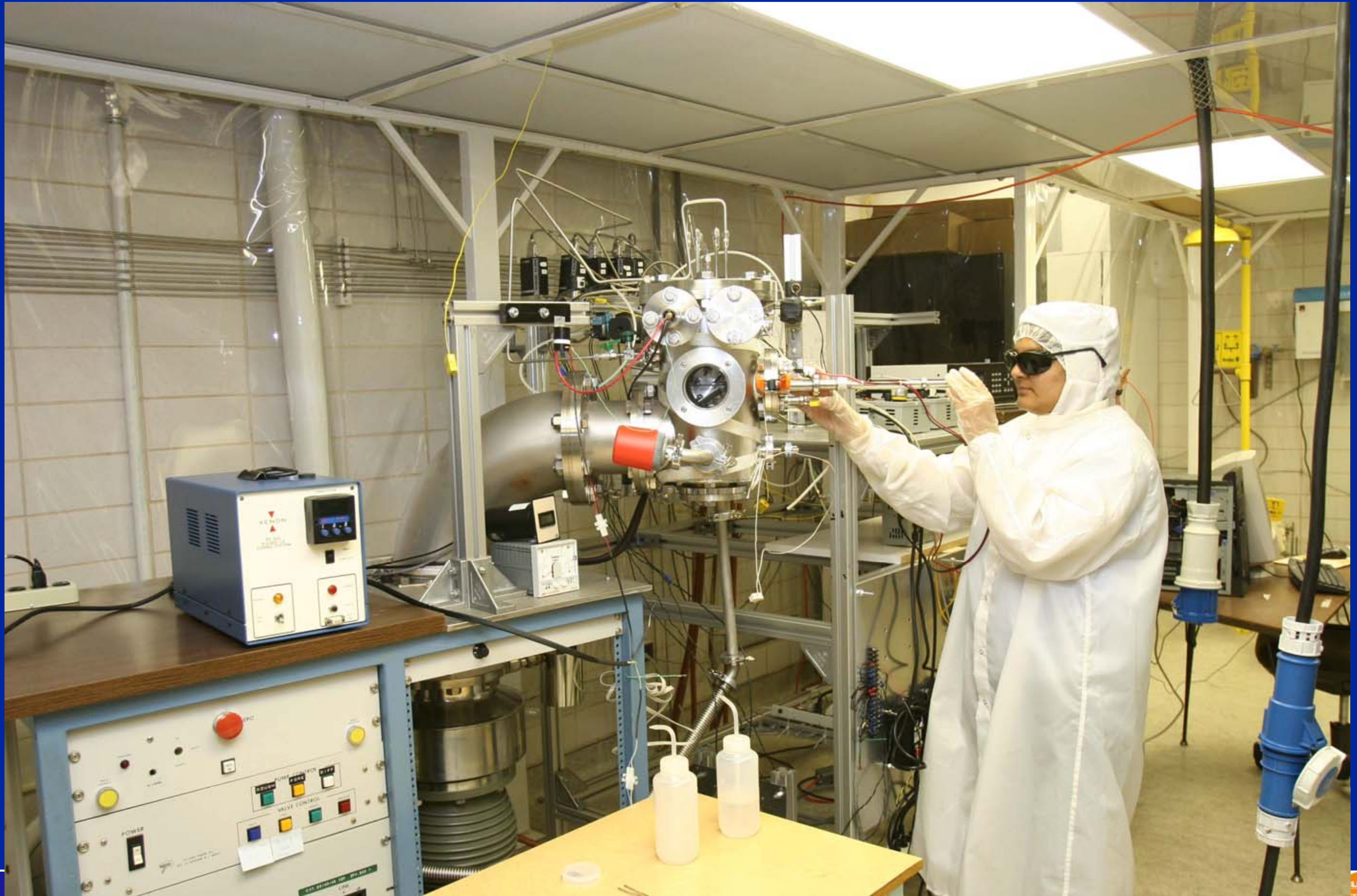
Intel already has used the technology to make working prototypes of microprocessors that it might begin shipping by the end of the year. "When word of that spread through the company, you could just feel the excitement level," Mr. Bohr said.

IBM is announcing plans to introduce similar materials to its 45-nanometer production process, which is being developed jointly with engineers from **Sony** Corp., **Toshiba** Corp. and **Advanced Micro Devices** Inc. IBM expects chips based on the new materials to begin appearing in its computer systems during the first half of 2008.

"We are coming out with something that is hugely aggressive," said Bernie Meyerson, IBM's chief technologist.

The IBM announcement could be important in the long-running competition between Intel and AMD, which fell more than a year behind Intel in starting 65-nanometer production. AMD has vowed to close that gap, and the fact it can use the jointly developed technology could help its plans to introduce products using 45-nanometer technology by mid-2008.

Texas Instruments, meanwhile, already has chosen a hafnium-based material to add to its 45-nanometer process, said a company spokesman. It is also committed to adding the metal technology for transistor gates, but hasn't settled on the material, he said. TI plans to offer sample chips on the 45-nanometer process by the end of 2007, he said, with volume production expected in mid-2008.



Center For Silicon Nanoelectronics

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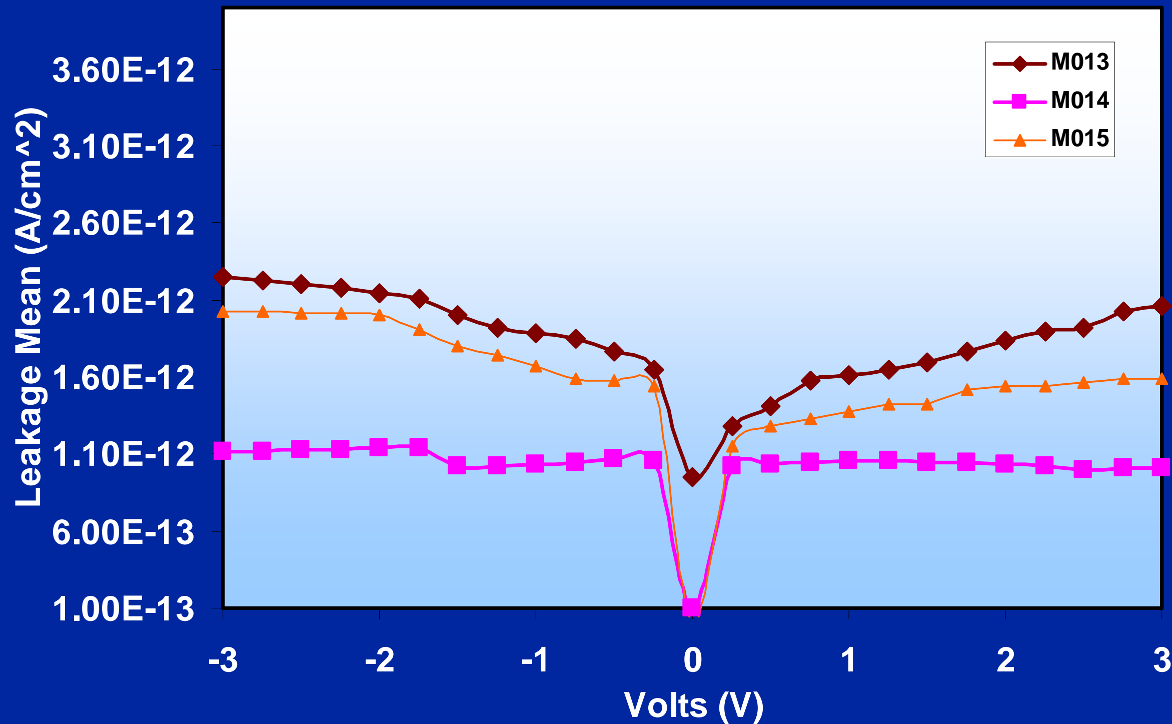
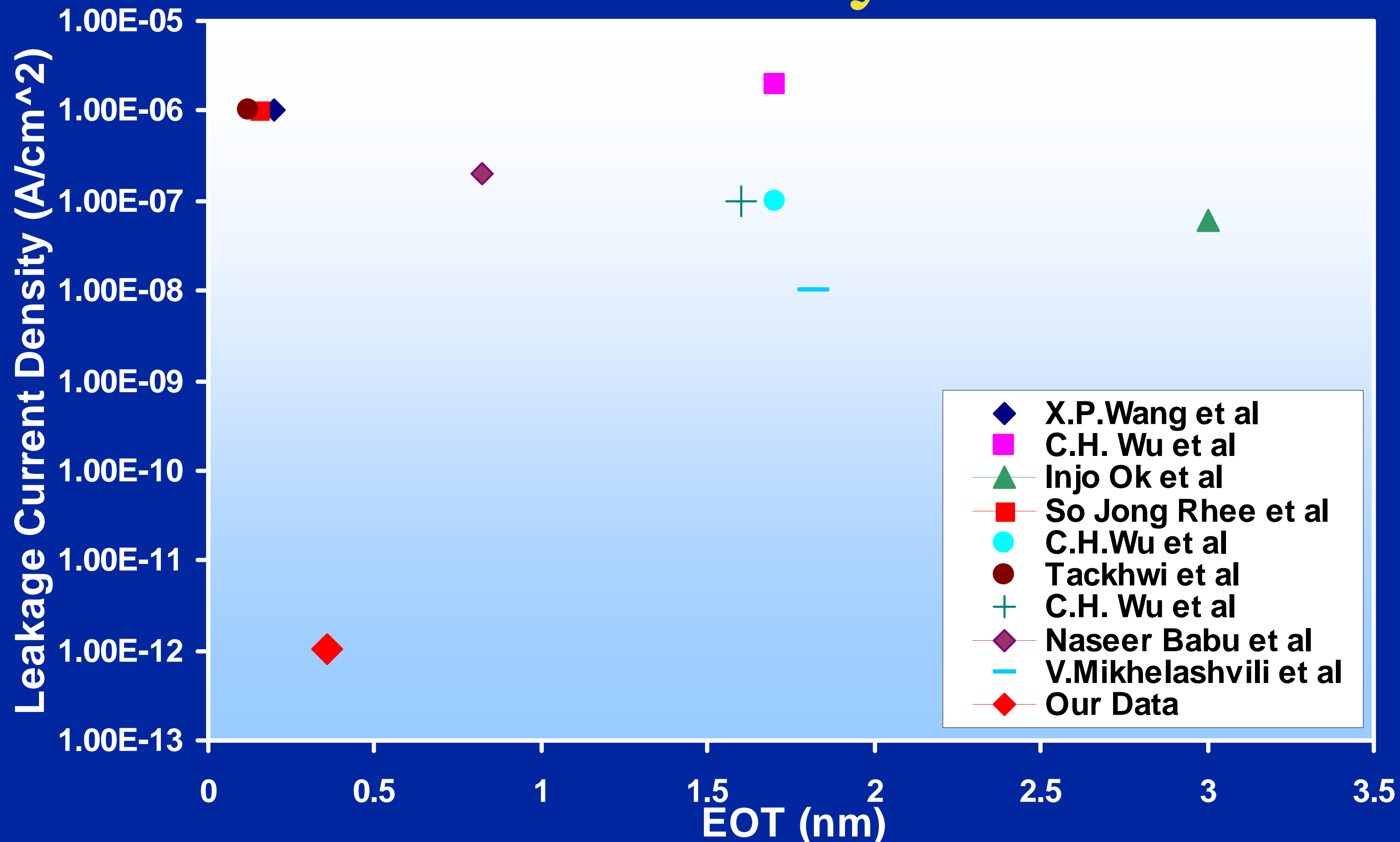
Leakage Current Density of 2.1 nm High-K Dielectric



Comparison of Leakage Current Density



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Process Variation Analysis

- Based on the optimized parameters for In-Situ Clean, Deposition and in-situ annealing we have conducted repeatability tests.
- 99% prediction interval for the leakage current density of a single future wafer is

(0.9746E-12 A/cm^2, 1.1104E-12 cm^2).

- The implication of these results is that for all the next generation of CMOS the leakage gate current is zero
- This will reduce the heat problem and higher speed ICs will be fabricated

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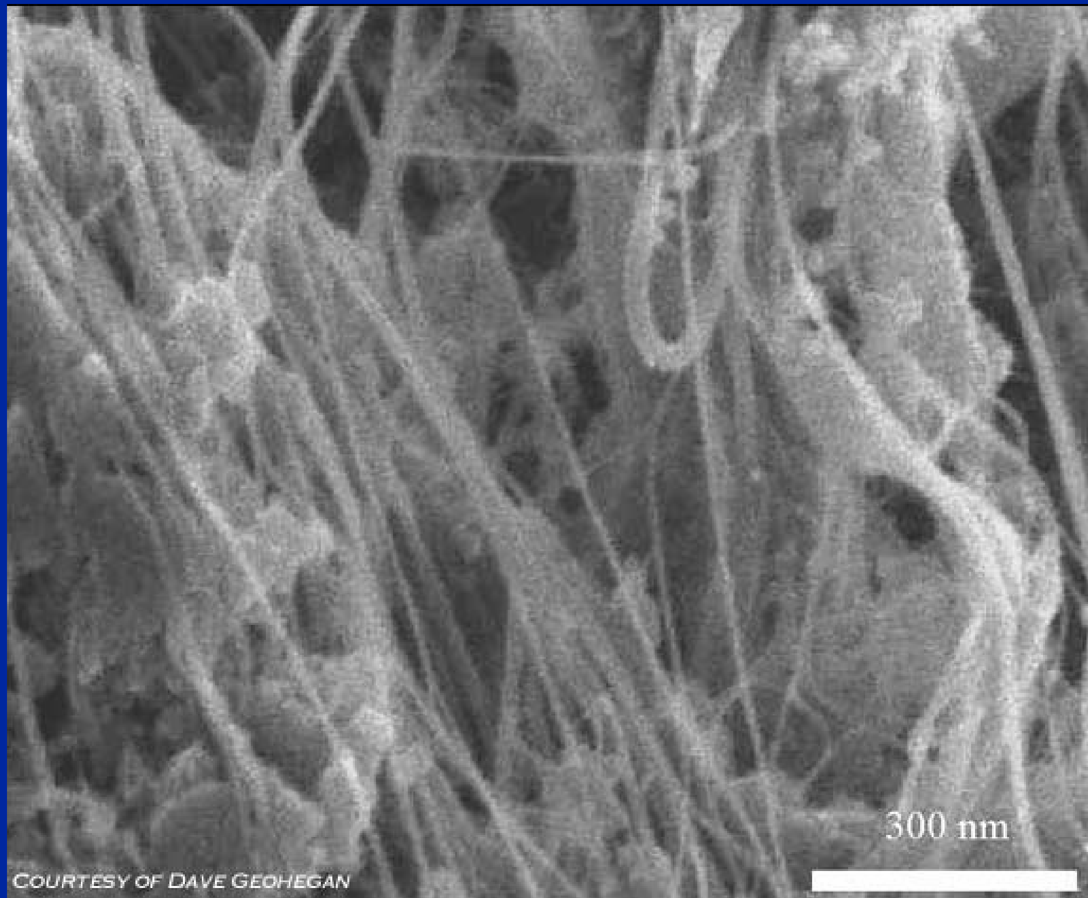
CNT - Fabrication

SWCNT - Single Wall Carbon NanoTube



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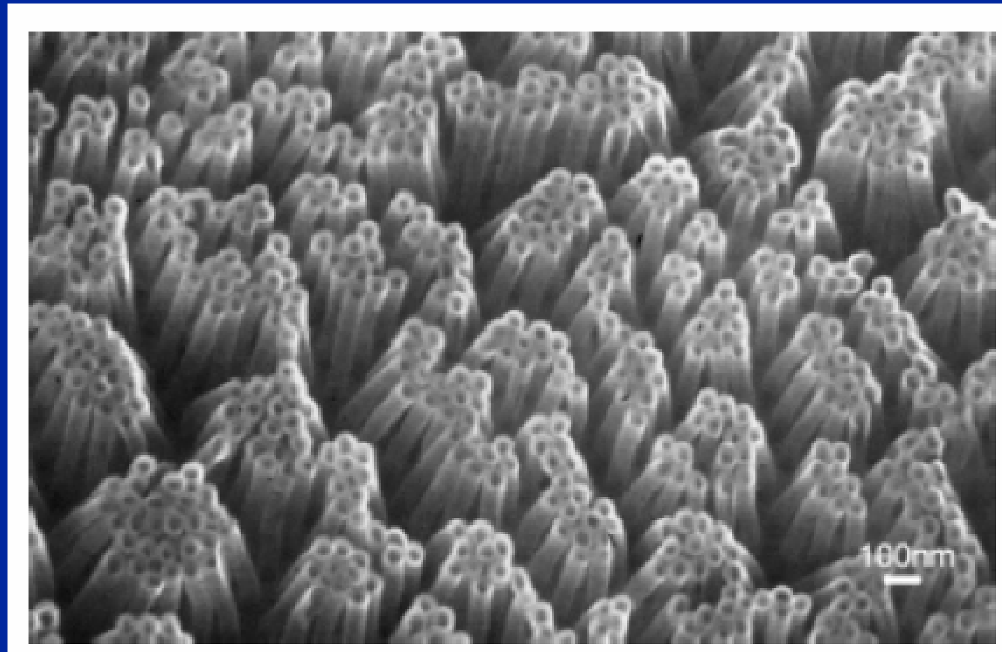
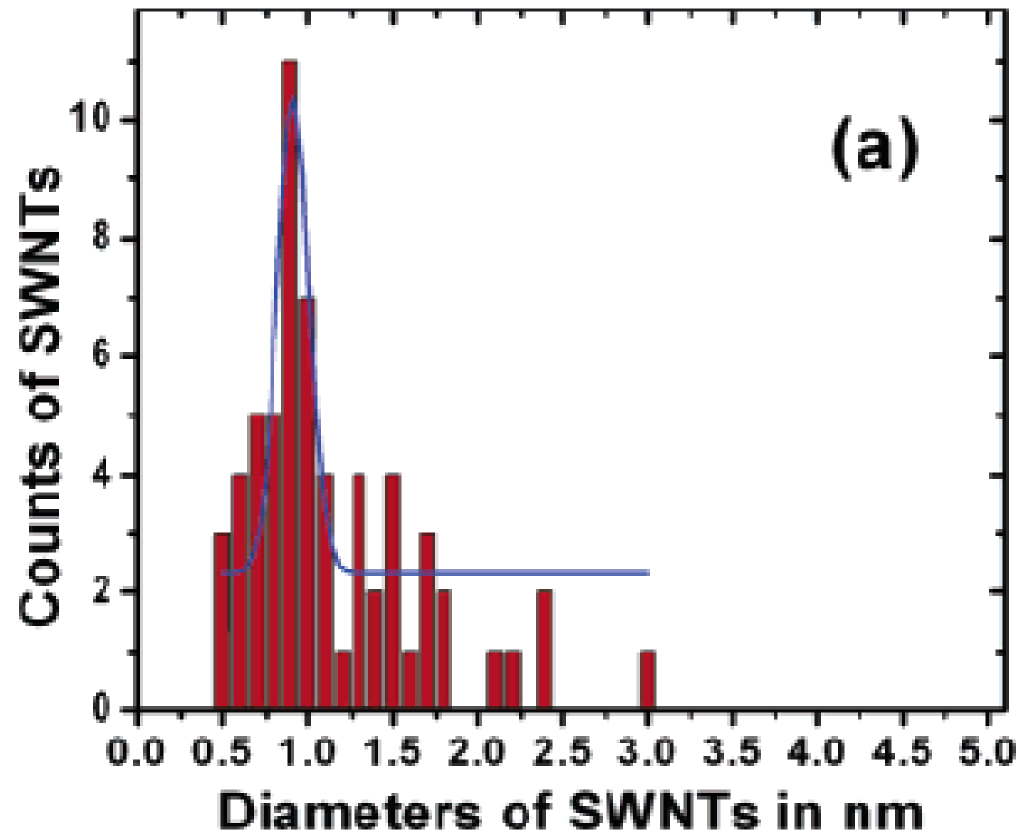
SEM image showing long, exposed stuck nanotubes clumped together from a sample

(Source: IEEE Proceedings, page 1823, 2003)

WE EXPECT ALL KINDS OF PROBLEMS DUE TO LACK OF MICROSTRUCTURE HOMOGENITY



Diameter Distribution of CNT



Best Values of CNT Control of diameter

- The distribution of diameter ~1.3 to 1.6 nm
- Ref: G. Zhang et al. Science, vol. 314, p. 974 (2006)

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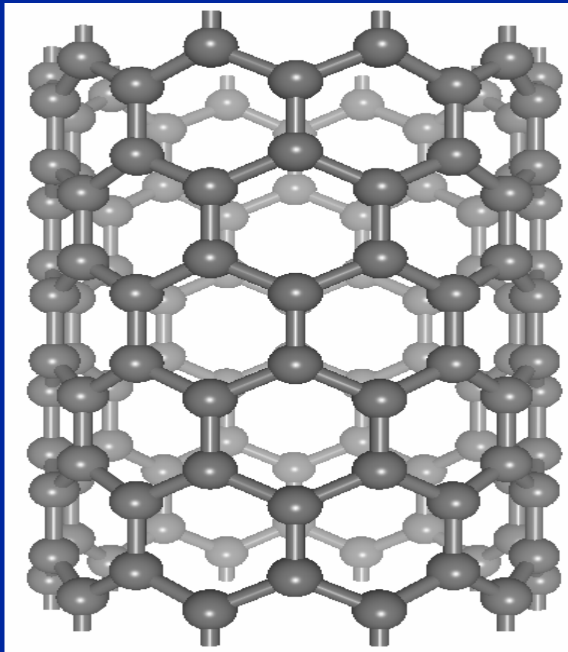
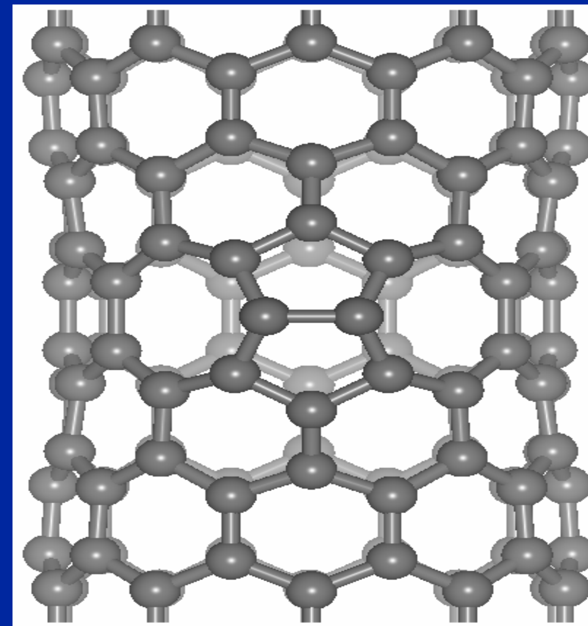
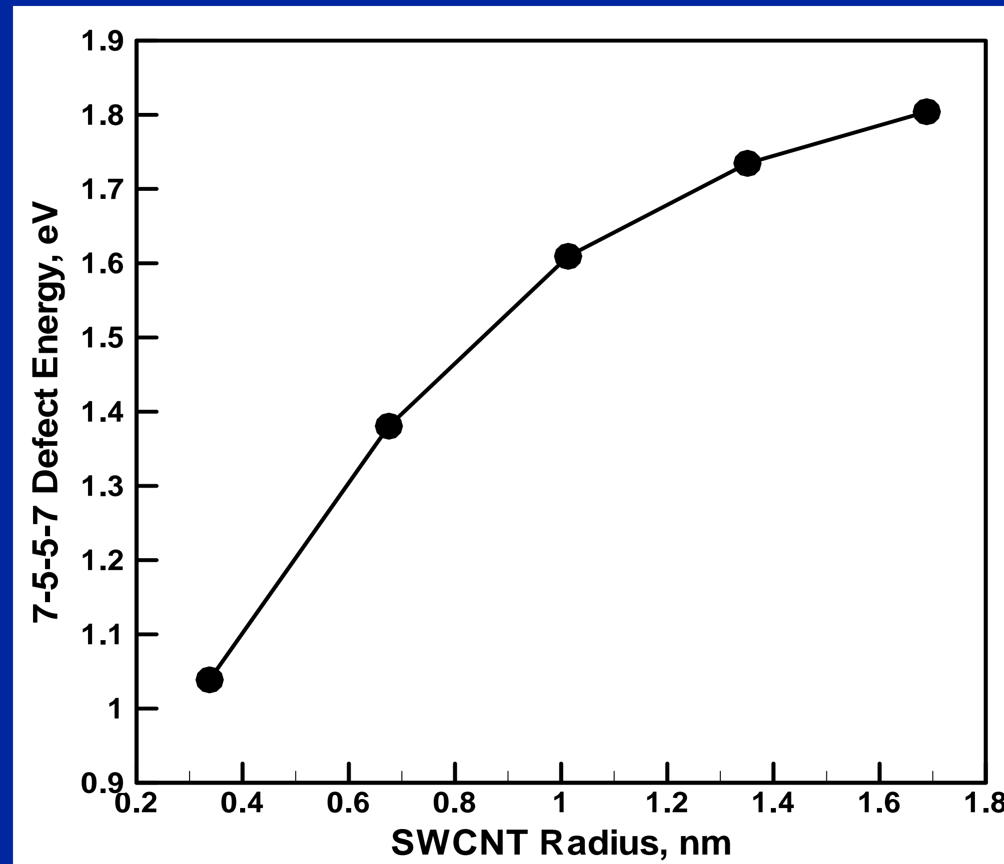
Side views of the fully-relaxed structures of: (a) a perfect semiconducting zig-zag (10,0) SWCNT; (b) the same nanotube containing a single 7-5-5-7 defect.


(a)


(b)

Defect activation energy of SWCNT



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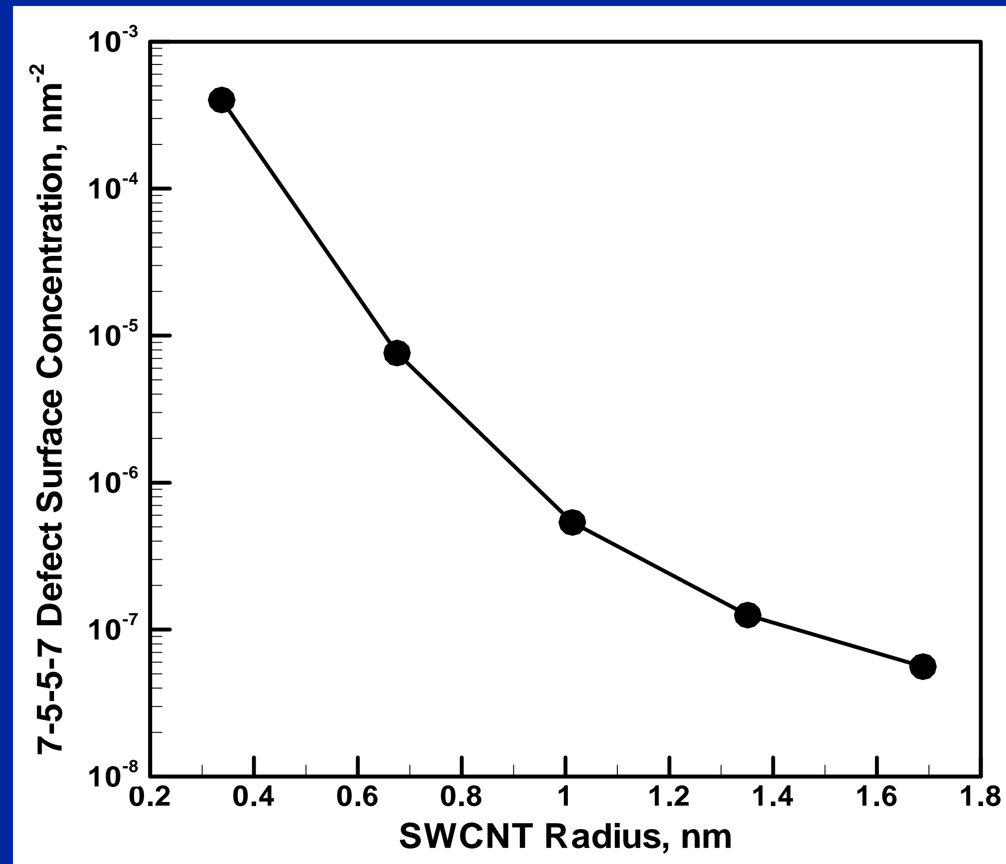
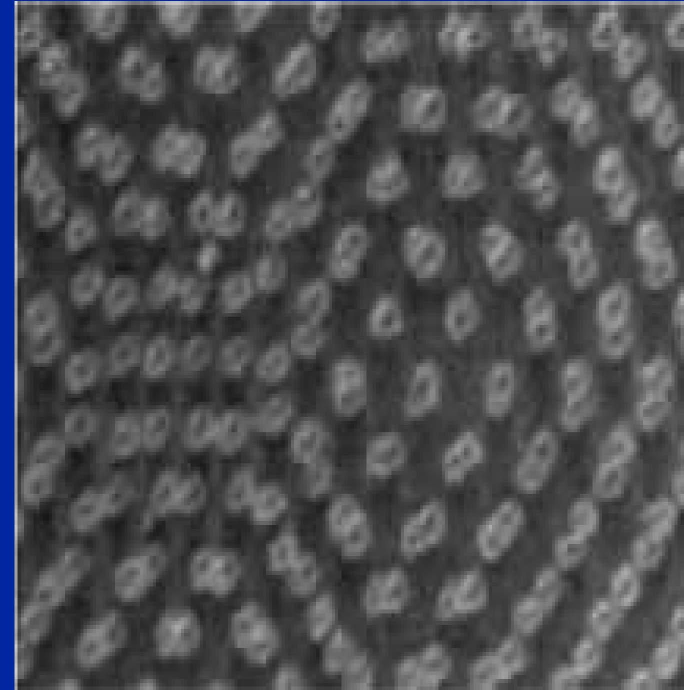
Defect Surface Concentration of SWCNT



IBM Millipede

200,000,000,000 bits/inch^2



10 nm

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Bottom Line Challenge in Bottom Up Approach of the Nano World

- Biological Systems work well in the presence of defects
- Throughput is low
- DNA replication produces one error per billon nucleotides
- Silicon ICs are operating with failure in time (FIT) of the order of one part in billon
- Open Q : Why to use a low throughput and same defect density technique

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DISRUPTIVE TECHNOLOGIES IN THE NANO WORLD

How disruptive are they ?

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Fundamentals of Disruptive Nanoelectronics

JOURNAL OF NANOSCIENCE AND NANOTECHNOLOGY

Fundamental Device Design Considerations in the Development of Disruptive Nanoelectronics

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In the last quarter of a century silicon-based integrated circuits (ICs) have played a major role in the growth of the economy throughout the world. A number of new technologies, such as quantum computing, molecular computing, DNA molecules for computing, etc., are currently being explored to create a product to replace semiconductor transistor technology. We have examined all of the currently explored options and found that none of these options are suitable as silicon IC's replacements. In this paper we provide fundamental device criteria that must be satisfied for the successful operation of a manufacturable, not yet invented, device. The two fundamental limits are the removal of heat and reliability. The switching speed of any practical man-made computing device will be in the range of 10^{-15} to 10^{-3} s. Heisenberg's uncertainty principle and the computer architecture set the heat generation limit. The thermal conductivity of the materials used in the fabrication of a nanodimensional device sets the heat removal limit. In current electronic products, redundancy plays a significant part in improving the reliability of parts with macroscopic defects. In the future, microscopic and even nanoscopic defects will play a critical role in the reliability of disruptive nano-electronics. The lattice vibrations will set the intrinsic reliability of future computing systems. The two critical limits discussed in this paper provide criteria for the selection of materials used in the

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Examination of Disruptive Technologies

- Reversible computers & Nano Motors Based on Random Motion
- Quantum Computers
- Spintronics
- Molecular Computers
- Optical Computers
- Carbon Nano-tubes Based Computers
- DNA Computers

HEAT DISSIPATION

- Slow speed computers pose no fundamental limit
- Human brain with neural density ~ 10^6 per cm^2, speed ~10^{-3} s handles a power density of 250 nW/cm^2
- The design of faster and denser computers is dictated by power handling capability
- Commentary: Thermal Solutions Rut Threatens Electronics innovation (1-2-07) http://www.edn.com/article/CA6402944.html?partner=eb

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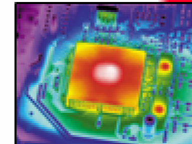
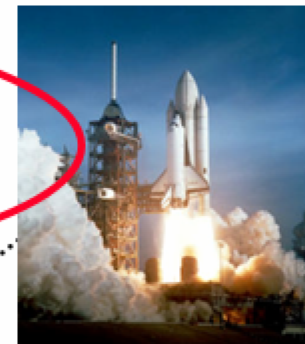
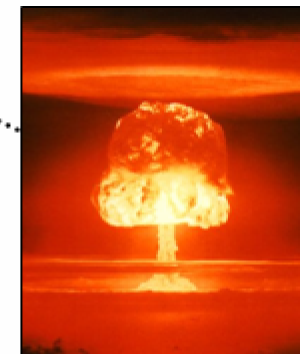
Putting the Heat Flux Challenge into Perspective

Honeywell

Shuttle Re-entry


Tomorrow's Microprocessors


Rocket Nozzle Throat


1 Megaton at 1 mile

Sunlight on a Tropical Beach

Heat Flux (W/cm^2): 0.01, 0.1, 1, 10, 100, 1000, 10000

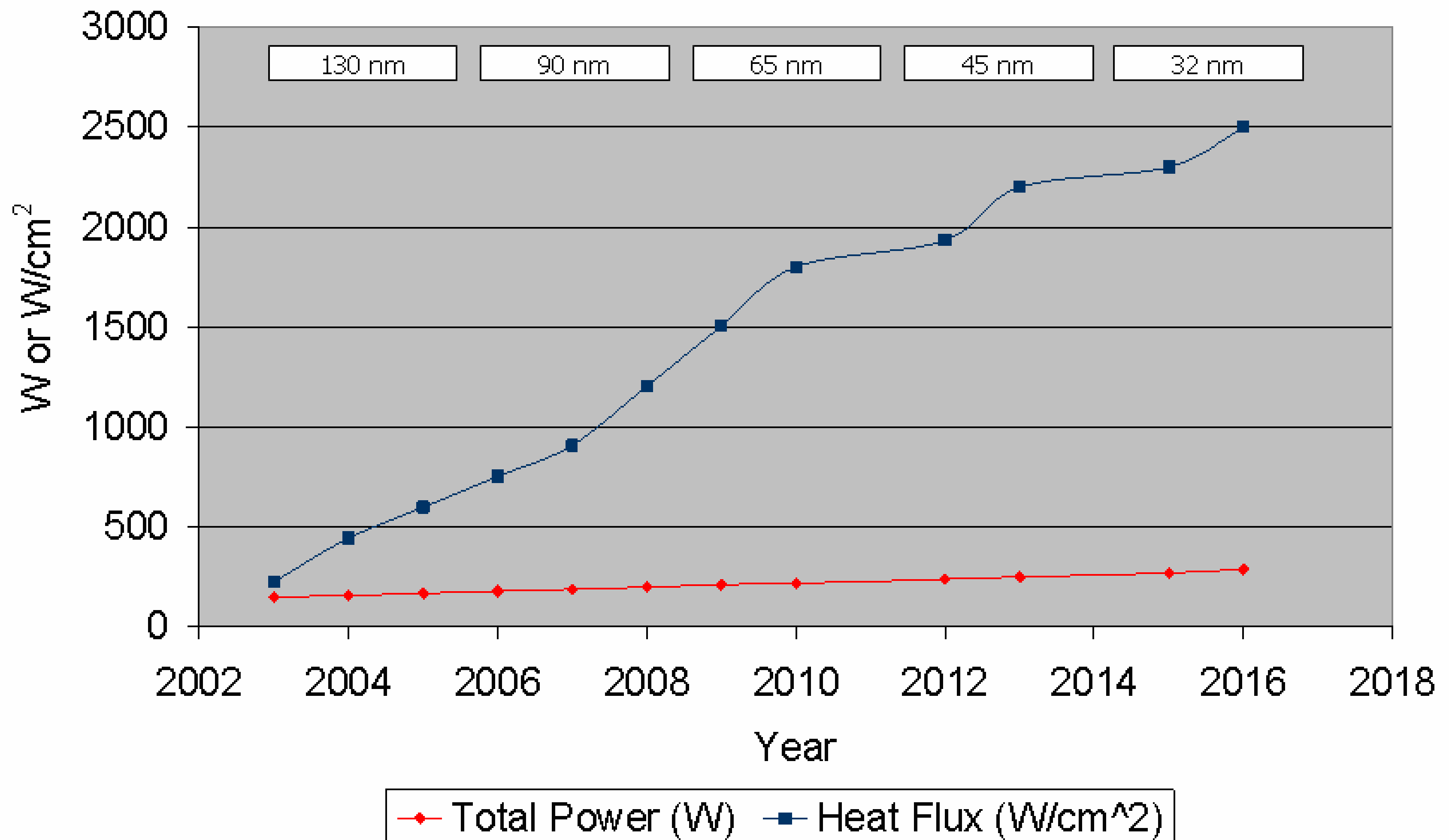
Temperature (°C): 0, 500, 1000, 1500, 2000, 2500, 3000

The thermal challenge in an IC is a truly daunting problem

CPU Power is Steadily Increasing

Honeywell

ITRS Power Predictions



Flux at the core continues to rise despite design innovation

CPU Heat Flux is High

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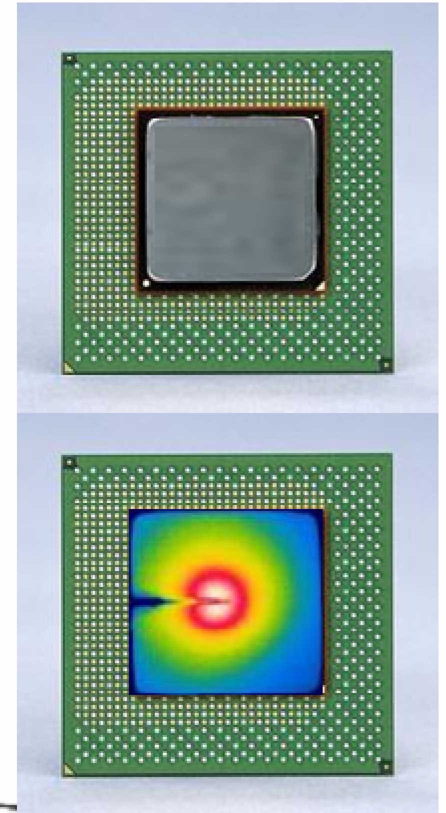
IR image of an actual processor



Most heat leaves through center 15% of the spreader's surface area

Reversible Computation

- The literature on the topic of reversible computers and nanotechnology has a fundamental flaw due to work of Bennett of IBM cited example of biological systems.
- The fault in Bennett's work is the fact that biological systems capable of processing context-related events have to be open, nonlinear and operate at non-equilibrium or preferably far from equilibrium conditions at slow speeds of the order of milli seconds. All of these requirements are not met in non-biological closed systems and reversible computation with no energy loss is fundamentally impossible.
- Silicon IC designers know that at best the concept of reversible logic or adiabatic switching applied to integrated circuits saves power at the expense of speed. This is already in practice in a number of applications.

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Random Motion based Motors

- Similar to reversible computers, there are many claims that one can operate a nano-motor based on the exploitation of random motion, with no use of external source of energy.
- The molecular motors on which life depends are open systems and are driven by Brownian motion
- For closed systems with no external source of energy, one can never exploit "random motion" into useful work. Only by supplying external energy source, the nano-machines can operate in an open system mode.
- The question of interfacing these man-made non-biological motors at nano-scale with the micro-scale and macro scale world is a practical engineering problem and does not pose any fundamental issue.

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Quantum Computers

- QUANTUM COMPUTERS: Since error correction is part of quantum computing, more heat will be generated in a quantum computer than a Von-Neumann architecture based computer operating at the same speed.
- Assuming that researchers can lengthen the decoherence interval to 10 microseconds; quantum computer chips will still consume more than 100 megawatts.
- The facts presented here indicate that quantum computers if ever realized will involve massive size and extra ordinary cooling techniques (e.g. cooling of a nuclear reactor) needs to be implemented.

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Molecular Computers

- MOLECULAR COMPUTERS: The literature is full of conceptual errors about the potential of molecular computing systems. First of all a two terminal logical molecular device will never find any practical applications in realizing a practical system.
- The second claim by the advocates of molecular computers is that components as large 10^{24} can be accommodated in the design of molecular nanoelectronics. The power density values for such a molecular computer (molecular device area of the order of $0.025 nm^2$) operating at switching speed of 1 ps will be of the order of 10^{29} W/cm^2.
- Thus due to heat dissipation problem, it is fundamentally impossible to envision general purpose molecular computers.

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CNT Based Computers

- Band gap too small (noise problem)
- Thermal Conductivity along the tube axis is more than 30 W/cm x ^{0}C and in a direction normal to tube is only 0.056 W/cm x ^{0}C.
- Hotspots are created both in devices as well as in interconnects at nano dimensions [J. Kloeppel, *Science Daily*, Jan 2006].
- Anisotropy and local heating will severely affect the reliability of CNT based computers.
- Also, problems due to electrical inter coupling may arise in case of CNTs.
- In a recent work [Z. Chen, et al. , *Science*, vol 311 ,March 2006], an unwarranted claim of higher performance is made without the inclusion of any parasitic and the reported switching time is of few naano second.

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Requirements of new technology

PROCESS	
Substrate size	450 mm diameter
Feature size	< 45 nm
Thermal conductivity	>Silicon
Integration density	$>10^{10}$ elements/cm^{2}
PERFORMANCE	
Operating Temperature	Room temperature
Power consumption	$<10^{-3}$ fJ/switch
Gain	>10
Speed	<100fS
Reliability	<0.1FIT

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Ultimate Computer ?

- Nano-diamond based C-MIS FET deposited on Silicon Substrate
- Nano-diamond is the only material that can meet all other fundamental requirements and provide complimentary FET(μ_n= 2200 cm^2/V-s and μ_p= 1600 cm^2/V-s) in line with the legacy of silicon CMOS
- Best for high temperature, high performance, high frequency, and high power Nanoelectronics

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OPPORTUNITIES & CHALLENGES OFFERED BY THE NANO WORLD IN THE AREA OF ENERGY CONVERSION

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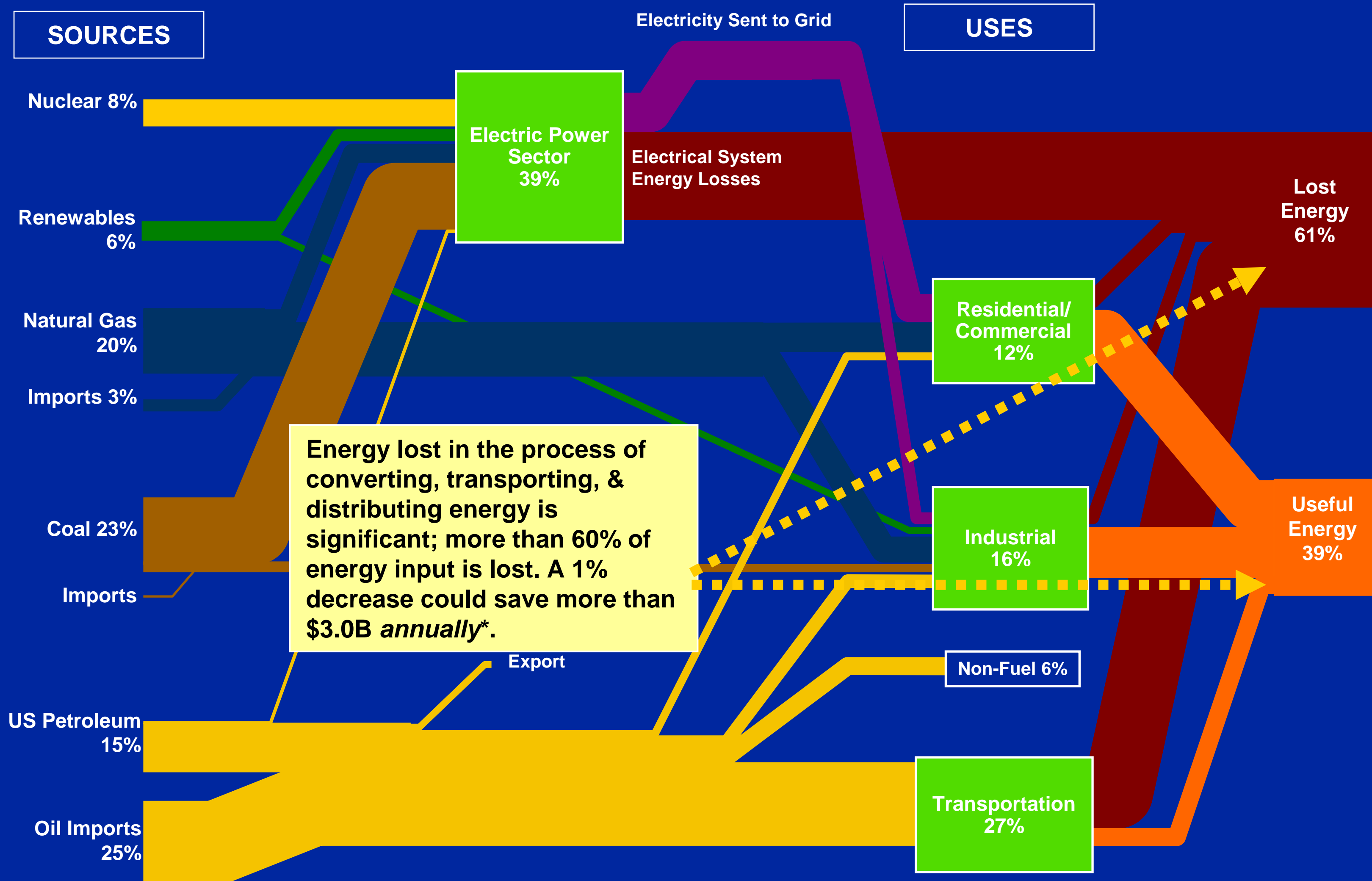
Energy Losses are Tremendous



* NCI estimate using $50/bbl oil & $3/mmbtu blended cost for gas/coal
Source: Lawrence Livermore Natl Labs; EIA
2002 Data: Net Resource Consumption ~ 97 Quads
Sources less than 1% not included

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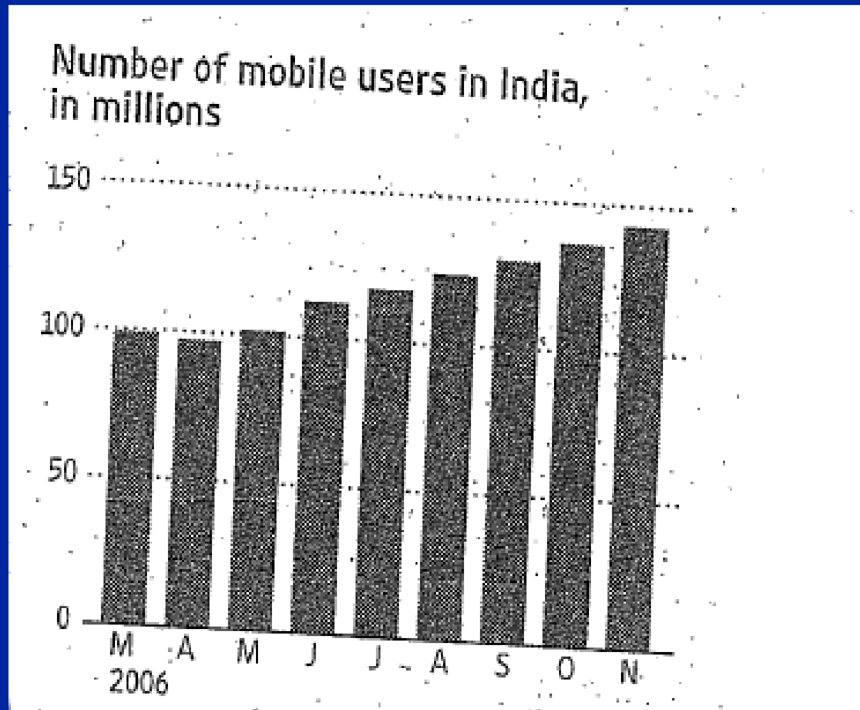
Growth of Cell Phones in India



By the end of year 2008, one third of the population (billon plus) will have cell phones

Key Issues in Energy Conversion

- Local generation of power can provide a solution similar to the growth of Cell phones
- Electrical power provide an ideal solution for a number of applications
- The Environmental issues can not be ignored
- During the life time of a particular device the energy converted must be much more than the energy consumed in the manufacturing of a particular device. This will dictate the economics of a particular process or method
- Materials used in any device or method should not increase the prices of raw materials used in the manufacturing (R. Singh & J. D. Leslie, Solar Energy, 1980). Based on this concept we stressed silicon as an ideal photovoltaic material.

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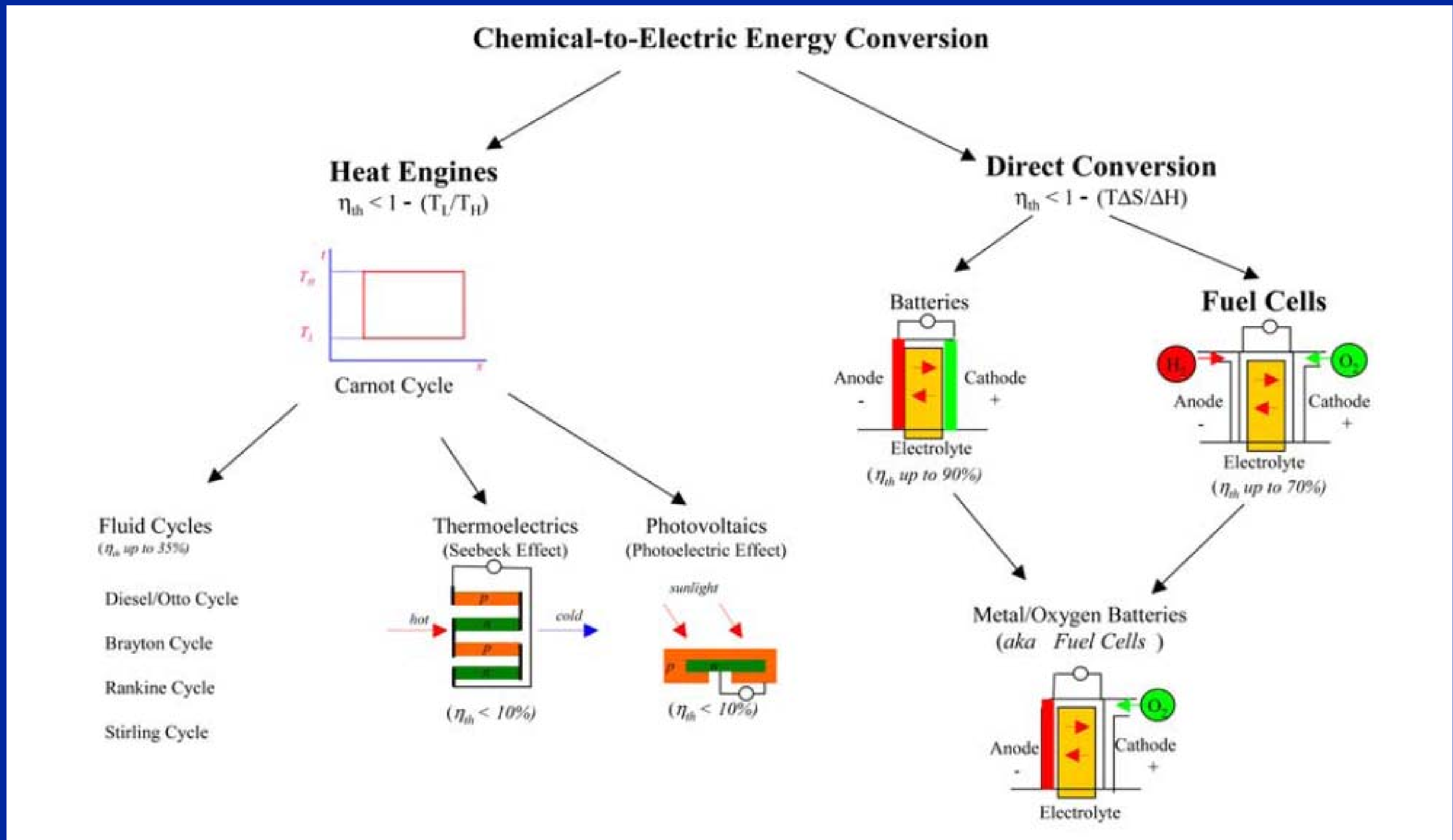
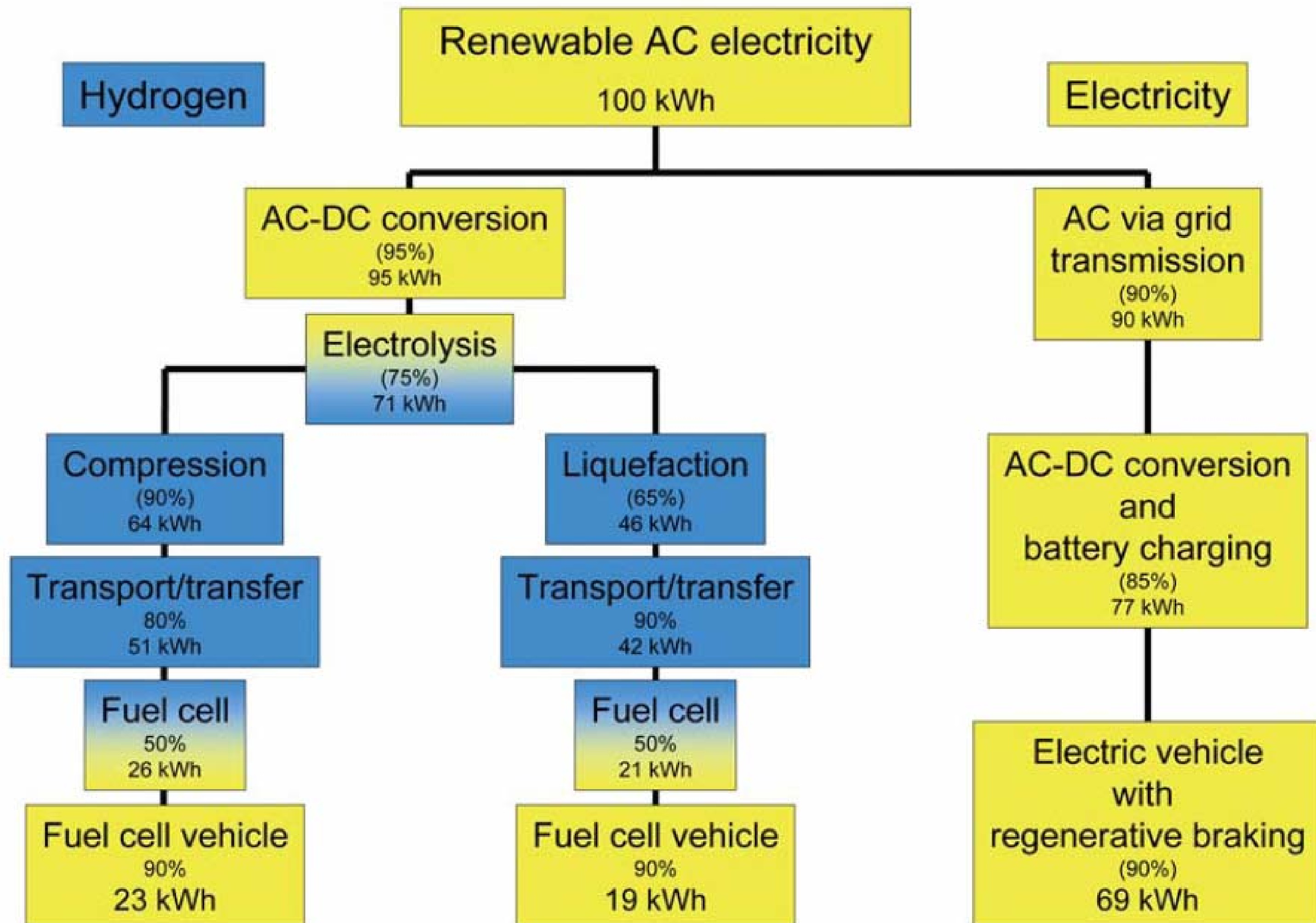
Electric Power Generation: Fuel Cells

J. Scott, Proc. IEEE, 94, 1815, Oct. 2006



H_2 Economy Does Not Makes Sense

U. Bossel, Proc. IEEE, 94, 1826, Oct. 2006



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Challenging Opportunities

- MOLECULAR COMPUTERS: The literature is full of conceptual errors about the potential of molecular computing systems. First of all a two terminal logical molecular device will never find any practical applications in realizing a practical system.
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- Thus due to heat dissipation problem, it is fundamentally impossible to envision general purpose molecular computers.

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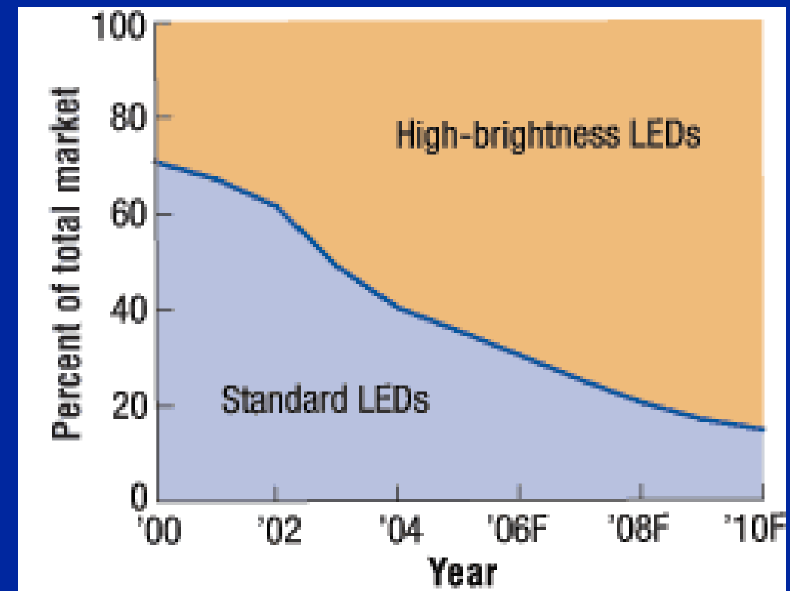
Challenging Opportunities

- Thin film silicon solar cells
- New Solid State batteries
- White Light LED
- High-brightness LEDs, including those used in room lighting systems, will account for about 86% of the world's $6.7 billion total revenues for light-emitting diode sales in 2010



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CHIP AND PACKAGING MANUFACTURING INNOVATIONS

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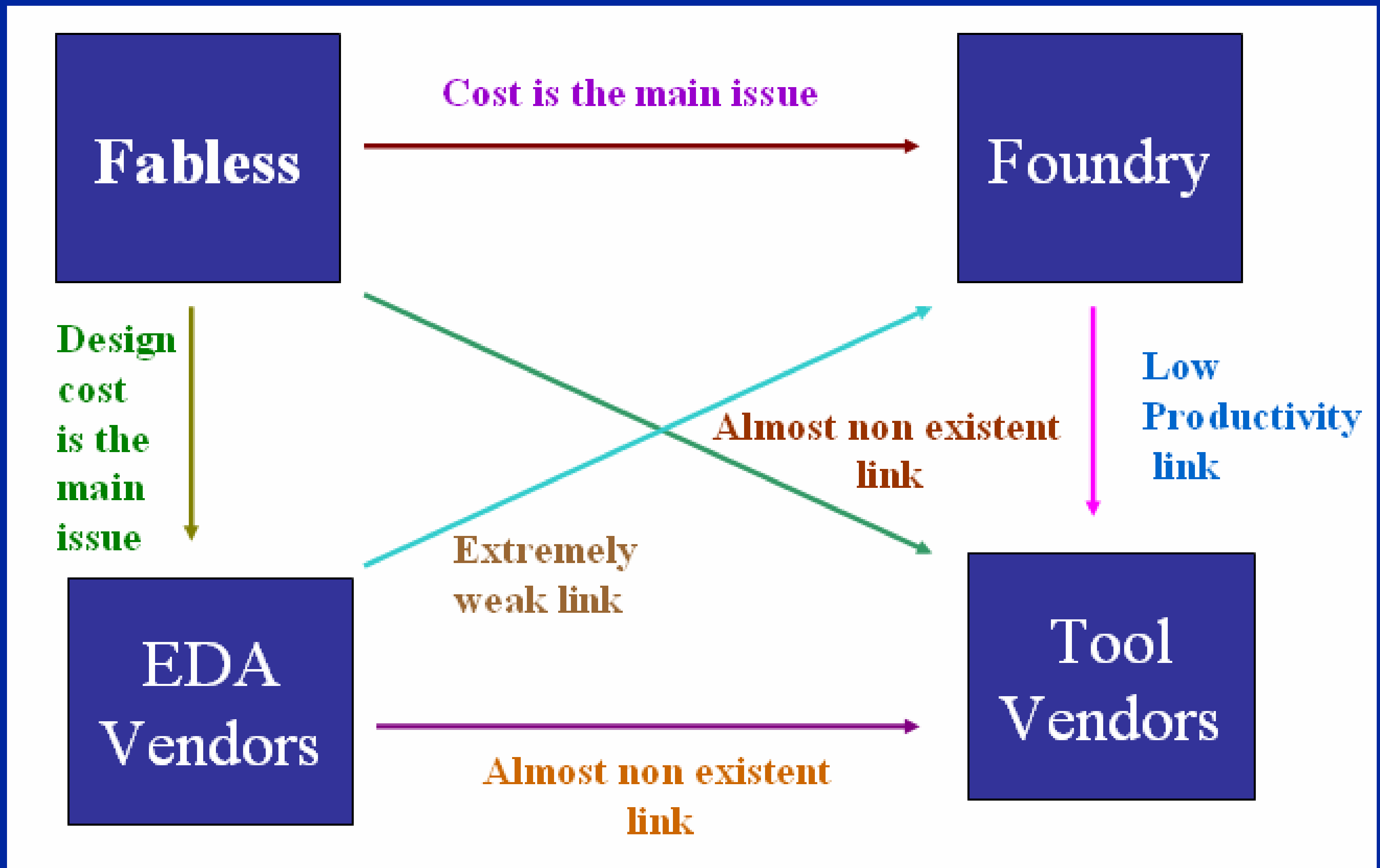
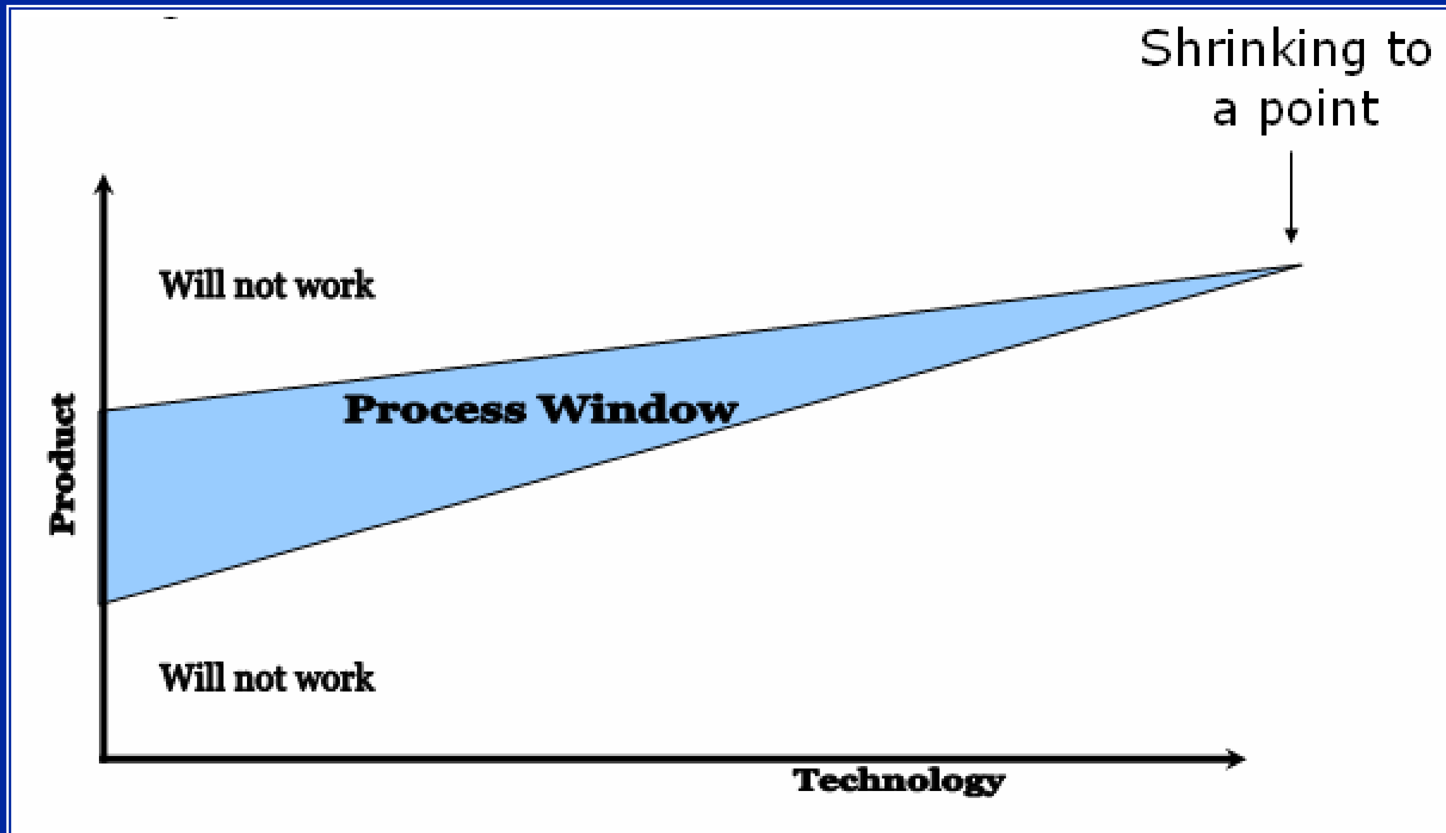
Sustainable Profitability

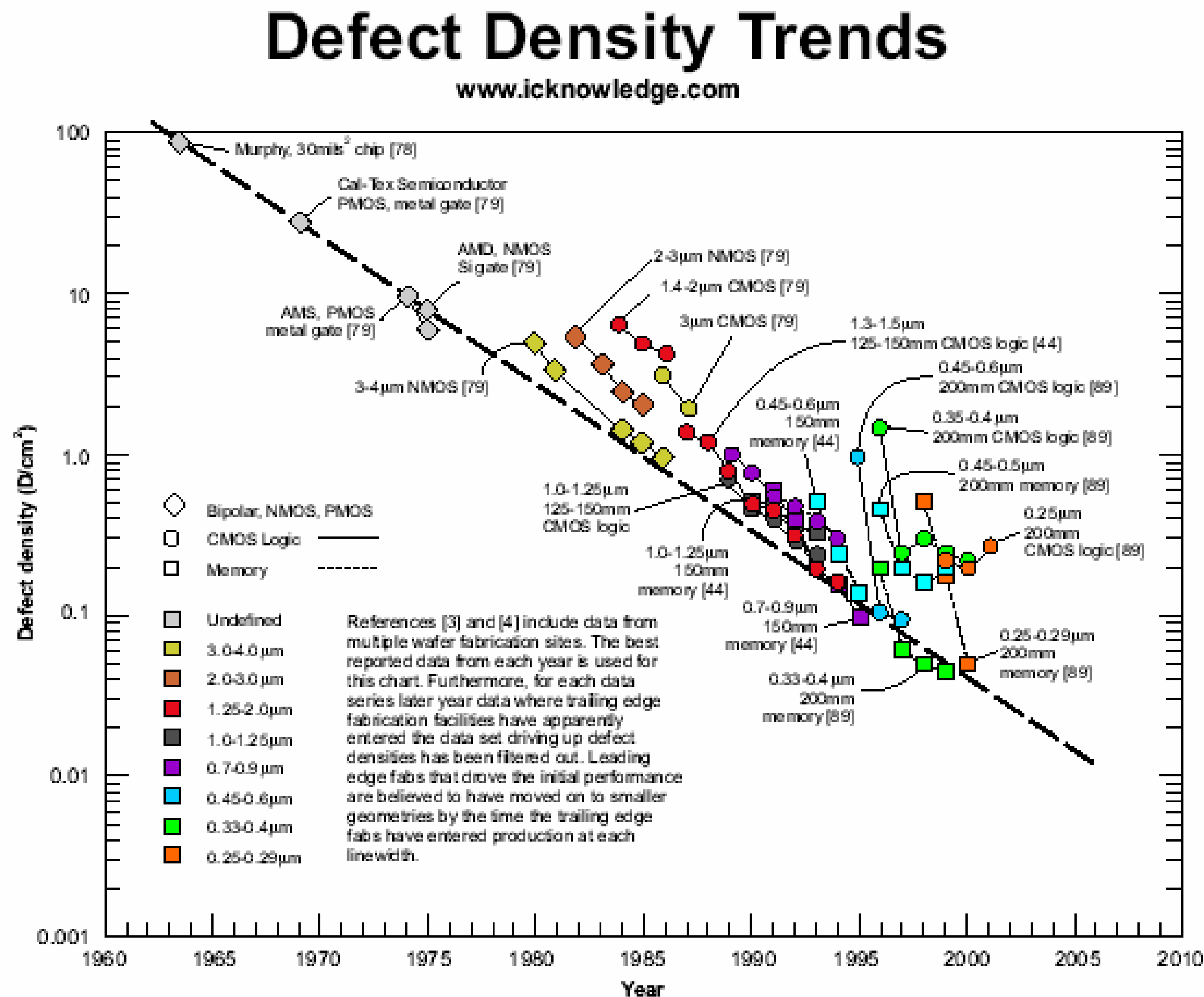


Challenges

Shrinking process window



Reduction of Defect Density



Future Lithography Requirements (ITRS)

Node (nm)	Defect Density (#/cm^2)	Throughput (# of wafers/h)	Overlay (nm)	Linewidth roughness (nm)
45	0.03	60	8.0	2.4
32	0.02	60	5.7	1.7
22	0.02	60	4.0	1.2
16	0.01	60	2.8	0.8

LITHOGRAPHY

- EUV Lithography not yet ready for manufacturing
- Nanoimprint Lithography Template defects have been driven down to <0.1 per cm^2 and imprint defects to <1.0 per cm^2
- For 32 nm node, both metrics must reach <0.01 per cm^2

Our Manufacturing Mantra

- MICROSTRUCTURE HOMOGENITY: Best Values of Performance, Reliability & Yield
- Minimize magnitude and variations of local and global thermal and residual stresses of each layer of material
- Uniform Sources for fluid and Energy Delivery in Every Tool
- R. Singh, V. Parihar, K. F. Poole and K. Rajkanan, "Semiconductor Manufacturing in the 21st Century", Semiconductor Fabtech, 9th Edition, pp. 223-232, 1999
- R. Singh & K. F. Poole, US Patent No.: US 6,569,249 B1, Date of Issue: May 27, 2003

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CURRENTLY USED SWP STEPS IN IC MANUFACTURING

BATCH PROCESSING	SINGLE WAFER PROCESSING
Wafer Processing • Furnaces for Certain thermal processing steps • Wet Cleaning for certain surface cleaning steps	Wafer Processing • All steps other than certain furnace processing and wet cleaning are SWP steps
Packaging • Most of the steps are based on batch processing	Packaging • Lithography • Some applications of SWP tools for surface cleaning

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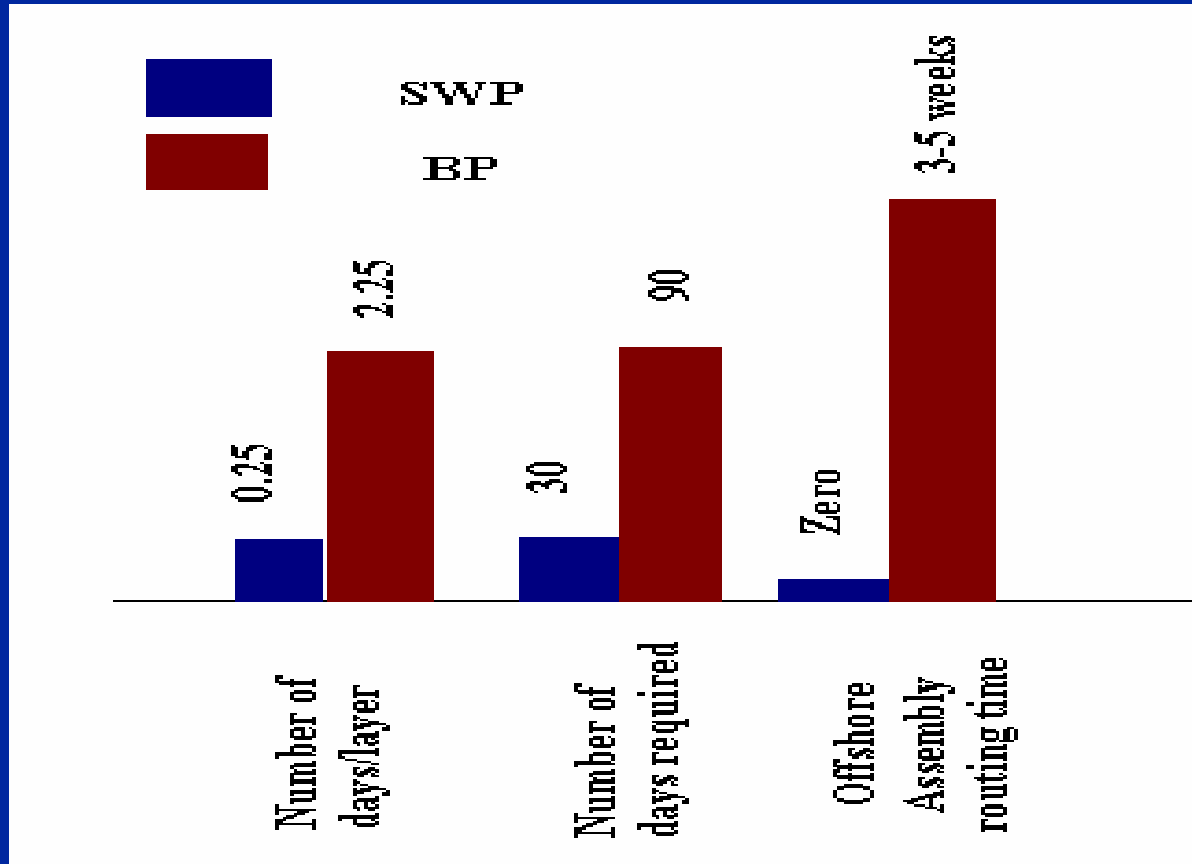
Cycle Time Advantage of Single Wafer Manufacturing



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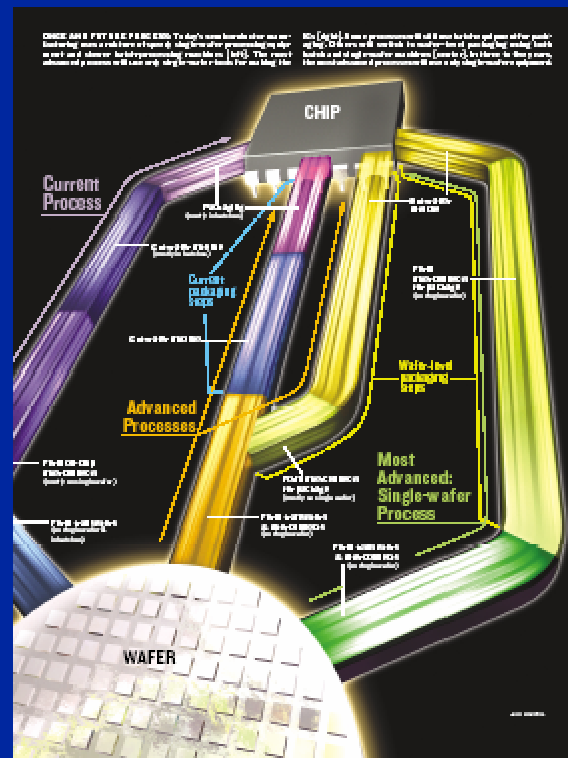
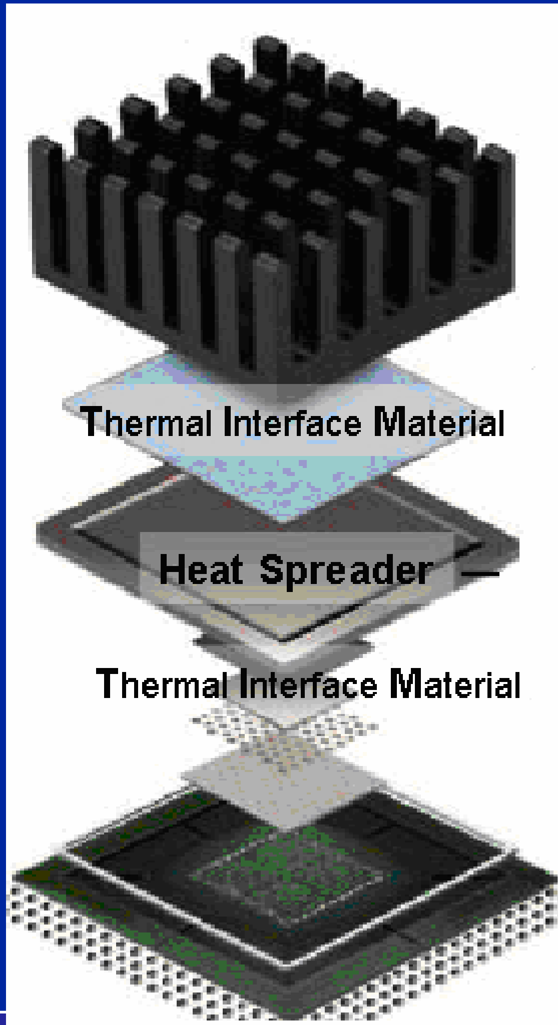
IEEE Spectrum (February 2005)

Chip Making's SINGULAR FUTURE

Ultimate Limit of Manufacturing: Single Wafer Processing



Classical Packaging Limits



- Classical Package consists of
- TIM1
- Heat Spreader
- TIM2

(TIM-Thermal Interface Material)

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Thermal Interface Material (TIM) Typical Thermal Values

Material	Bulk Thermal Conductivity (W/mK)	Typical Thermal Resistance (° K cm²/W)
High Performance Grease	0.5-10	0.08-0.15
Phase Change Material	0.5-5	0.08-0.15
Bismuth Tin	12-14	0.05-0.08
Lead Tin	30-35	0.04-0.07
Silver Tin	25-30	0.03-0.06
Indium	50-80	0.03-0.05

- Indium Based Thermal solutions are proven to provide the highest bulk conductivity and lowest Thermal resistance of the currently available technologies

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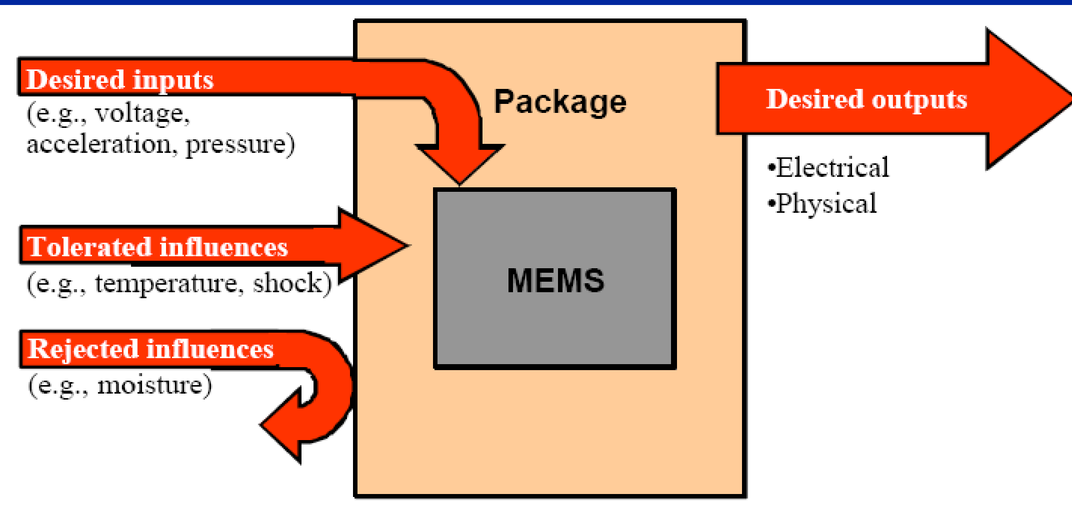
MEMS – Packaging Challenges



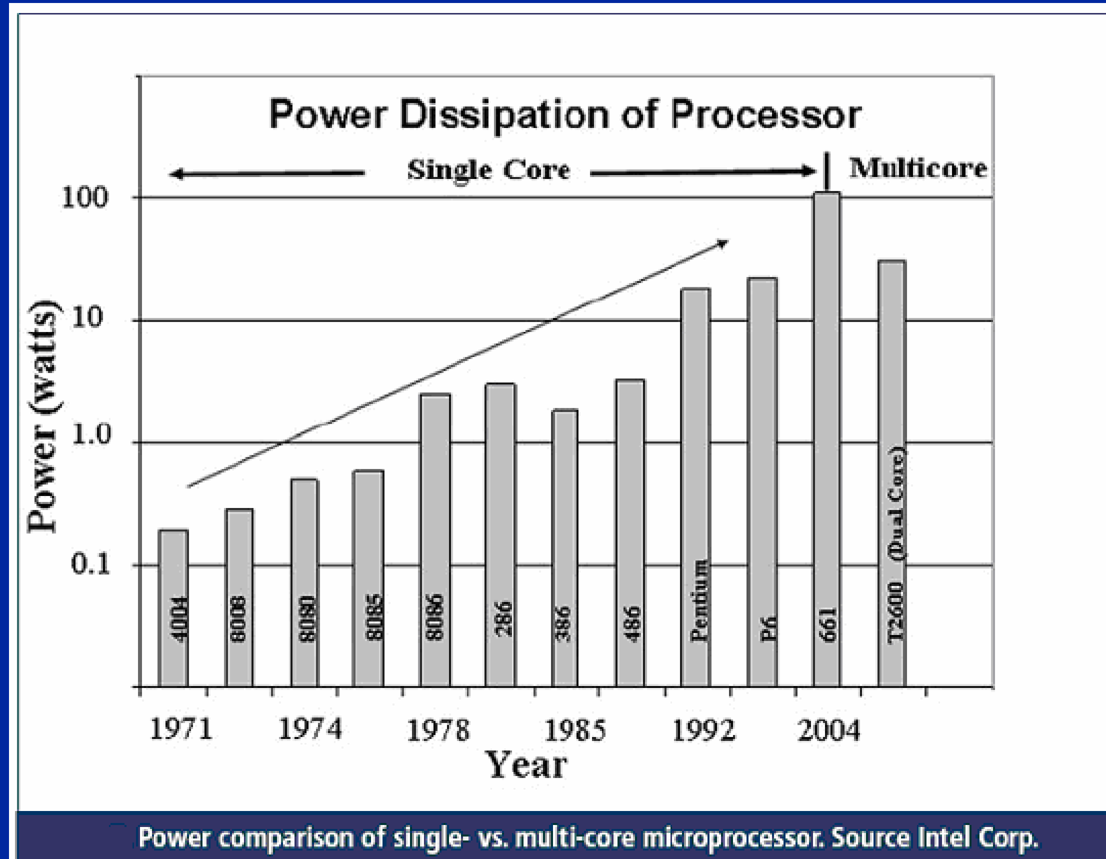
Cost effective packaging & robust reliability are two critical factors for successful launching of MEMS products.

- Unlike conventional IC packaging, some external influences on MEMS become desired inputs.
- Moving Microsystems structures create difficulty in applying traditional plastic encapsulation techniques.

Environmental factors affecting a MEMS device →

Mechanical	Chemical	Physical
Stress	Gases	Temperature
Vibration	Humidity	Pressure
Shock	Corrosion	Acceleration

Innovations in Packaging



Power comparison of single- vs. multi-core microprocessor. Source Intel Corp.

By moving from a single high speed core, to a multi-core architecture operating at a slower speed, the heat is reduced and improved performance of the packaged system is obtained.

Innovations in Packaging (Cont.)

TABLE 1. COMPARISON OF SINGLE- AND DUAL-CORE MICROPROCESSORS.

Core	Single core	Dual core
Processor name	661	T2600
Technology node (nm)	65	65
Clock speed (GHz)	3.6	2.16
Power (W)	112	31
Number of transistors (million)	125	155

Source Intel Corp.

- Multi-core architectures enable higher performance than single cores with low power dissipation.
- Due to the significant improvement in thermal efficiency, the performance of the multicore processor is high even though it runs at lower speeds.

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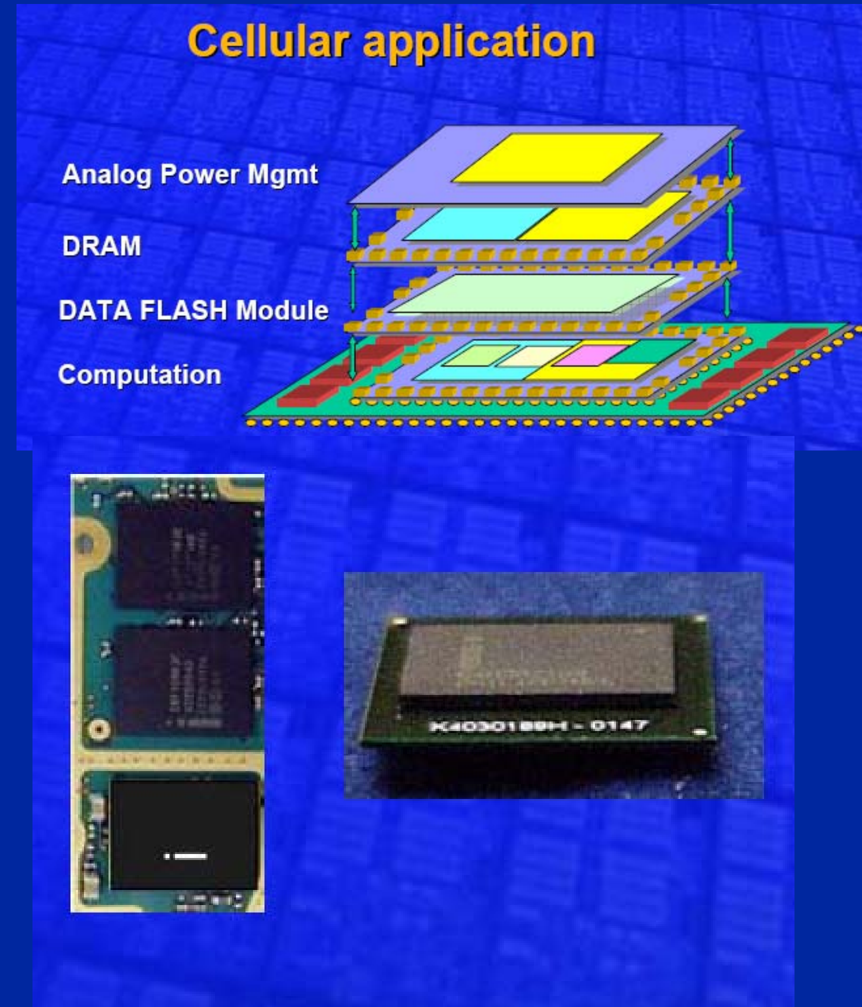
Integration via Package (SiP)

- Pragmatic SIP

  "Sub-System in a Package": Relevant functionality combined in single package (e.g. Logic + Memory, RF etc.) when it makes **business & technical** sense

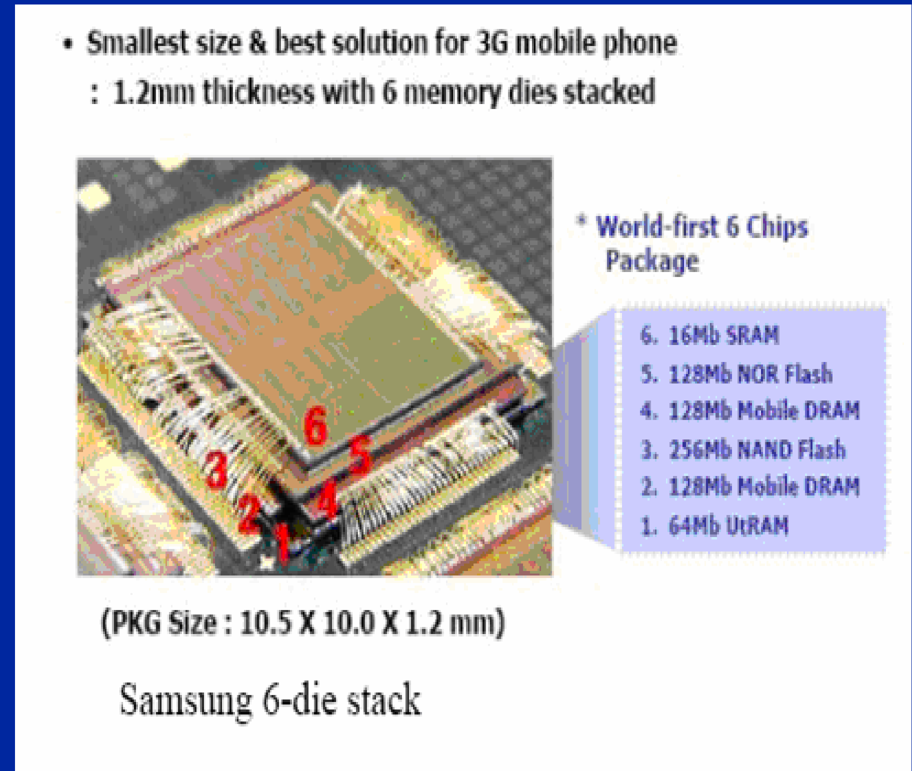
- Ultimate SIP

  Single multi-function, package with all needed system-level functions (e.g. Analog, Digital, Optical, RF and MEMs)



Chip Stacking (Limits)

- This method stacks fully processed and tested standalone components to produce a system-in package (SiP).
- The components in the vertical stack are connected with traditional wire bonding or flipchip techniques.
- Research groups have announced functional stacks of as many as eight chips.



Samsung 6-die stack

System on a Chip

- Definition: Integration of all components into a single chip
- Integrating similar technologies provides cost and performance/power advantages
- Example: Logic, processing, SRAM, etc in Digital CMOS
- Integrating dissimilar technologies requires balancing cost, process, and functional tradeoffs
- Embedded DRAM
- SiGe + CMOS
- Flash Memory + Logic

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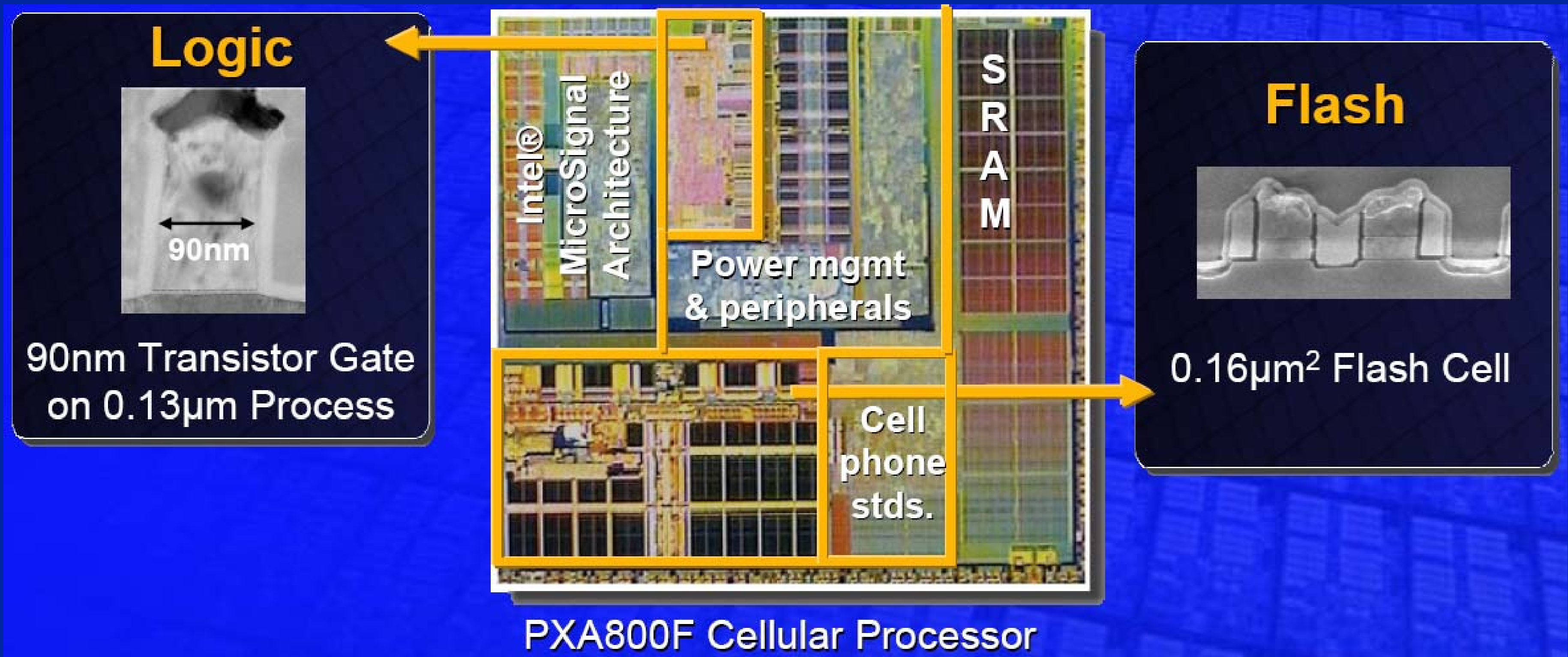
Integration Via Silicon (SoC)



Density, Speed, & Power Consumption are improved…
Cost, complexity, and flexibility suffer

Source: Intel

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NEW COMPUTER ARCHITECTURES

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Computer Architectures

- With the availability of low-cost ultra high speed silicon based nanoelectronics, breakthrough in computer architecture can lead to major advancements in computing systems.
- DNA width of 2 nm is true representative of nanotechnology operating in nature for as many years as DNA based living systems have existed.
- The number of neurons in the human brain is estimated to be at approximately 100 billion.

Computer Architectures (contd.)

- With an average of 1000 neurons per connections, there are approximately 100 trillion connections in an average human brain
- With slow switching speed of the order of 10^{-3} s, human brain handles a power density of the order of nW/cm^2 to $\mu W/cm^2$ very well.
- Past progress of artificial intelligence systems and artificial neural network systems has been less than satisfactory.

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Computer Architectures (contd.)

- For future progress, one has to study the relationship of mind and brain from a new philosophical point of view. The new philosophical approach must take into account the fact that we have low-cost ultra high speed and reliable logical devices and a massive amount of memory at our hand
- Recently Federal Drug Administration (FDA) approved vagus nerve simulation system that can be implanted under the collarbone and send an electrical signal to the part of the brain that seems to regulate moods.

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Computer Architectures (contd.)

- The fact that relationship between brain and mind is being established in current clinical approaches, one has to focus into research directions that will lead to invention of new computer architectures that will exploit the relationship between mind and brain and capitalize on the low-cost and reliable hardware available for developing computing systems beyond our current thinking.

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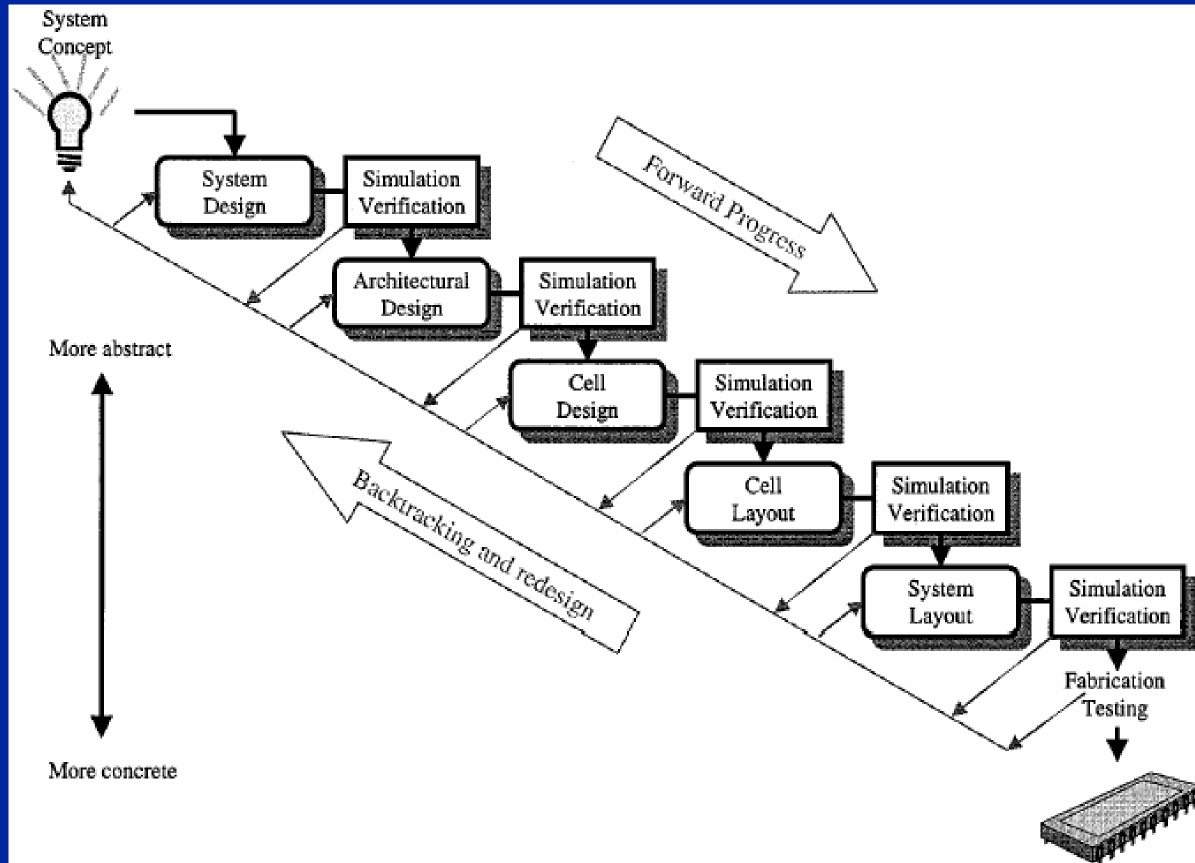
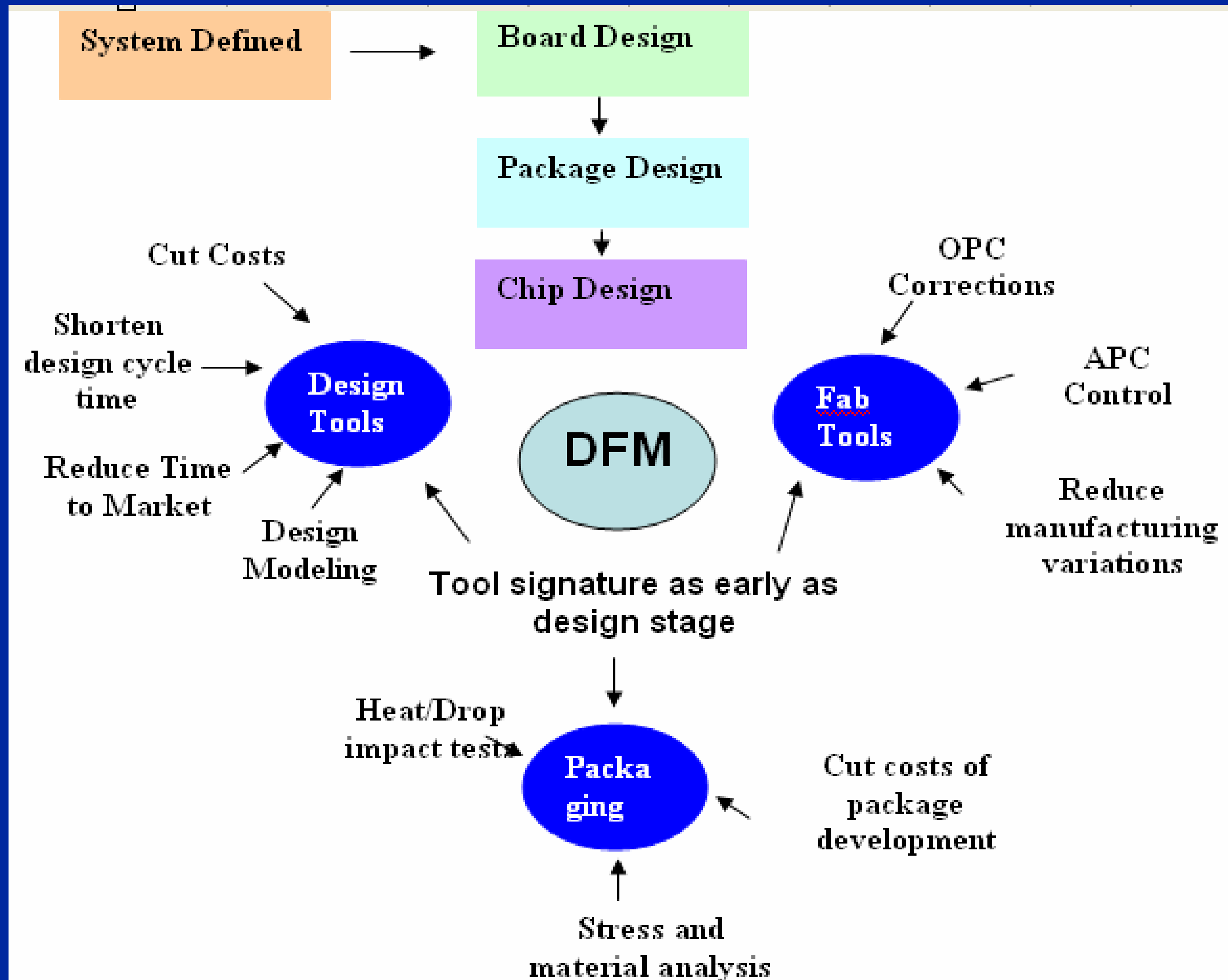
INNOVATIVE DESIGN

CHALLANGES



Design, Fab and Packaging



Design for Manufacturing (DFM)

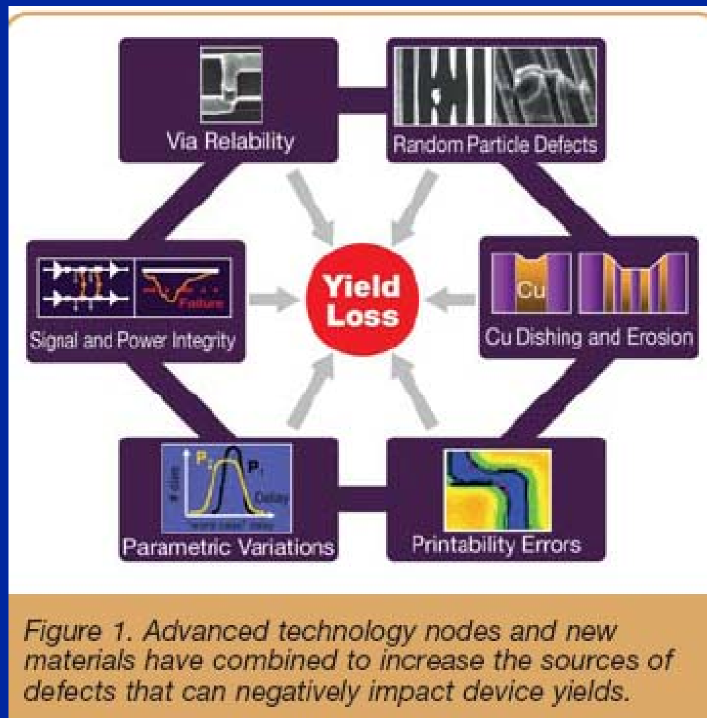


Figure 1. Advanced technology nodes and new materials have combined to increase the sources of defects that can negatively impact device yields.

- DFM is connections within designs, connections within the manufacturing flow, and connections between Design and Manufacturing
- Ref. Future Fab Int. # 22, p. 38, Jan 2007

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DFM (contd.)

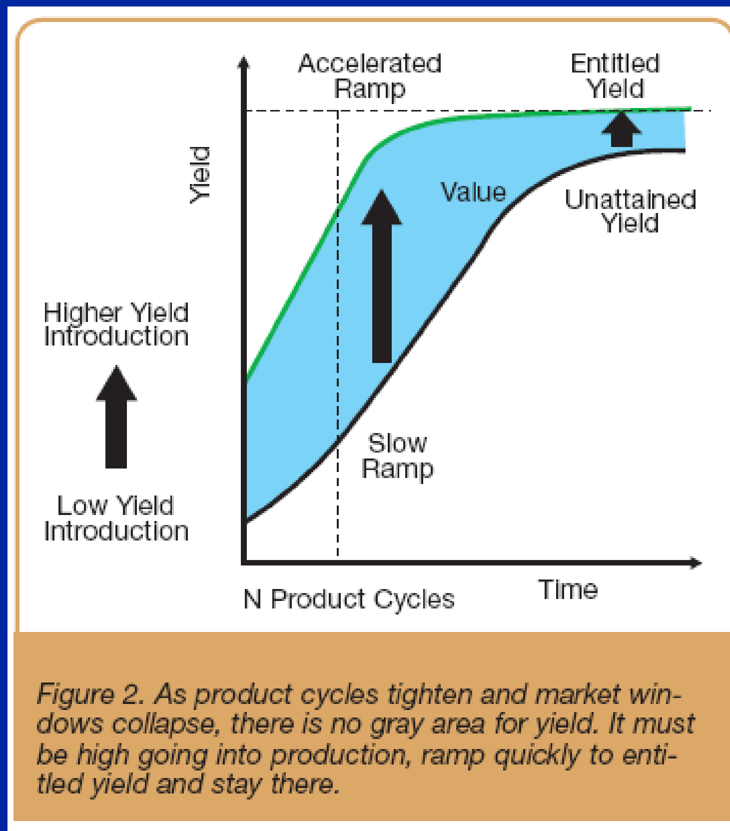
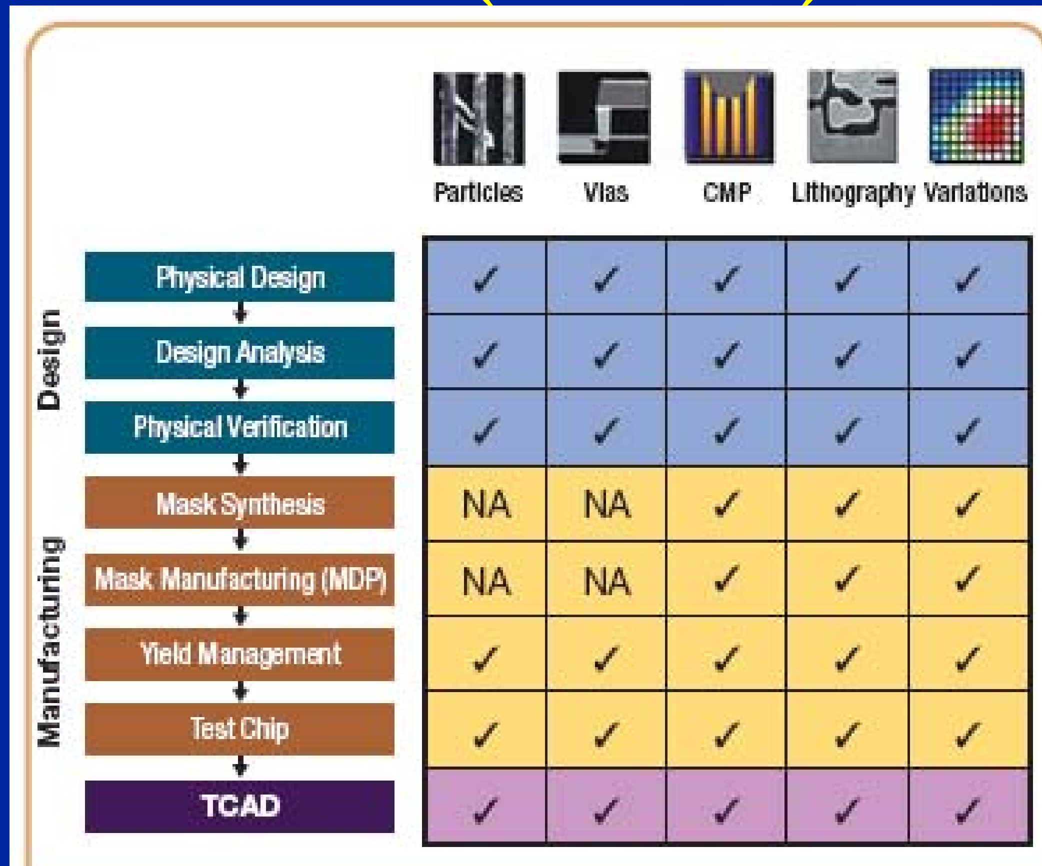


Figure 2. As product cycles tighten and market windows collapse, there is no gray area for yield. It must be high going into production, ramp quickly to entitled yield and stay there.

- Random defects are no longer primary focus of yield loss. Unlike in the past systematic and parametric defects are major cause of yield loss.
- Market Windows are collapsing from months to weeks.
- Ref. Future Fab Int. # 22, p. 38, Jan 2007

DFM (contd.)



		Particles	Vias	CMP	Lithography	Variations
Design	Physical Design	✓	✓	✓	✓	✓
	Design Analysis	✓	✓	✓	✓	✓
	Physical Verification	✓	✓	✓	✓	✓
Manufacturing	Mask Synthesis	NA	NA	✓	✓	✓
	Mask Manufacturing (MDP)	NA	NA	✓	✓	✓
	Yield Management	✓	✓	✓	✓	✓
	Test Chip	✓	✓	✓	✓	✓
	TCAD	✓	✓	✓	✓	✓

Figure 3. The evolution of the design-to-manufacturing flow has necessitated a shift away from point tools to fully integrated solutions that can take into account a host of yield-limiting defect types and sources.

DFM (Contd.)

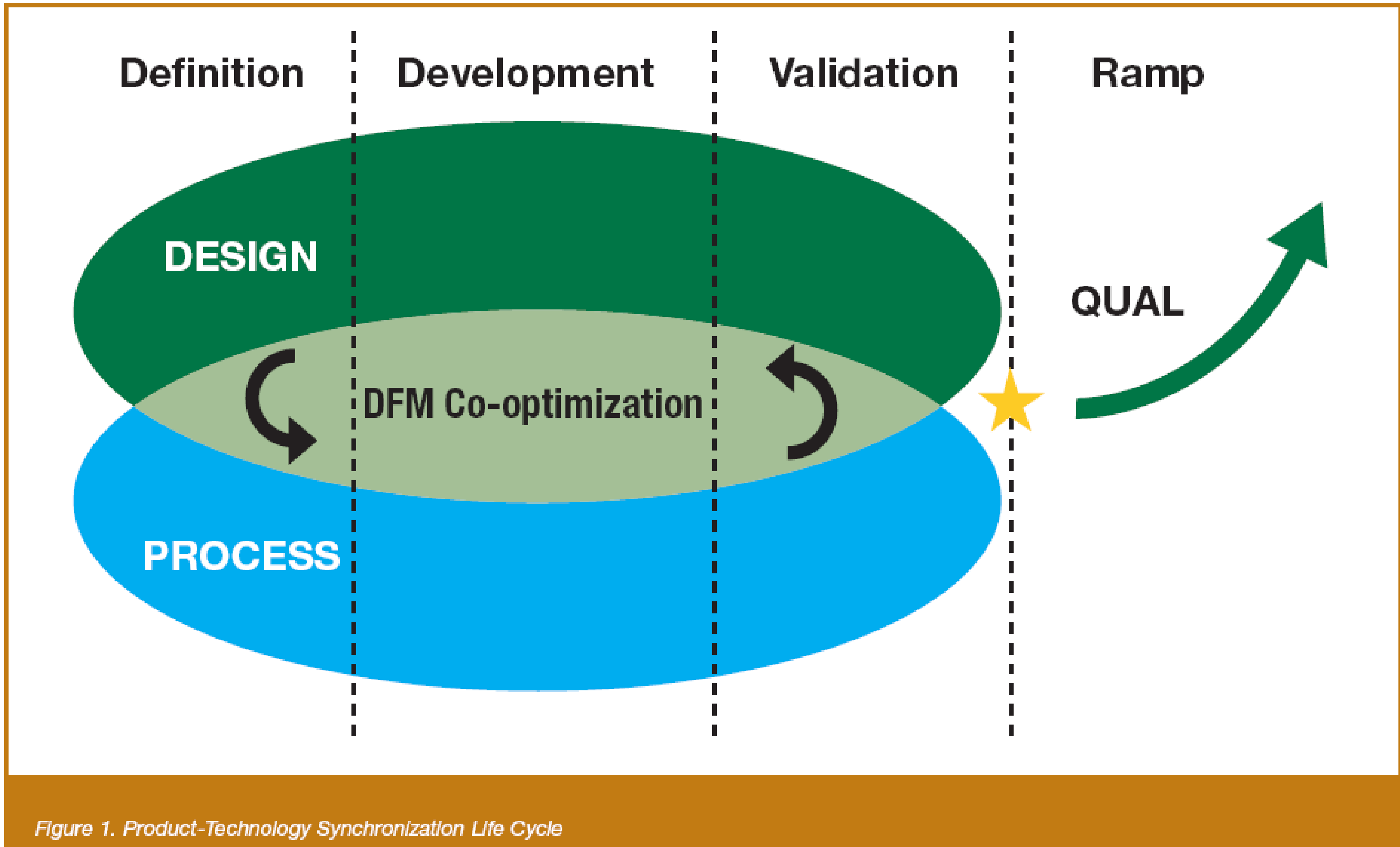


Figure 1. Product-Technology Synchronization Life Cycle

PLATFORM INTEGRATION

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Convergent Systems are driver of future growth

- Convergence of audio, data, voice, sensing etc. in a single system
- Convergent systems are providing convergence of computer, telecom, and consumer products on one platform
- System on Chip (SOC) and System in Package (SIP) are two different approaches to meet the goal of convergence
- Sensor Integration & energy conversion device integration are potential growth areas for convergent systems

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Convergent Systems (contd.)

- Materials problems related to system integration are highly challenging (lesson learned from a failed GaAs/Si Venture of Motorola)
- As shown in the early slide, Cell Phones will be used for platform integration for convergent systems and will provide more growth than one was thinking couple of years back

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NEW BUSINESS OPPORTUNITIES

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COMMON MAN ELECTRONICS MARKET

- THERE ARE ABOUT 1 BILLION HUMAN BEINGS ON THE EARTH WHO ARE READY TO PURCHASE AN ELECTRONIC DEVICE (SERVING THE PURPOSE OF COMPUTER, & CELL PHONE ETC.) PROVIDED THE COST is ABOUT $100. THESE DEVICES MUST HAVE "ACCESS", "AVAILABILITY" AND "AFFORDABILITY".
- THE $100 BILLION ELECTRONICS MARKET IS NOT FOCUS OF ATTENTION OF LARGE CORPORTATIONS
- UNIQUE OPPORTUNITY FOR LESS DEVELOPED COUNTRIES TO TAKE ADVANTAHE OF THIS MARKET
- THESE DEVICES WILL BECOME EDUCATIONAL TOOLS AND HELP IN REOMVAL OF POVERTY

CONCLUSIONS

- Profitability is the main issue
- Only system level innovation will lead to profitable new products
- Defect density and throughput main manufacturing challenges
- Opportunities exist to change business models and create paradigm shift
- Consider both technical and business issues in your R & D plan (you can not separate them any more)

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