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Southern Minnesota Section Newsletter

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Integrated Circuit Noise Isolation and Signal Integrity: A Resource and Time To Market Challenge!

On starting work at IBM in 1977, I joined an Integrated Circuit (IC) department that worked on ICs that were called "**specials**." As I soon learned, these were IC's that very few other groups wanted to work on; mainly because these chips contained analog and other non-binary or digital, noise sensitive circuits. The big problems always seemed to be unwanted signal interactions between the sensitive and noisy circuits mixed on the same chip. There weren't many good tools to predict the interactions with the result being occasional "surprises" when the early hardware was evaluated. Today we call these chips "**mixed-signal**" ICs and even straight digital logic circuits are being bothered by unwanted signal interactions from other digital circuits on the same chip. Since the world people deal with is analog, putting Systems On a Chip (SoC) means that we have large mixed-signal systems with analog and digital circuits & signals. Adding sensitive analog circuitry to these ICs is becoming a more difficult and time consuming task. This may be at the cost of special packaging, custom chip floor-planning, custom power bus routing, strict partitioning of noisy and noise sensitive functions, custom shielding and isolation structures, extensive and time consuming use of CAD, a fully custom design effort for the analog or sensitive portions of the chip and usually much increased resource and/or time to market for the chip. With the mask build and processing costs of a single state of the art CMOS IC exceeding a million US dollars, there is more emphasis than ever on making sure that there are no interaction "surprises" that occur when the chips come back from build. Until recently, CAD to analyze potential chip noise interaction problems required the designer to limit the analysis area to a small portion of the chip. Dramatic improvements in design/analysis CAD and specifically chip substrate extraction/simulation CAD, is allowing designers to predict and repair many more complex interaction problems on larger chips prior to building the IC. The increasing cost of prototype IC design runs and the time to market penalty of non-operational prototype hardware justify the added resource and complexity of the use of this CAD. Still, many design teams "roll the dice" and gamble that they will not have an unexpected interaction problem, rather than pay the time and resource penalty of using the prediction CAD. This presentation will address how the complexity increase in implementing this more accurate CAD environment can be reduced by hierarchical CAD use and up front design for signal integrity control. I will introduce a "best practices" design flow, survey key mixed-signal & RF SoC problem areas, and survey best practices chip and circuit design techniques. These design techniques will lower the risk of unwanted interaction problems, even if complete CAD simulation of the interactions isn't performed.

IEEE-USA Position Statements

IEEE-USA position statements identify important technical and/or engineering career-related aspects of specific public policy issues deemed to be of concern or affecting IEEE's U.S. members. They make specific public policy recommendations and provide recommended approaches for consideration by the U.S. Congress, Executive Branch officials, the Judiciary, representatives of State and Local Government, and other interested groups and individuals, including IEEE members. Topics include:

- Aeronautics, Space & Transportation
- Competitiveness & Innovation
- Computers & Communications
- Education Issues
- Energy & Environment
- Engineering Workforce
- Intellectual Property
- Medical Tech. & Health
- Research & Development
- Retirement Security

For more information, visit:
http://www.ieeeusa.org/forum/POSITIONS/index.html

Integrated Circuit Noise Isolation and Signal Integrity: A Resource and Time To Market Challenge!

Featuring: Timothy Schmerbeck

Monday, September 13th, 6:30 pm
Mayo Medical Sciences Building
(321 3rd Avenue SW, Rochester)

► Pizza at 6:30; Meeting at 7:00 ◄

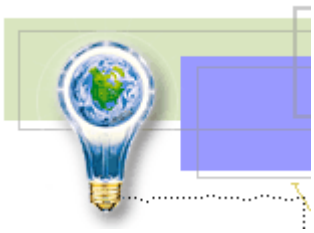
Timothy Schmerbeck is a senior member of the Integrated Circuit (IC) development team in JDS Uniphase's Datacom Products Division at Rochester, Minnesota. He has over 27 years of experience designing IC's. He received bachelor's, and master's degrees in electrical engineering from the University of Minnesota, Institute of Technology, in 1977 & 1985 respectively. His graduate work dealt with the design of a hybrid, integrated, analog signal processor IC for disk drive servo systems.

He joined the Integrated Circuit (IC) design group at IBM in Rochester, MN in 1977 where he spent roughly 25 years working on virtually every aspect of analog and digital IC design & development for storage, communications, and computer systems. He has specialized in mixed analog and digital IC designs and has been teaching on the subject of IC signal integrity at seminars, worldwide, for over a decade. Those seminars have influenced the development of the only chip substrate signal integrity analysis CAD on the market today. He has been given numerous IBM corporate and division awards and corporate honors including the title of Master Inventor.

Since the acquisition of the IBM optical communications group by JDS Uniphase in December 2001, he has continued to be involved with the design of 1 to 10 GHz optical transceiver ICs.

He has been involved with IEEE since 1975 when he was treasurer of the University of Minnesota student chapter. He is on the Teaching Advisory Board of MEAD Education. He has authored and contributed to numerous technical publications, conference presentations, panel sessions, tutorials, workshops, books, college courses, and holds many patents in IC design.

In his spare time he studies theology and enjoys contemplating the works of the greatest engineer.



Discover Engineering

Visit: http://www.discoverengineering.org/

New Faces of Engineering 2005

A Recognition Program Sponsored by Engineers Week

The New Faces of Engineering strives to promote the accomplishments of young engineers by highlighting their engineering contributions and the resulting impact on society. The campaign is designed to enhance and improve the image of engineering by:

- Putting faces to what has often been referred to as "the stealth profession";
- Showing a group of young, diverse and talented engineers, thereby portraying engineering as an exciting profession open to everyone;
- Providing both stimulation and incentive for college engineering students to explore the variety of career options available to them with their engineering degrees as well as encouraging high school students to study engineering in college.
- Help students understand they are part of a global profession.

Criteria for Recognition:

- Engineers 30 years of age or younger are the focus of the recognition program.
- Engineers Week sponsoring societies will nominate young working engineers from among their membership.
- New Faces of Engineering recognizes achievements in all engineering disciplines
- Societies with international chapters are requested to nominate 2 of their 5 candidates from outside the U.S.

The deadline for individual nominations is October 1st. For further information and nomination form please visit:
http://www.eweek.org/site/News/Eweek/2005_Nominations.shtml

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