



Southern Minnesota Section Newsletter

Published by the Southern Minnesota Section of the Institute of Electrical and Electronics Engineers

January 2000

Parallel Compilation & Execution

by John Willis

Computing applications grow steadily in their need to handle larger data sets, to perform more complex analysis of these data sets, and to deliver more complex forms of user interaction. This growth demands comparable increases in the available computing power. My presentation at the January 17 IEEE meeting will focus on meeting this demand through parallel compilation and execution with a specific focus on FTL Systems' Auriga®.

Through fundamental changes in the computing system and processor industry, the raw performance and capacity needs of high-end applications are more efficiently met by multiple processors than by higher-performance but much lower-volume uniprocessors. A 150% performance increase can be achieved with less than a 20% cost increase through multiprocessing, but with more than a 100% cost increase through faster uniprocessors, for leading-edge systems using high-volume commodity processors. The case for multiprocessing improves more than linearly with increasing performance demand -- until the faster uniprocessor is simply infeasible.

Meeting customer demands requires not only the raw performance and capacity that is latent in multiple processor systems; also required is suitable application software capable of scalable parallel operation. Expert programming talent skilled in parallel software design and development suffers from a short supply. Design, development and test cycles for manually generated parallel applications result in costs and risks which substantially exceed sequential program development costs. Frequently, the need for fundamentally new data structures and implementation for effective parallel operation prevents effective migration of legacy application implementations. As a result of these three factors, the very limited availability of effective parallel computing applications seldom motivates use of multiple processor systems beyond multi-tasking of largely unrelated computing applications.

Over the last five years, FTL Systems has developed the Auriga® family of parallel compilers and execution environments to facilitate both parallel compilation and parallel execution with little explicit effort on developer's part. In order to provide for transparent parallelization, the compilers use source languages which have well-defined communicating sequential process semantics. Current production announcements center on the VHDL hardware description languages. Target computing systems transparently range from uniprocessors, through multiprocessors, up to the largest massively parallel processors available.

FTL Systems does much of its research and development in Rochester, Minnesota. Following the growth of communicating sequential process languages in Europe, FTL Systems UK Ltd. is opening a new R&D center near Southampton, England.

FTL Systems began business in 1995 under DARPA research contracts, US Air Force research contracts and commercial funding. Today, its focus is shifting from an R&D to support of customers worldwide. The talk will conclude with some of the interesting aspects of launching and sustaining a local company into a worldwide market.

IEEE Computer Society & Section Joint Meeting

John Willis, FTL Systems
Parallel Compilation & Execution

Monday, January 17, 7:00 pm
Mayo Medical Sciences Building
(321 3rd Avenue SW, Rochester)

☞ *Pizza & socializing at 6:30 pm* ☜

John Willis is CEO of FTL Systems, Inc., and managing director of FTL Systems UK Ltd. He completed his PhD in 1991 at Carnegie Mellon University, Pittsburgh. Previously he worked in computer architecture at Philips and IBM. He is the author of more than fifty academic publications and patents.



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