

TPCI-X 2.0: Bandwidth and Reliability for the Future

By Ross Franke

Recently, new Ethernet, Fiber Channel, and IB (Infiniband) standards have been created supporting data rates of 10 Gb/sec (gigabit per second) or more. The creation of these standards requires an infrastructure capable of supporting these rapidly increasing data rates.

In anticipation of system needs, the PCI (Peripheral Component Interconnect) SIG (Special Interest Group) created the 2.0 revision of the PCI-X addendum to the PCI Local Bus Specification. The PCI-X 2.0 protocol specification was approved in July of 2002.

PCI-X 2.0 provides an infrastructure with a bandwidth of more than 4 GB/sec (gigabyte per second). Along with increased bandwidth, PCI-X has enhanced the PCI protocol for more efficient use of the bandwidth.

Not only is bus speed a concern but today's consumer of computer technology requires improved RAS (reliability, availability and serviceability) features. The PCI-X 2.0 specification addresses RAS by incorporating features used in memory architectures such as ECC (error correction code).

The presentation will be an overview of the evolution from PCI to PCI-X demonstrating why PCI-X is the primary bus architecture used in servers and workstations for connecting IOAs (input/output adapters) to the system processor. The topics that will be covered are the increased bandwidth of PCI-X attained using source synchronous clocking, protocol changes that improve the efficiency of the PCI bus, new RAS features built into PCI-X 2.0 such as ECC protection, and a few niche architectural changes in PCI-X 2.0.

IEEE Section Meeting

Ross Franke
IBM Rochester

TPCI-X 2.0: Bandwidth and Reliability for the Future

Monday, January 20, 6:30 pm
Mayo Medical Sciences Building
(321 3rd Avenue SW, Rochester)

◆ Pizza at 6:30; Meeting at 7:00 ☞

Ross Franke earned his bachelor's degree in electrical engineering at Michigan Technological University (MTU) in 1999. While attending MTU, Ross was a member of the IEEE student organization and held both vice-chair and treasurer positions during his membership.

After graduating from MTU, he joined IBM's Server Group. Initially his role was writing diagnostic microcode for PCI-based LAN (local area network) adapters. Since 2000, Ross has been involved with the development and implementation of PCI-X bridges for use in server applications. His PCI/PCI-X expertise is relied upon by the IBM Server Group to debug PCI hardware and software problems.

In September 2002 Ross was a presenter on PCI-X 2.0 at two developers' conferences hosted by the PCI Special Interest Group.



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