Reliability Study of Split Gate Silicon Nanocrystal Flash EEPROM

Cheong Min Hong, Jane Yater, Sung-Taeg Kang, Horacio Gasquet, Gowrishankar Chindalore
Technology Solutions Organization, Freescale Semiconductor, Inc., Austin, Texas, *cheong.m.hong@freescale.com*

Introduction

Silicon nanocrystal nonvolatile memories have been identified as one of the leading candidates to replace floating gate nonvolatile memories for embedded microcontrollers at 90nm node and beyond [1, 2]. Split gate nonvolatile memories [3, 4, 5] employing source side injection (SSI) have the advantages of low program current and large program window. Owing to the thin dielectrics used in these memories, one main concern is the long term reliability such as data retention and program disturb. Charge loss can occur from the nanocrystals through the top oxide or bottom oxide. Developing a good understanding on the path of charge loss is important for optimizing the reliability of split gate nanocrystal nonvolatile memories.

In this paper, we present a measurement based on biased data retention to determine the direction of charge loss. Top oxide and bottom oxide thickness can be optimized to meet long term reliability goal. A split gate nanocrystal nonvolatile memory with large program window, while demonstrating excellent data retention and program disturb characteristics is also presented.

Results and Discussion

High temperature data retention plots of split gate nanocrystal Flash single bitcells as well as that for an array with single gate nanocrystal Flash (1T-Flash) are shown in Figure 1. The split gate nanocrystal devices are programmed by source-side injection (SSI) while the single gate nanocrystal devices are programmed by conventional hot carrier injection (HCI). The threshold voltage (V_t) losses for both types of devices are comparable even though the split gate bitcells have a 76% larger V_t window. However, the nanocrystal stack used in the split gate sample is about 20% thicker than that of the single gate sample, which may be partially offsetting the effect of larger operating window. Room temperature biased data retention plots for various split gate nanocrystal nonvolatile memory samples are shown in Figure 2. For low control gate bias ($V_{cg} < 0V$), the primary charge loss occurs through the bottom oxide is evident from the observation that increasing bottom oxide thickness substantially reduces the V_t loss. On the other hand, for higher control gate biases, the charge loss can be minimized by thickening the top oxide which indicates that the charge loss is through top oxide in this bias regime. At the cross-over of these two voltage regimes there is a small bias region with a charge loss minima. By changing the balance of top and bottom oxide thickness, the minimum charge loss point can be made to move along the control gate bias as desired. Figure 3 shows the unbiased retention characteristics for different bottom oxide / top oxide combinations. Since most of the unbiased retention loss occurs in the low gate bias regime, increasing bottom oxide thickness improves charge retention while increasing the thickness of top oxide has no effect. Figure 4 shows the unbiased data retention characteristics at room temperature and 150°C. The results indicate no discernible thermal acceleration of charge loss. The effect of cycling on data retention is shown in Figure 5. A steeper slope at the earlier phase indicates additional charge loss from oxide traps generated during cycling. After one week of 150°C retention bake, both uncycled and cycled bitcells exhibit similar rate of V_t loss.

Figure 6 shows the high temperature (150°C) retention characteristics of bitcells programmed to different V_t windows. Larger charge loss with increasing threshold window is observed due to increasing internal electric field within the nanocrystal stack. However, the charge loss accelerates by only about 80mV even when the V_t window is increased by as much as 1V. This result shows that the split gate nanocrystal Flash maintains robust charge retention even under a wide range of program window. The effect of natural V_t on data retention is shown in Figure 7. Negative natural V_t is achieved by implanting a highly doped n-type region near the surface using a heavy atom such as phosphorus or antimony [6]. Devices over a range of 900mV in natural V_t differ by only about 60mV in V_t loss after about one month of 150°C data retention bake. This result shows that increasing counter-doping does not adversely affect retention characteristics despite higher internal electric field. Figure 8 shows the program disturb characteristics for a typical bitcell corresponding to a program control gate bias of 9V. No discernable disturb is observed for a device in the programmed state. For a device in the erased state, at least a 10x margin beyond the targeted maximum disturb time is achieved.

Conclusion

A split gate silicon nanocrystal nonvolatile memory with robust reliability has been demonstrated. The understanding of charge loss at different bias regimes allows an optimization of the nanocrystal stack. In addition to having a large program window, the device exhibits good retention characteristics across temperature, cycling, and natural threshold voltage. The results strongly suggest that the split gate silicon nanocrystal nonvolatile memories will continue to be an attractive candidate to replace floating gate nonvolatile memories for 90nm node and beyond.

References

[1] R. Muralidhar, et al., IEDM, Dec. 2003, p. 601.
[2] R. Steimle, et al., IEEE Conf. on Nanotechnology, Aug. 2004, p. 290.
[3] T. Osabe et al., VLSI Symposium Tech. Dig., 2004, p. 242.
[4] L. Breuil, et al. IEEE TED, Oct 2005, p 2250.
[5] J. Yater, et al., NVSMW, 2006, p. 60.
[6] C. Swift, et al., NVSMW, 2006, p. 56.

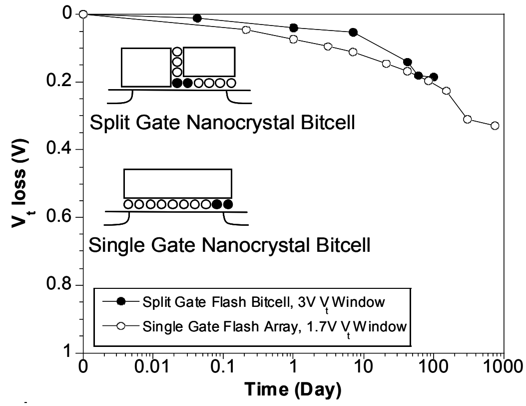

Figure 1: Effect of Bitcell Structure on 150°C Retention

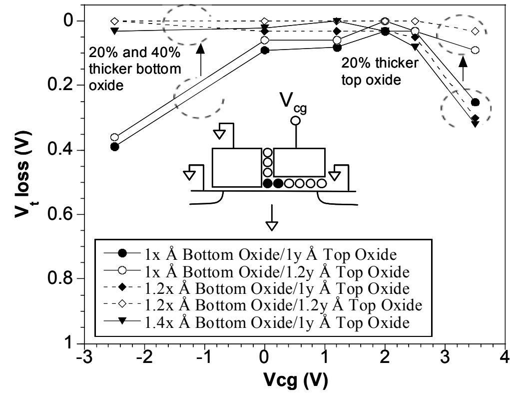

Figure 2: Room Temperature Biased Retention

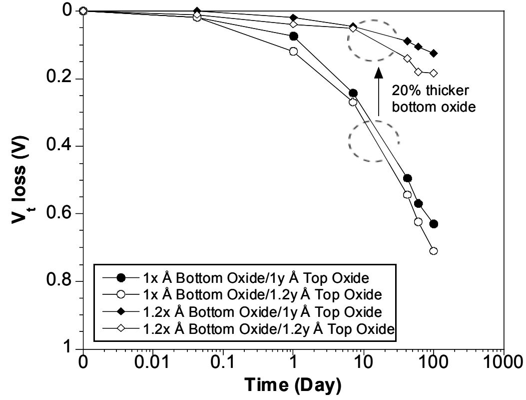

Figure 3: Effect of Oxide Thickness on 150°C Retention

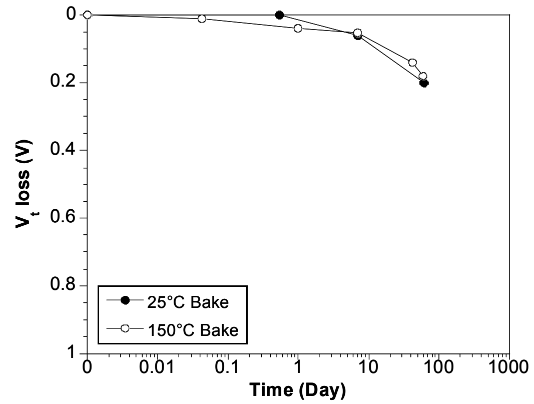

Figure 4: Effect of Temperature on Retention

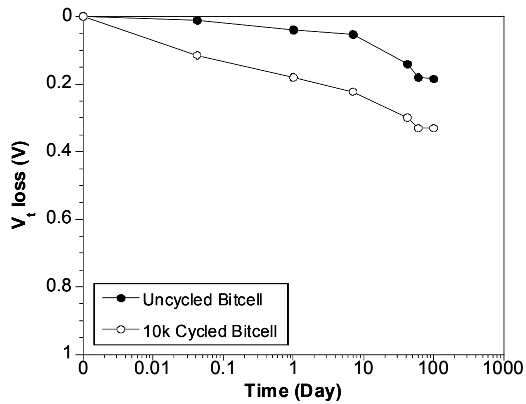

Figure 5: Effect of Cycling on 150°C Retention

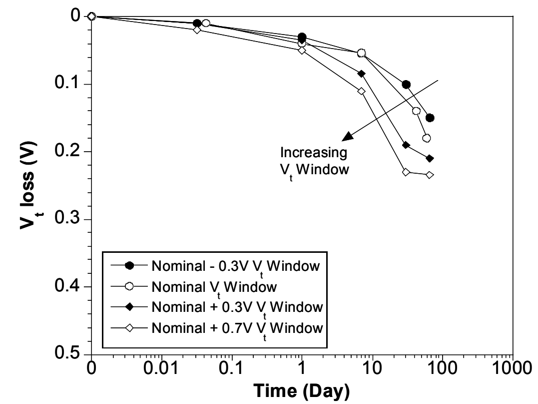

Figure 6: Effect of V_t Window on 150°C Retention

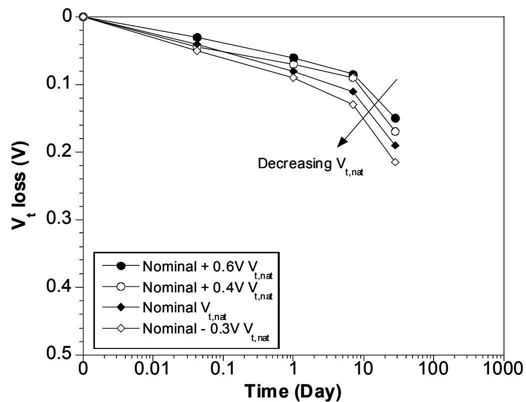

Figure 7: Effect of Natural V_t on 150°C Retention

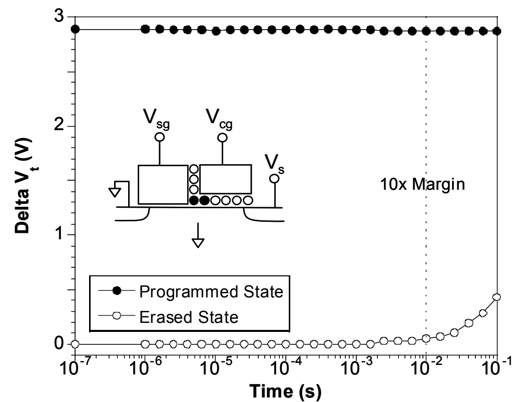

Figure 8: Program Disturb