Uniaxial-Biaxial Stress Hybridization For Super-Critical Strained-Si Directly On Insulator (SC-SSOI) PMOS With Different Channel Orientations.

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Abstract

This paper describes the novel stress engineering of SC-SSOI devices through the interactions between biaxial lattice strain, uniaxial relaxation, process-induced stressor and channel orientation. We have demonstrated a method of uniaxial stress relaxation with compressive capping layer (cESL) to achieve the desired stress configurations for enhanced short-channel SC-SSOI pMOS devices.

Introduction

Superior isolation with efficient leakage and parasitic capacitance control has enabled partially-depleted (PD) SOI devices to achieve high performance with strict power budgets, demanded by embedded microprocessor applications [1]. Building upon the PD-SOI device architecture, SC-SSOI devices and circuits with performance enhancement through strong wafer-level biaxial strain were demonstrated recently [2]. In addition, a strong positive impact of biaxial strain on gate leakage reduction, with no performance penalty, was observed [2]. This promises new options for circuit standby leakage reduction, especially when gate-dielectric scaling becomes limited.

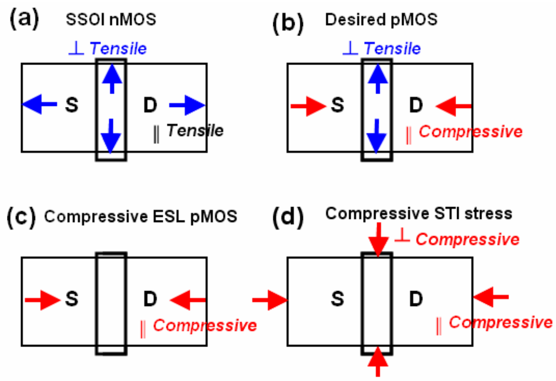

Fig.1 Schematic showing various stress configuration and their associated stressors.

The advantages of wafer-level biaxial strain versus localized uniaxial stress have generated much discussion [3]. Despite of the debate, recent wafer bending experiments have shown that biaxial strain produces greater electron mobility enhancement than equivalent uniaxial stressors [4]. However, the fundamentally weak pMOS enhancement will pose scaling difficulties for biaxial stressors in high-performance CMOS. In this paper we investigate a novel in-plane stress engineering approach to achieve the desired pMOS stress configuration (Fig. 1), which will otherwise be difficult for pure uniaxial or biaxial stressors to accomplish. The interactions between the hybridized biaxial-uniaxial stresses and channel directions will also be discussed.

CMOS Stress Configuration

Although biaxial tension can produce modest hole mobility enhancement at low vertical effective fields, channel carrier subband splitting due to biaxial stress and its associated effective mass change [5] lead to an undesired enhancement sensitivity to the vertical effective field (Fig. 2). The hole mobility enhancement under high effective gate fields is diminished and becomes negative when the fields are high (>1.1MV/cm). Piezoresistance coefficients show that once the undesired tension along the channel is reversed strong pMOS enhancement should result. Moreover, the transverse tension along W should be preserved for pMOS performance [6].

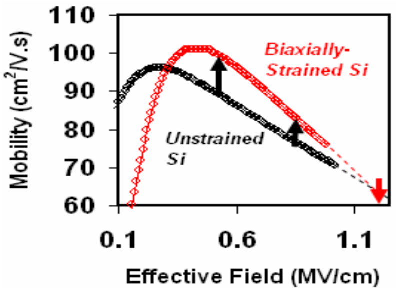

Fig. 2 Long-channel hole mobility showing the strong sensitivity of the biaxially-strained Si enhancement as a function of effective vertical field.

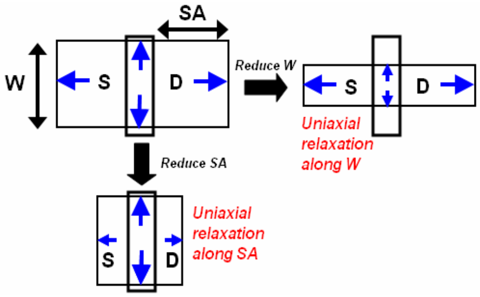

Fig. 3 Schematics illustrating the uniaxial relaxation of the SSOI biaxial stress components as a function of active Si pattern and layout. SA is defined as the gate to isolation distance along the channel direction.

SC-SSOI Uniaxial Relaxation

The wafer-level strain of un-patterned SSOI wafers is robust even when strained-Si critical thickness is dramatically exceeded [2]. However, small isolated islands of strained Si become susceptible to stress relaxation. The relaxation process is sensitive to the island dimensions and the process conditions. Here we show that the relaxation can occur along specific directions, leading to uniaxial relaxation of the intrinsic biaxial stress (Fig. 3).

A dramatic demonstration of uniaxial relaxation occurs when the widths of pMOS SC-SSOI are reduced causing the stress along the W-direction to relax. A similar approach applied to biaxially-compressed SGOI was recently reported [7]. Figure 4 compares the performance of <110>- and <100>- oriented SC-SSOI short-channel pMOS and <100>-directed SOI devices. The biaxial stress produces a mild 5% degradation for both the <110> and <100> channel pMOS devices, when the device widths are large (W=1µm). However, when the widths are reduced to 120nm, we observed that the <100> SC-SSOI device no longer experiences any degradation while the <110> device degradation has increased to 40% (Fig. 5). Since the <100> p-channel is insensitive to uniaxial stresses directed parallel/normal to the channel, the residual SA-directed tension has little or no impact on its device performance (Fig. 6). On the other hand, the SA tension impacts the <110> p-channel even more severely without the beneficial transverse tension, removed during uniaxial relaxation (Fig. 6).

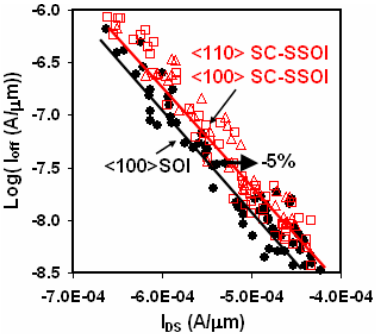

Fig. 4 pMOS Idsat degradation due to biaxial tensile strain for <110>- and <100>- short channel SSOI pMOS (W=1µm).

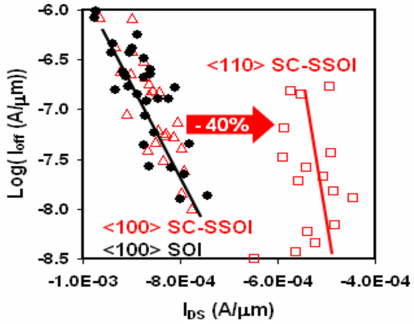

Fig. 5 Dramatic difference in short <110>- and <100>-channel SC-SSOI pMOS devices after experiencing uniaxial stress relaxation along the narrow widths (W=120nm)

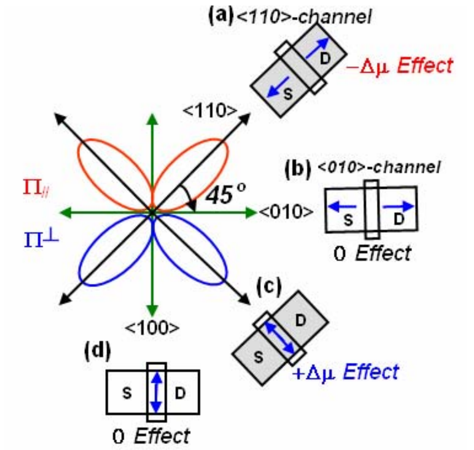

Fig. 6 p-Si (100) piezoresistance coefficients for tensile stress as a function of channel orientation after [8].

SC-SSOI & Uniaxial Stressor

To enhance the <110>-oriented SC-SSOI pMOS devices, we apply a uniaxial stressor. Figure 7 is a TEM cross section of a 28nm gate SC-SSOI pMOS device with a compressive capping layer that induces compressive stresses along the SA direction. Channel resistance data, which separates the short-channel mobility and S/D resistance influences, reveals that pure SC-SSOI biaxial stress increased the p-channel resistance by 17% while the cESL stressor reduces it by 27% and the biaxial-uniaxial effects appear to be additive. Since the cESL stressor had to recover the degradation, it was only effective in providing a net 10% improvement over unstrained Si. IDsat data show less enhancement for both SC-SSOI and SOI, possibly due to high-field mobility degradation (Fig. 9). Nevertheless, the reduced effectiveness of the cESL in the presence of strong SA-directed tension is still evident. A similar observation showing the reduced impact of the capping layer stressor when it is coupled to strong biaxial stress was also reported for SGOI devices [9].

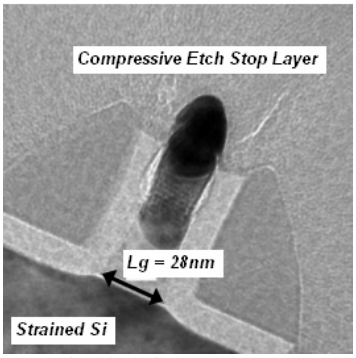

Fig. 7 TEM cross-section depicting a 28nm gate SC-SSOI pMOS transistor with compressive ESL.

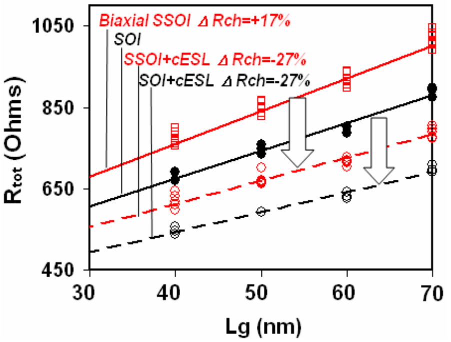

Fig. 8 pMOS total resistance versus Lg showing the channel resistance change as a function of biaxial and uniaxial stressors

To take full advantage of the cESL compression, the SA-directed tension will need to be weakened or removed through uniaxial relaxation. Figure 10 shows the impact of relaxing the undesired SC-SSOI tension through SA-reduction. Now the SC-SSOI and the SOI pMOS devices are identically enhanced and the cESL effectiveness is no longer compromised (Fig. 10).

Figure 11 describes the interactions between the intrinsic biaxial stress and the process-induced stresses. Under wide width and large SA conditions (point C), only 5% enhancement with respect to unstrained Si is attained. Due to uniaxial relaxation, SC-SSOI+cESL display a much stronger sensitivity to SA then the SOI+cESL devices. As SA is reduced (points C to E), the SC-SSOI enhancement improves dramatically with the weakening of the undesired SA tension. Finally at the smallest

SA, we match the cESL enhancement for SC-SSOI and SOI. Comparison between the wide- and narrow-width SOI devices reveals the negative influence of compressive STI stresses in the W-direction. In both cases the SA-sensitivity is hardly affected but the enhancement for the narrow-width SOI devices are reduced due to the presence of compressive STI stresses along W (points A-E,B-G). The role of the transverse (W-directed) tension (absent in SOI) is highlighted in the dramatic SA sensitivity change for the narrow-width SC-SSOI devices. As W is reduced, the beneficial transverse tension is also uniaxially reduced. In the presence of the W-directed STI compression, SA-reduction alone was insufficient to overcome the degradation, leading to points D to F. In contrast to the wide width devices, the narrow-width transistors also exhibit a much larger difference in SA behavior between the SOI and SC-SSOI devices due to the interaction of W-directed relaxation and the compressive STI stresses. At the smallest SA, the cESL enhancements for SOI and SC-SSOI for narrow width transistors (point G) are still matched.

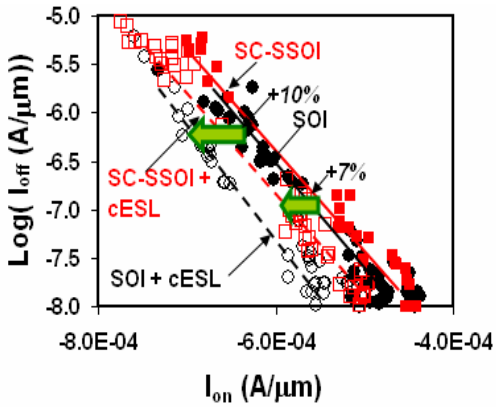

Fig. 9 SOI and SC-SSOI pMOS IDsat performance with cESL (SA=3µm).

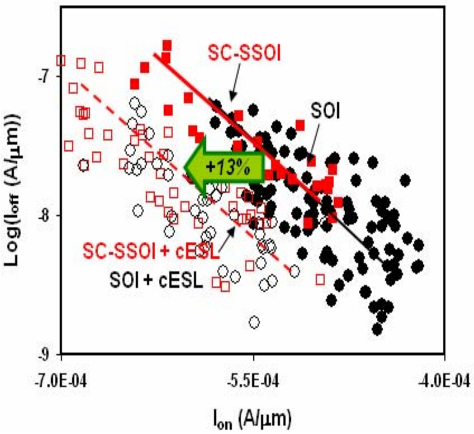

Fig. 10 SC-SSOI pMOS performance after SA-uniaxial relaxation and the impact of cESL (small SA).

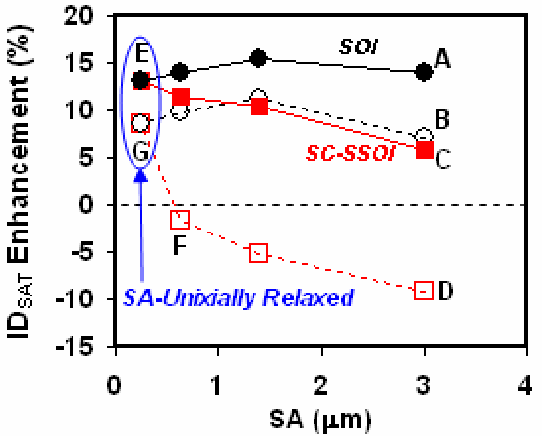

Fig. 11 Idsat enhancement of SOI and SSOI with cESL as a function of SA. Solid symbols: W=1µm devices. Open symbols: 0.22µm devices. Circle symbols: SOI, Square symbols: SC-SSOI.

<110> Vs <100> channel SC-SSOI pMOS

Figures 12 and 13 show the performance differences between the <110> SC-SSOI, SOI and the <100> SC-SSOI when the SA is substantially reduced. Since the <100> p-channel is insensitive to uniaxial stresses directed parallel/normal to the channel, uniaxial relaxation of the SA-tension are not expected to impact device performance. By the same argument, the <100> p-channel cannot benefit from the compressive STI stresses directed along the SA. Figure 14 charts the IDsat enhancement as a function of SA and width for the two channel orientations. Influenced by the biaxial stress, the wide width (W=1µm) transistors show little difference in SA behavior between the <110> and the <100> channels, except at the smallest SA dimension, where biaxial stress reduces to uniaxial. However, when the transistor width is reduced to 0.22µm, the advantage of the <100> channel SC-SSOI is evident. Insensitive to the negative STI compressive stresses, the <100> p-channel exhibits a 10% average IDsat improvement over <110> SOI devices. <110> SC-SSOI and SOI are both negatively impacted by the W-directed STI compression, but the <110> SC-SSOI experiences further degradation due to the tension along the SA, except for the smallest SA dimension (Fig. 14).

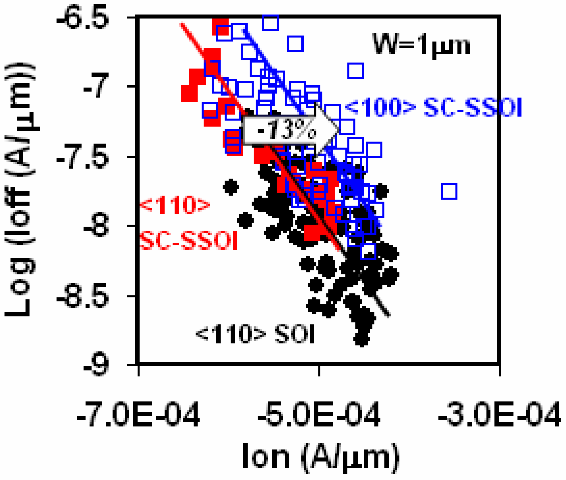

Fig. 12 pMOS performance difference for <110> and <100> channel SSOI for wide width devices with smallest SA.

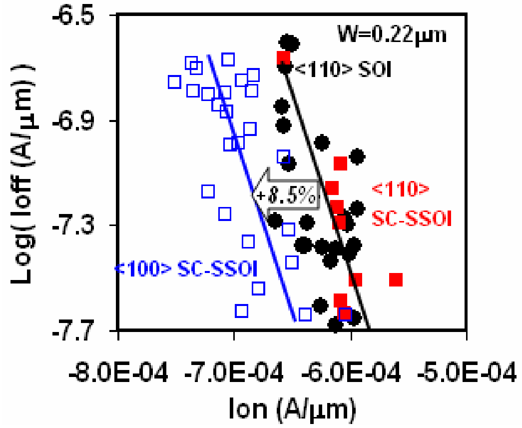

Fig. 13 pMOS performance for narrow width and smallest SA devices.

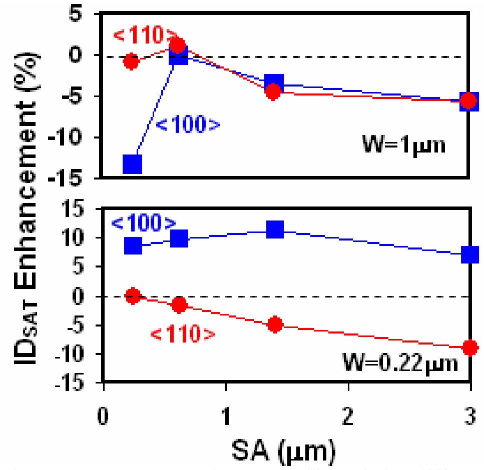

Fig. 14 pMOS IDsat enhancement/degradation differences between <110> and <100> SSOI.

Conclusions

The weak or negative pMOS enhancement poses fundamental scaling issues for substrate-level biaxial tensile strain. Uniaxially relaxing SC-SSOI and biaxial-uniaxial stress hybridization provide an effective solution. In this work we have demonstrated a novel in-plane stress engineering approach that achieved the desired SC-SSOI pMOS stress configurations through selected lay-out changes and the application of a compressive capping layer. With SA-directed uniaxial relaxation, the full benefit of the uniaxial stressor on <110> SC-SSOI pMOS devices can be realized. In contrasts, <100>-oriented SC-SSOI pMOS exhibits a desired immunity to the negative STI stresses but it is limited in its potential to improve with unixial stressors.

Acknowledgements

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