Energy Limits in Current A/D Converter Architectures

Driven by ever-increasing application demands, the energy expended per A/D conversion has been reduced substantially over the last decade.
This presentation will survey the most recent trends and will investigate energy limits as they apply to A/D converter architectures commonly employed in fine-line CMOS technology (Flash, Pipeline, SAR and Oversampling Converters). Through this analysis, opportunities for further improvements will be identified and discussed in detail, specifically emphasizing the impact of technology scaling.

BIO: Boris Murmann is an Associate Professor in the Department of Electrical Engineering, Stanford, CA. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 2003. From 1994 to 1997, he was with Neutron Mikrolektronik, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. Dr. Murmann's research interests are in the area of mixed-signal integrated circuit design, with special emphasis on data converters and sensor interfaces. In 2008, he was a co-recipient of the Best Student Paper Award at the VLSI Circuits Symposium in 2008 and a recipient of the Best Invited Paper Award at the IEEE Custom Integrated Circuits Conference (CICC). He received the Agilent Early Career Professor Award in 2009 and the Friedrich Wilhelm Bessel Research Award in 2012.
He currently serves as an Associate Editor of the IEEE Journal of Solid-State Circuits, the Data Converter Subcommittee Chair of the IEEE International Solid-State Circuits Conference (ISSCC) and as a program committee member of the European Solid-State Circuits Conference (ESSCIRC). He is a Distinguished Lecturer and elected AdCom member of the IEEE Solid-State Circuits Society.