VLSI Architectures for Communications and Signal Processing

Part 1 of this lecture covers introduction to VLSI architectures for Communications and Signal Processing Systems. Various topics include pipelining and parallel processing, retiming, unfolding, folding, systolic architecture design and algorithmic transformations. The emphasis is how to design high-speed, low-area, and low-power VLSI systems for a broad range of DSP and communication applications.

Part 2 of this lecture covers speaker's research. Low-Density Parity-Check codes now have been firmly established as coding technique for communication and storage channels. This talk gives an overview of the speaker's research and contributions in the development of low complexity iterative LDPC solutions for Turbo Equalization for magnetic recording storage channels. Complexity is reduced by developing new or modified algorithms and new hardware architectures viz. system level hardware architecture, statistical buffer management and queuing, local-global interleaver, LDPC decoder and error floor mitigation schemes.

Speaker's Bio

Kiran Gunnam received the MSEE and PhD in Computer Engineering from Texas A&M University, College Station, TX. He currently works as Director of Engineering at Violin Memory. He previously held research and development positions at Nvidia, Certicom, LSI, Marvell Semiconductor, Starvision Technologies, Schlumberger, Intel and Texas Engineering Experiment Station.

Dr. Gunnam has extensive research and development work experience in complex data path and control path systems. Dr. Gunnam is an expert in IC implementation of communications and signal processing systems. His PhD research contributed several key innovations in advanced error correction systems based on low-density parity- check codes (LDPC) and led to several industry designs. He has done extensive work on ASIC hardware architecture, micro-architecture and digital IC implementation for different systems (IEEE 802.11n Wi-Fi, IEEE 802.16e WiMax, IEEE 802.3 10-GB, Holographic read channel, HDD read channel and Flash read channel).

Dr. Gunnam has around 75 patents/patent applications/invention disclosures on hardware architecture and micro-architecture (33 issued patents, 17 pending patent applications and 25 more invention disclosures). He is the lead inventor/sole inventor for 90% of them. He is an IEEE Senior Member. He is also an IEEE Solid State Circuits Society Distinguished Lecturer for 2013 and 2014.