Fundamentals of Sigma-Delta ADCs

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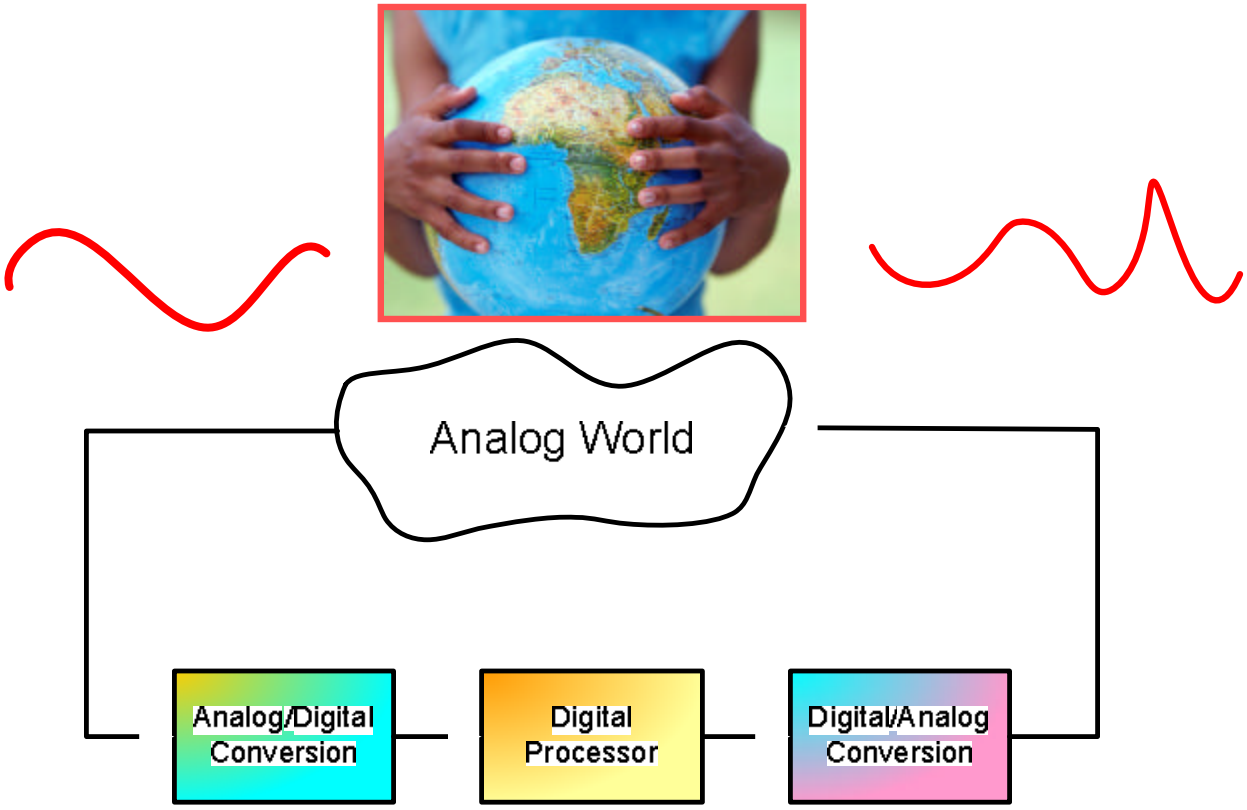
Why Analog to Digital Conversion?



- ✓ Naturally occurring signals are analog signal
- ✓ Human beings perceive and retain information in analog form
- ✓ BUT, Analog signal is more sensitive to noise than digital signal

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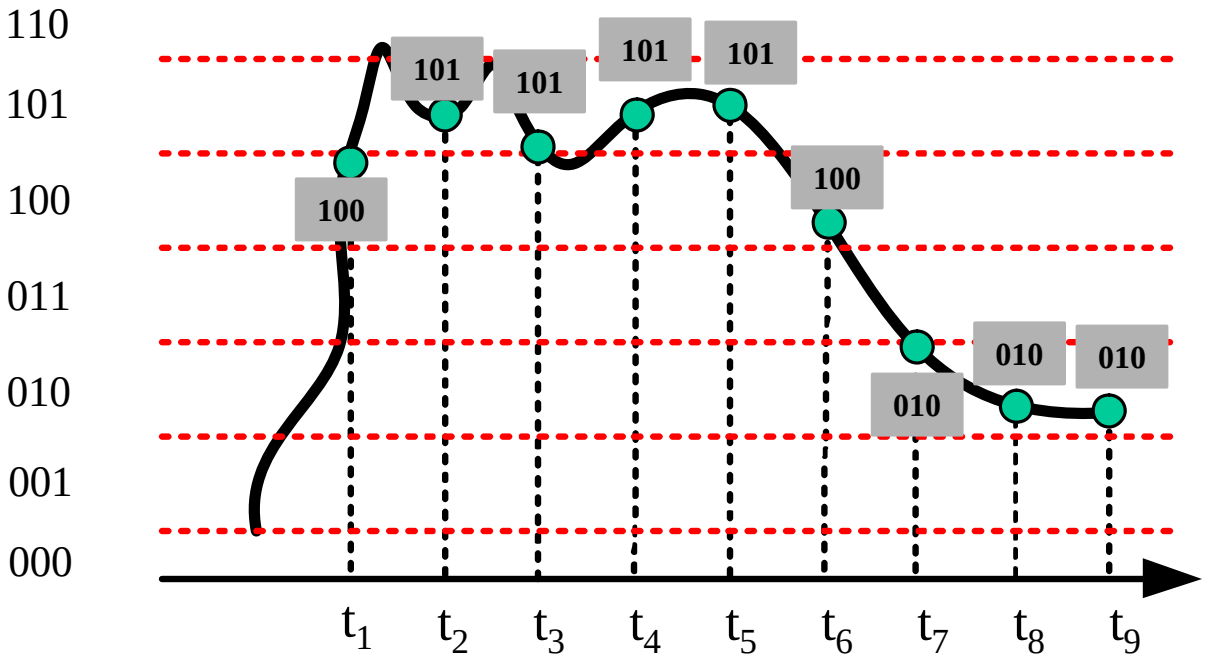
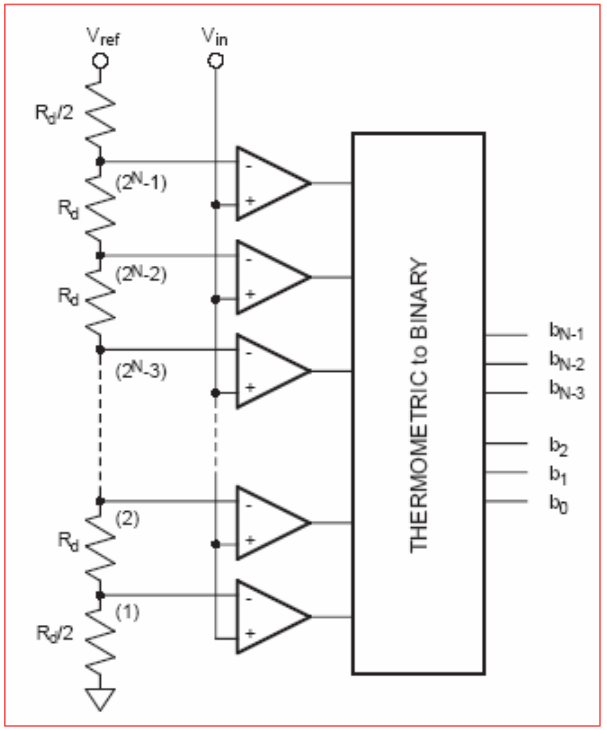
How Analog to Digital Conversion?





1. Sample analog signal
2. Quantize sampled analog signal→ Quantization noise
3. Faster sampling time, better accuracy
4. Higher quantization levels, better accuracy

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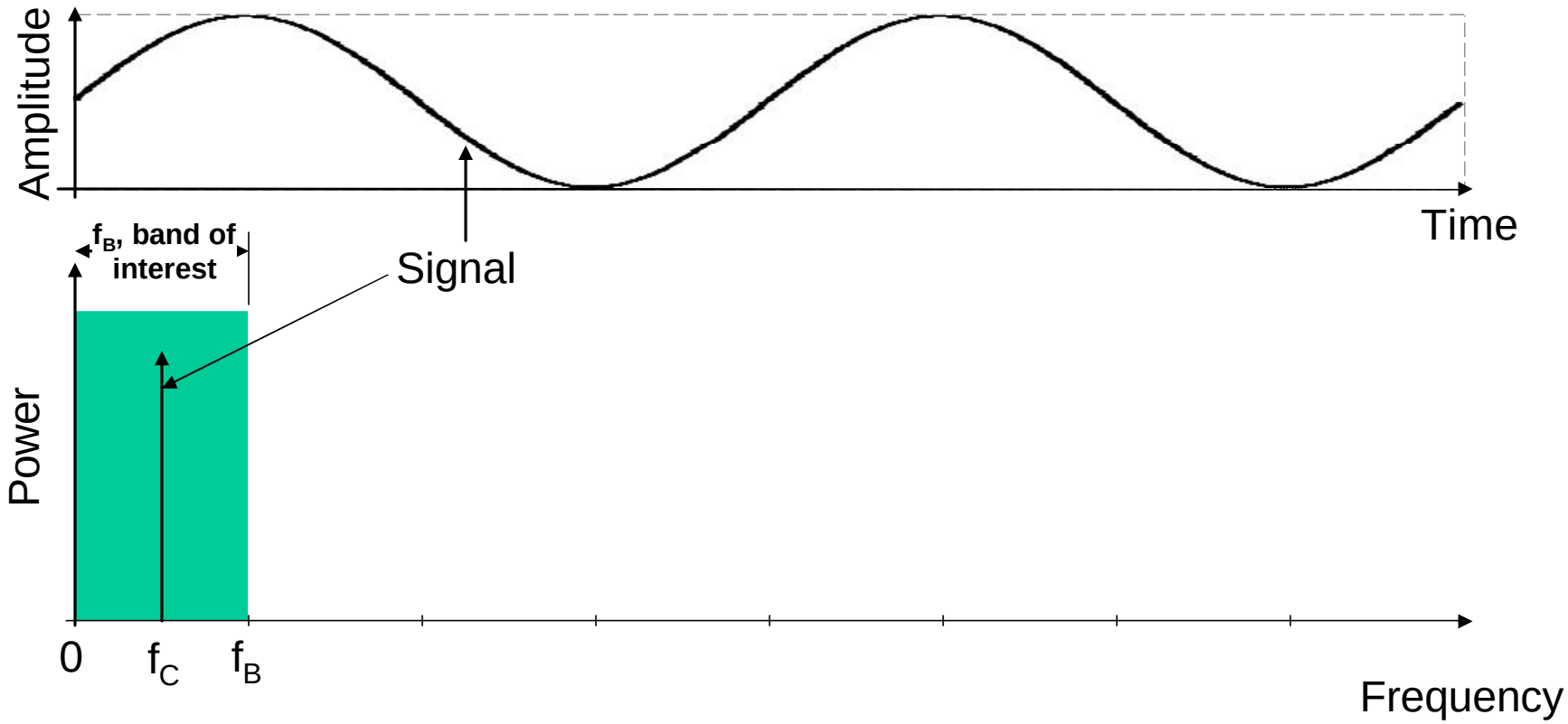
Continuous Time Signal



Signal frequency, f_C = band of interest, f_B (Maximum frequency of the signal)

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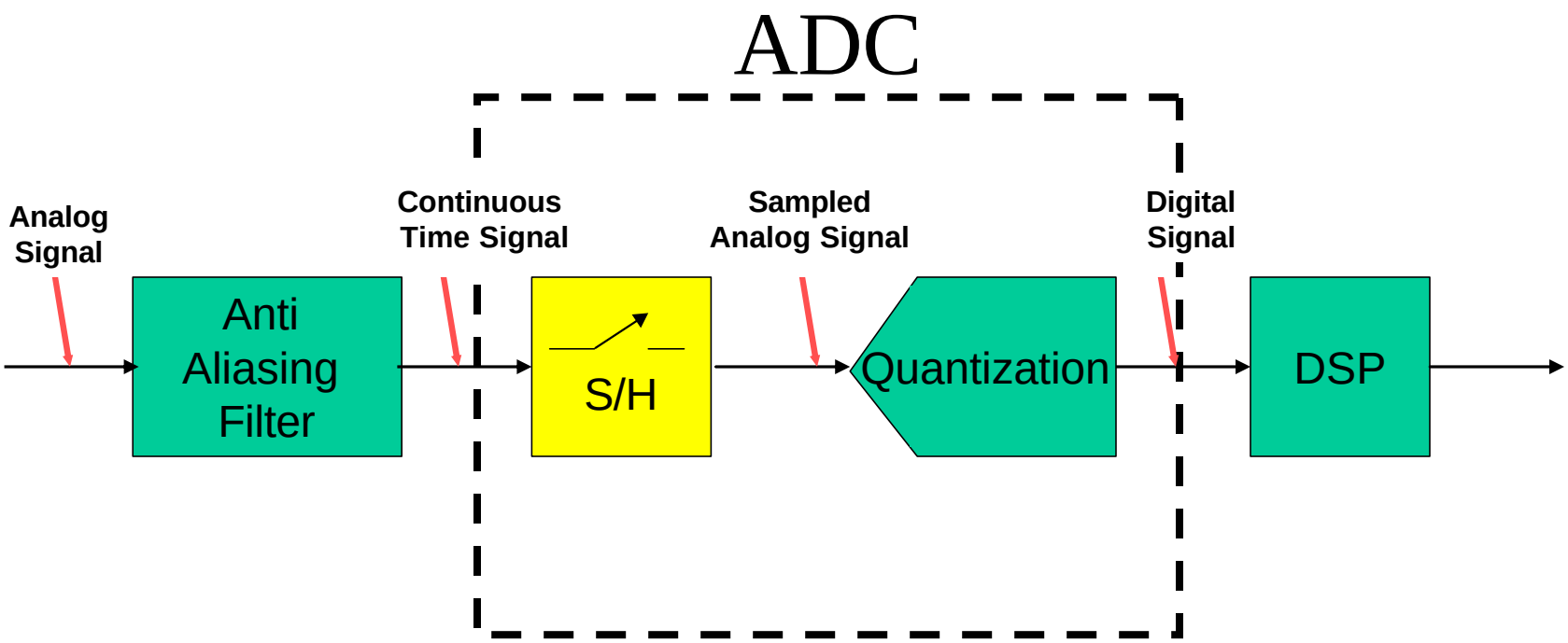
Typical Architecture for Analog to Digital Conversion



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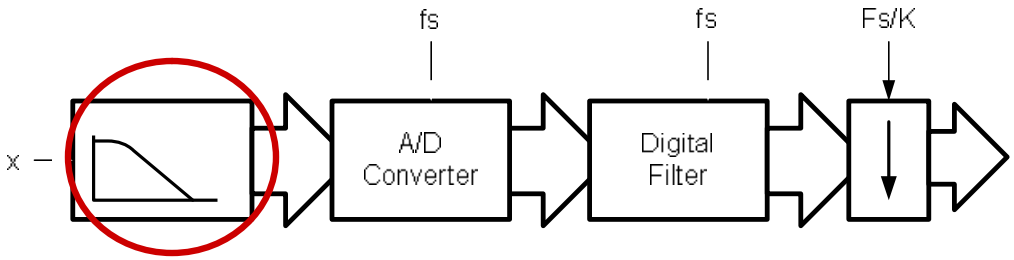
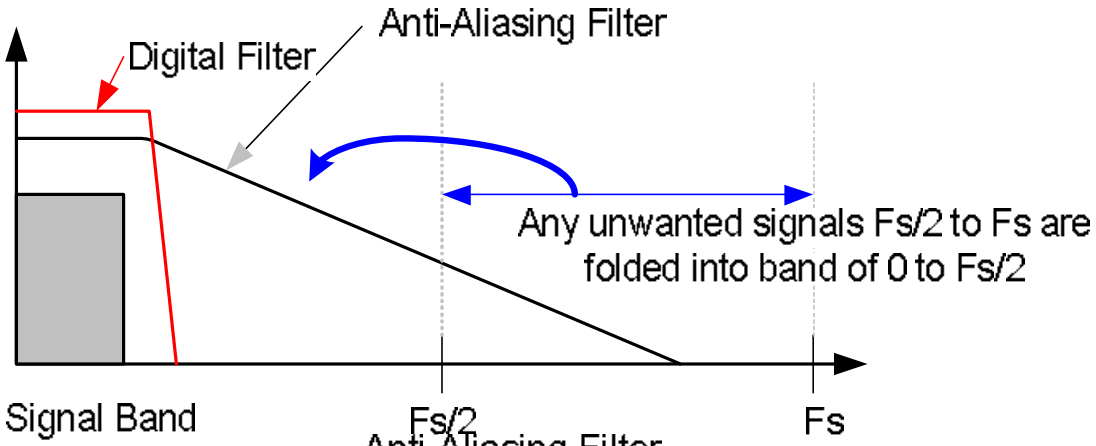
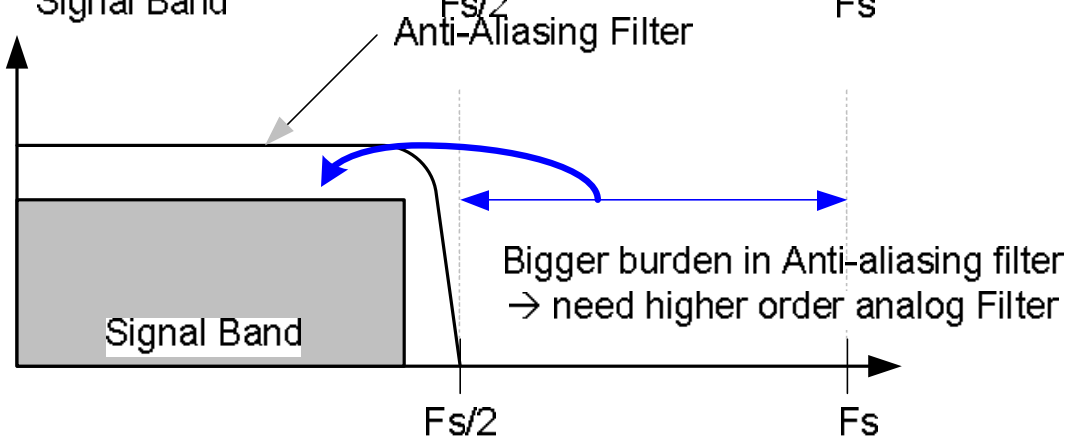
Nyquist Rate vs. Oversampled







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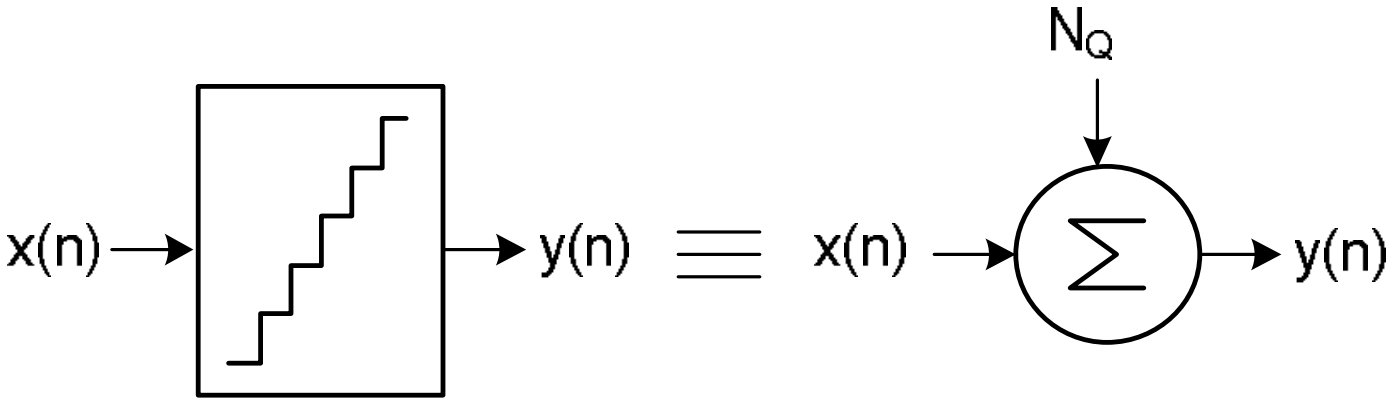
Modeling of Quantizer



- **Quantizer is non-linear building block**
  - Need modeling for simplifying the analysis
- **White additive noise assumptions**
  - It is not fulfilled in many applications, However
  - It makes analysis easy and makes possible the use of z-tansformation

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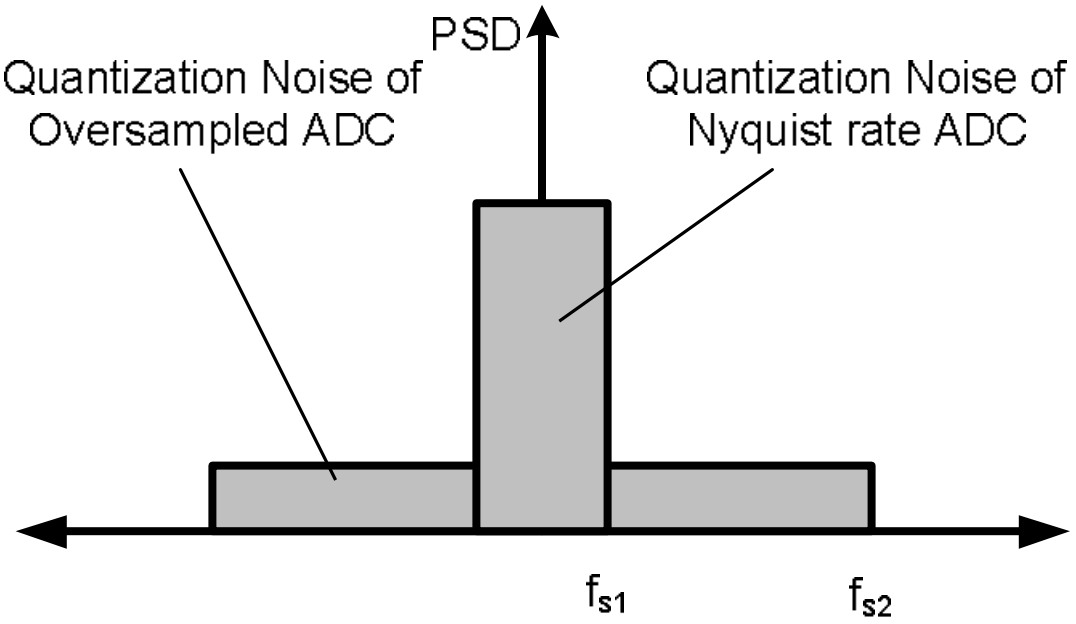
Quantization Noise



- **Quantity of in-band noise depends on the over-sampling ratio**
  - SNR = $10\log(s_x^2) - 10\log(s_n^2) + 3.01r$(dB), where
  - s_x^2 and s_n^2 are input signal power and in-band noise power respectively, and
  - r is defined by over-sampling ratio, $f_s/2f_b=2^r$

Pervez M. Aziz, "An overview of sigma-delta converters," IEEE Signal processing Magazine, pp 61-84, Jan. 1996

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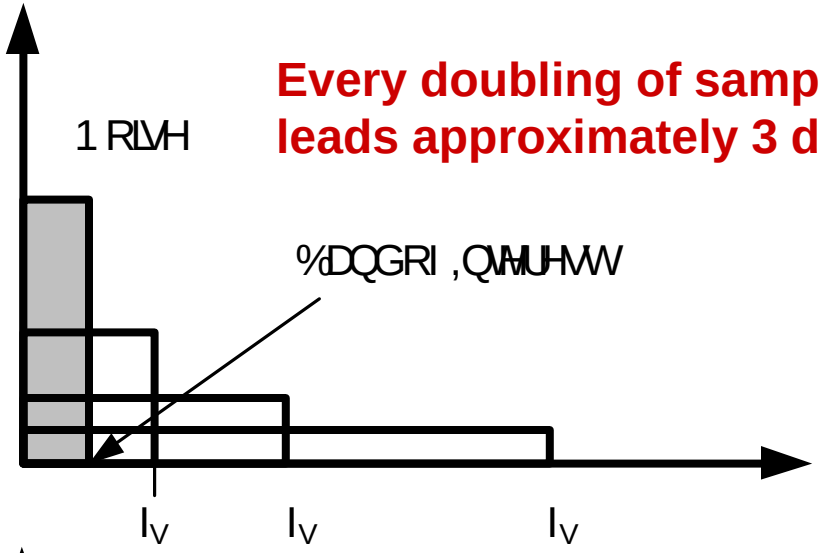
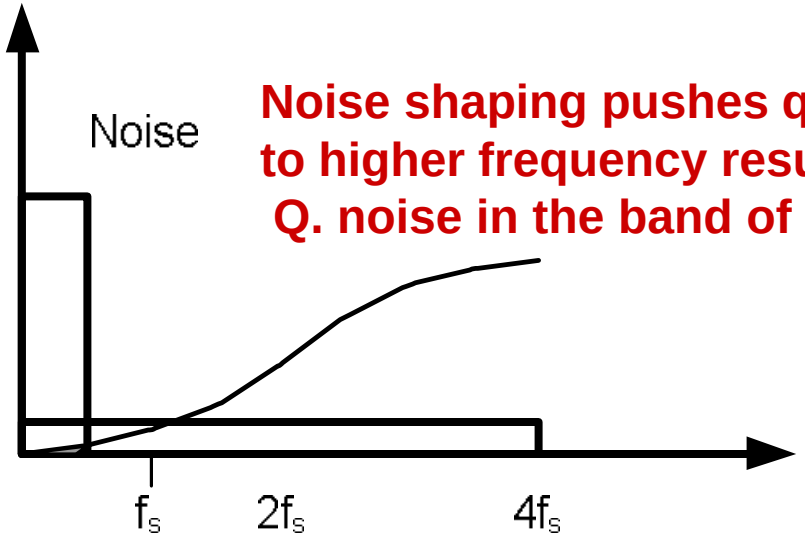
Over-sampling and Noise Shaping



Every doubling of sampling frequency leads approximately 3 dB enhancement in SNR



Noise shaping pushes quantization noise to higher frequency resulting in suppressing Q. noise in the band of interest

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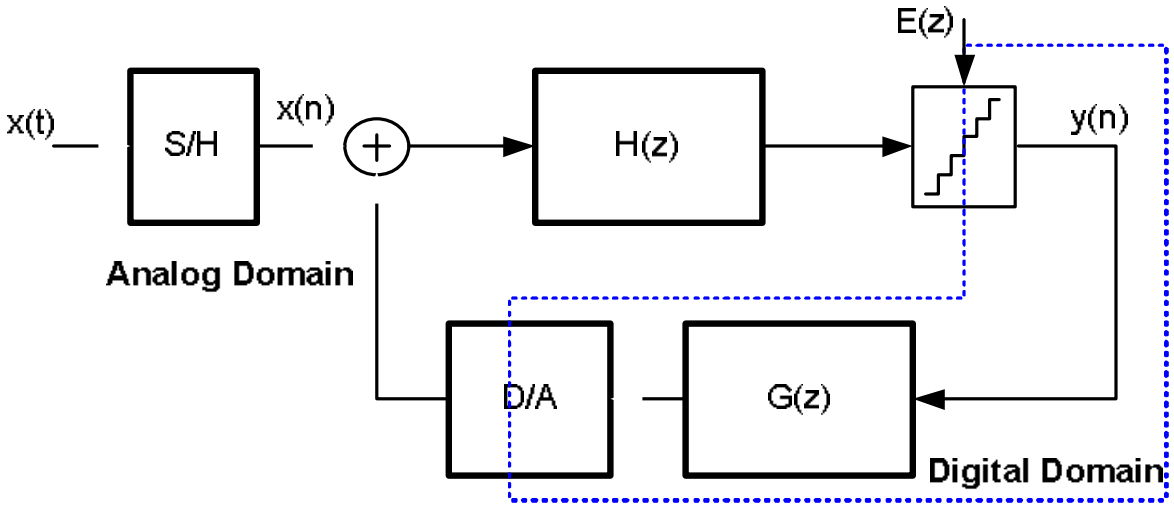
How to Shape the noise?



$$Y(z) = \underbrace{\frac{H(z)}{1+H(z)G(z)}}_{STF} X(z) + \underbrace{\frac{1}{1+H(z)G(z)}}_{NTF} E(z)$$

If $H(z) = z^{-1}/1-z^{-1}$ and $G(z)=1$, NTF and STF will be:

$$NTF = \frac{Y(z)}{E(z)} = 1 - Z^{-1} \qquad STF = \frac{Y(z)}{X(z)} = Z^{-1}$$

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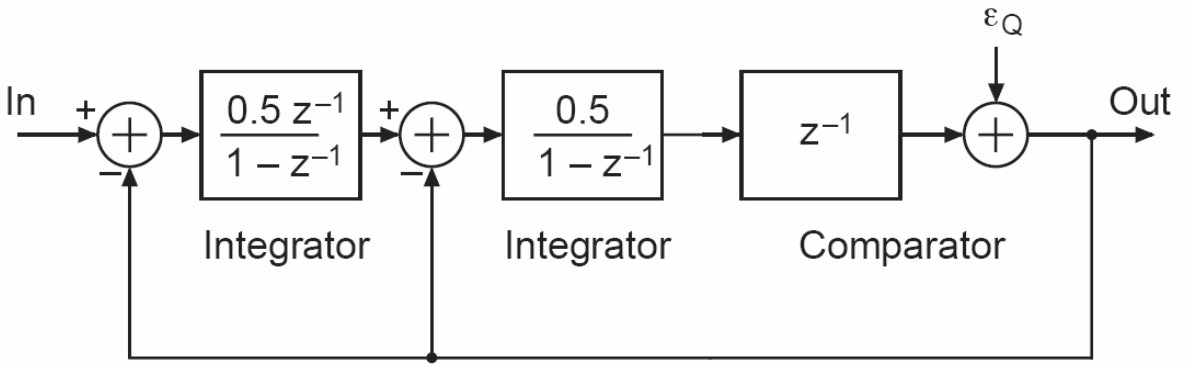
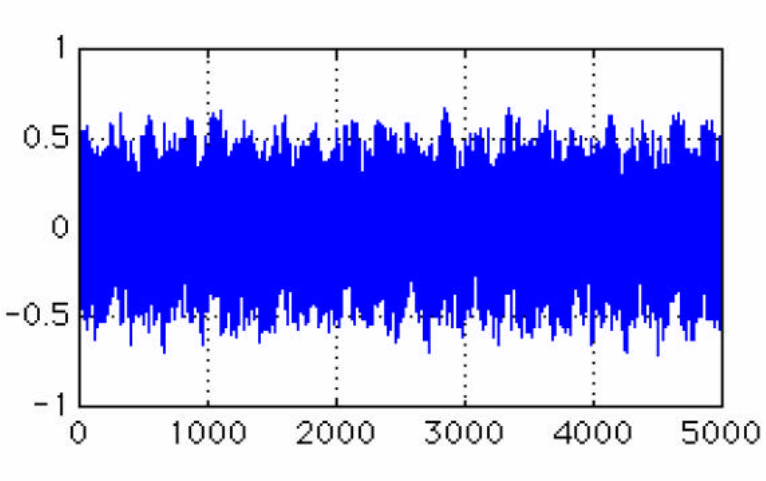
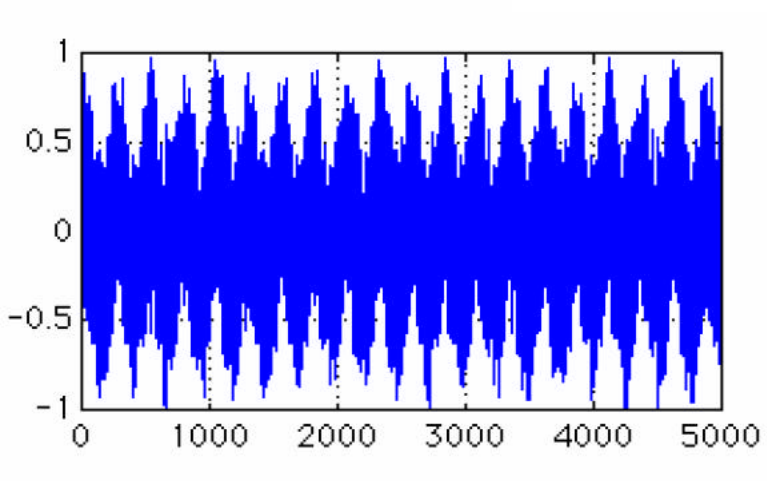
Example, 2nd order Sigma-Delta ADC





Output of the 1st integrator



Output of the 2nd integrator

- ✓ The dynamic range at the output of the two integrators is limited
- ✓ Input signal attenuation by 6 dB

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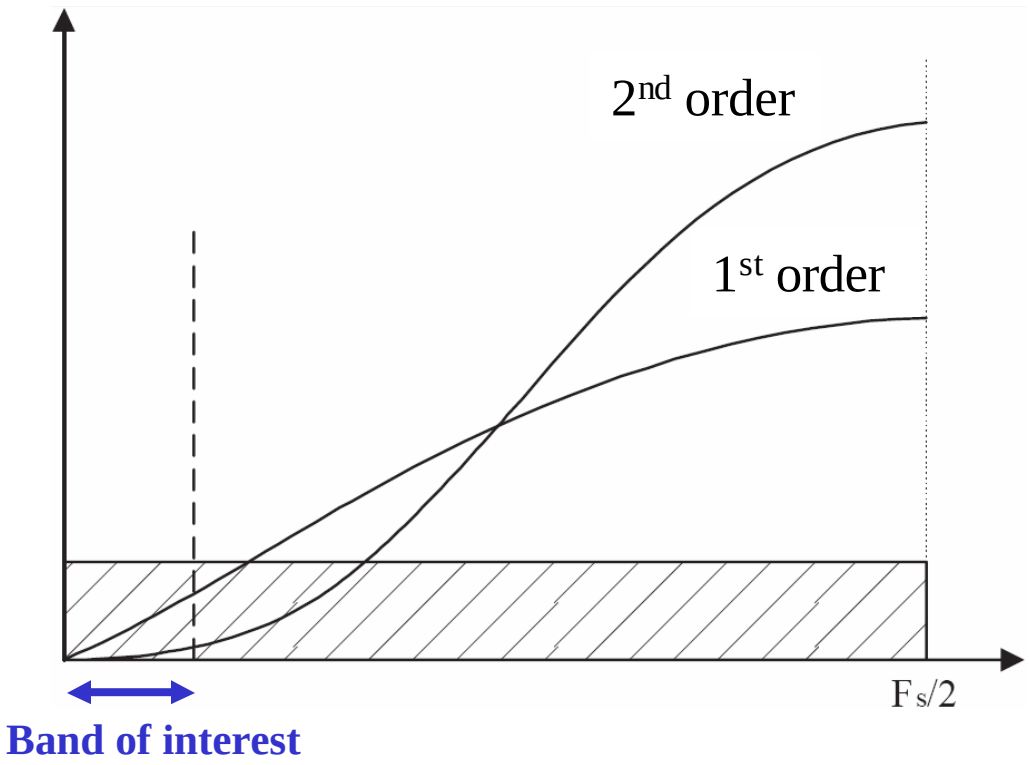
Noise Shaping



In-band quantization noise is suppressed more with 2nd order

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Single-bit or Multi-bit ? S

Single Bit

- **Feedback DAC inherently linear. So no HD distortion.**
- **Need a faster Amplifier**
- **Lower SQNR for a given modulator order**

Multi Bit

- **Gives higher SQNR**
- **Relaxed opamp specs due to smaller step size**
- **DAC non-linearity is a performance limit**
- **Require dynamic element matching**

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Summary

- **Sigma-delta ADC provide trade-offs between:**
  - **Power consumption,**
  - **Over-sampling ratio (*OSR*)**
  - **System performance (*SNR*)**
- **High OSR implies:**
  - **Lower number of quantization levels**
  - **Lower modulator order, but**
  - **More demanding settling requirements for the analog building blocks**

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A Sigma-Delta ADC with a built-in Anti-aliasing filter for Bluetooth receiver in 130 nm digital process

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Published in CICC2004

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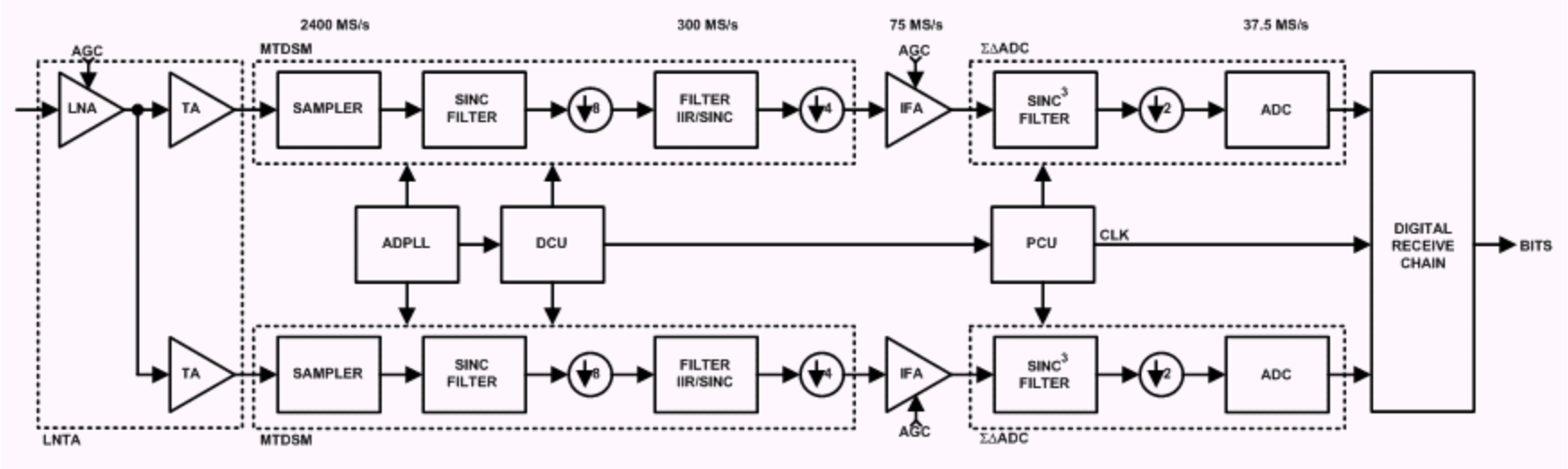
Introduction



- **RF input signal is amplified by two stage Amplifier, LNA and TA.**
- **TA output is down converted and filtered by Direct-Sampling Mixer (DSM).**
- **IFA amplifies mixer output signal operating at 75 Mhz.**
- **Sigma-Delta ADC converts 75 MHz IFA output to 37.5 MHz digital words.**

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ADC Requirements

- **60 dB Dynamic range at 1 Mhz signal bandwidth**
  - **2^{nd} order sigma-delta ADC**
  - **5 level quantizer**
  - **37.5 MHz sampling frequency.**
- **Gain Control**
  - **O dB and 14 dB gain option is required for system AGC function.**
- **Low Power consumption**
- **Low cost**

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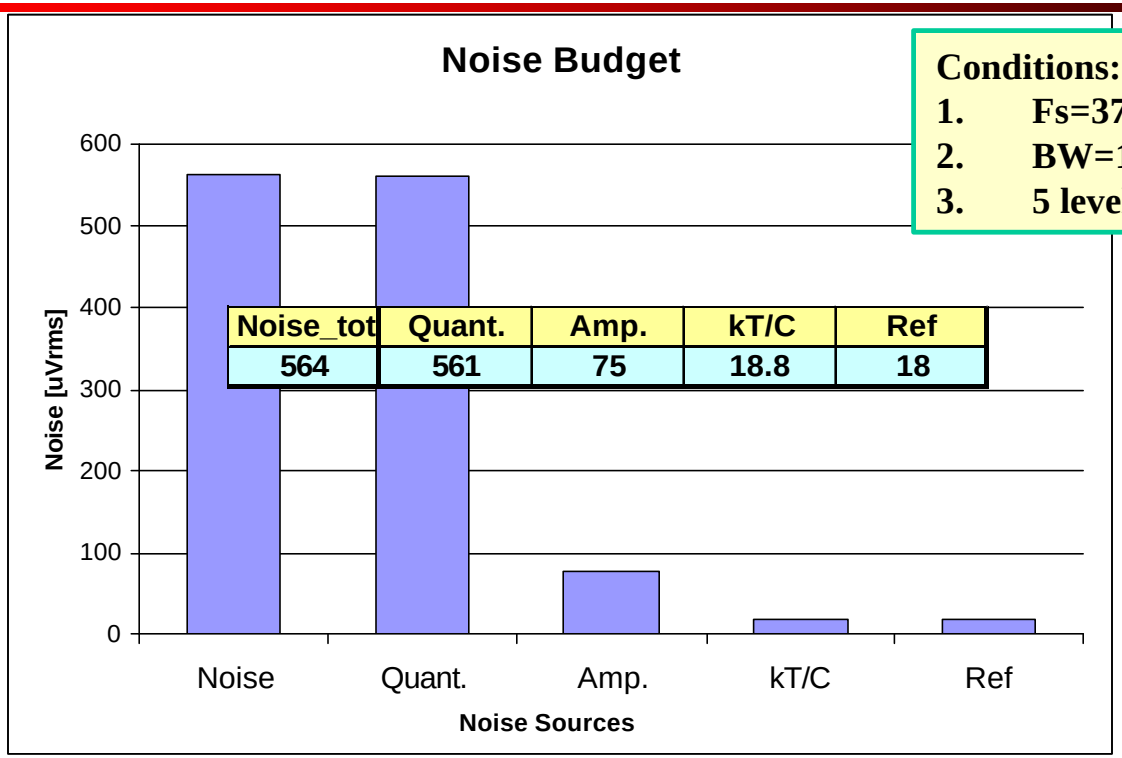
Noise budget



- **Quantization noise is a dominant noise source.**
  - **Unit capacitance element is selected based on considering mismatch effect.**
  - **Noises from amplifier and reference buffer are not critical.**
  - **Power consumption of amplifier is minimized since noise from it is negligible compared to the high in-band quantization noise.**

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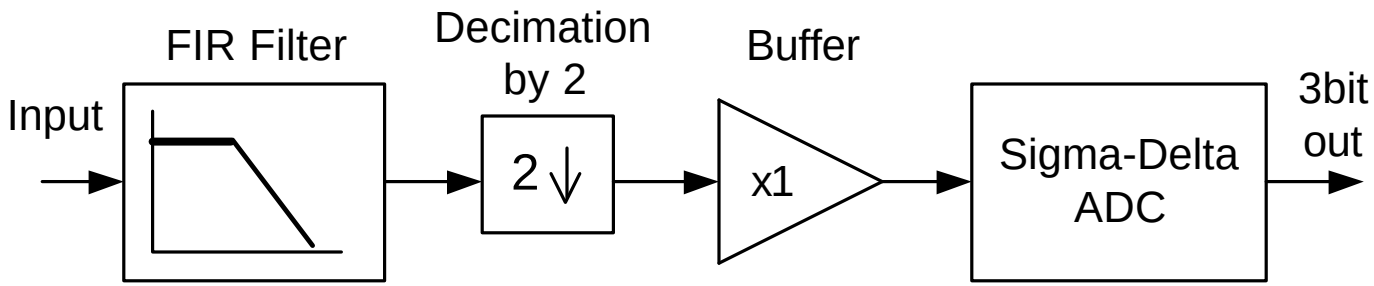
Required building blocks



- **Based on power consumption and noise analysis, following functions are required.**
  - **Decimation by Two: sampling frequency 37.5 MHz can provides enough Dynamic Range utilizing 5 level flash ADC.**
  - **Anti-alias filtering: Decimation by two function causes folding noise.**
  - **Buffering: buffer amplifier is required to avoid charge sharing between Switched capacitor FIR filter and sampling circuits in Sigma-Delta ADC.**

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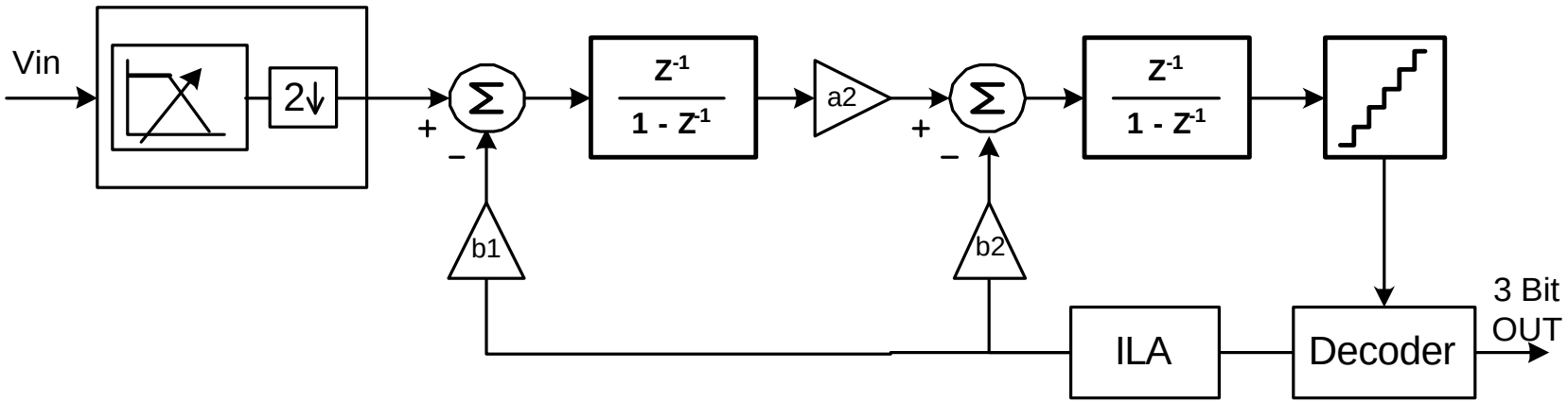
Proposed Architecture



- **Decimation, anti-aliasing filtering is merged with sampling circuits.**
  - **Saved power consumption and silicon area since it avoids the buffer.**
- **Second order Sigma-Delta ADC with 5 level flash.**
- **ILA DEM is used to suppress mismatch energy from DAC in feedback loop.**

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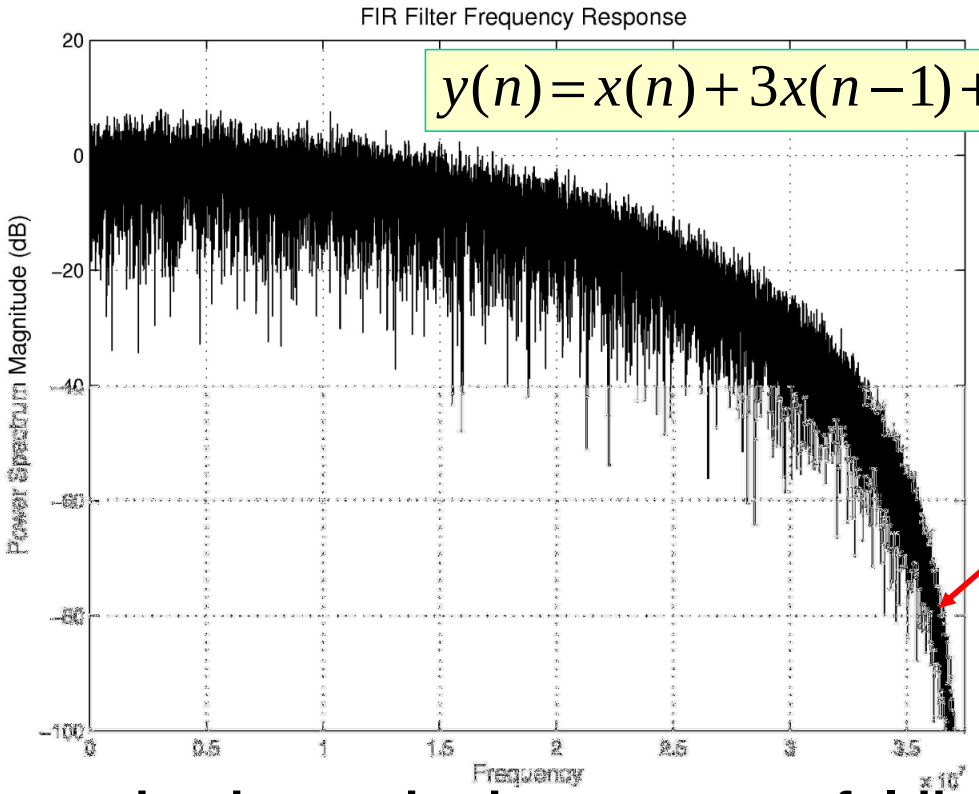
FIR Anti-aliasing Filter



$$y(n) = x(n) + 3x(n-1) + 3x(n-2) + x(n-3)$$

-80 dB at 36.5 MHz

- **60dB attenuation is required to suppress folding noise by system simulations.**
- **Third order FIR filter is chosen and provides 80 dB attenuation at folding frequency band edge.**

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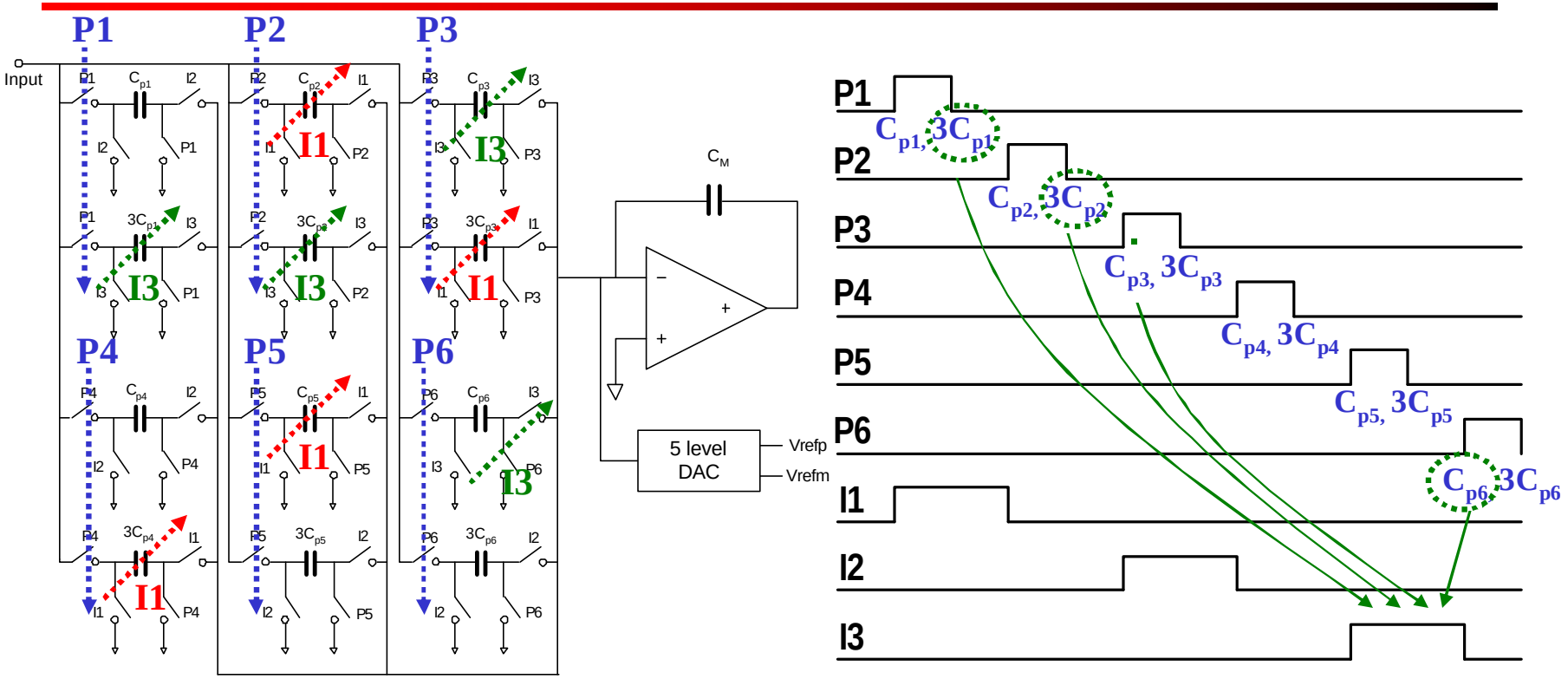
FIR Anti-aliasing Filter and Decimation



- 6 phase clock signals are utilized to implement FIR filter.
- On Pi phase, input is sampled at Cpi and 3Cpi capacitors,
- On I3 phase, Cp3, 3Cp2, 3Cp1 and Cp6 is dumped into integrating capacitor.

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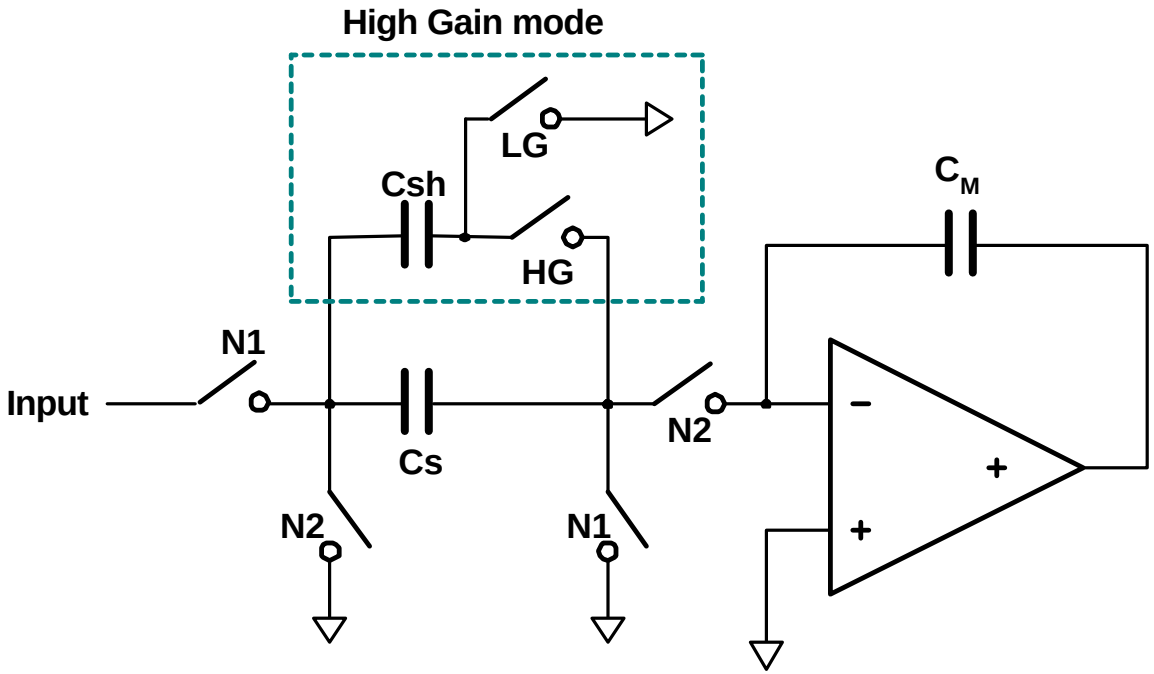
Gain control



- **Gain control function is implemented in FIR sampling block by adding the high gain mode switched capacitor circuits in parallel with each capacitor in SC FIR filter.**
- **Gain is defined by the ratio between sampling capacitors and integrating capacitor (C_M).**

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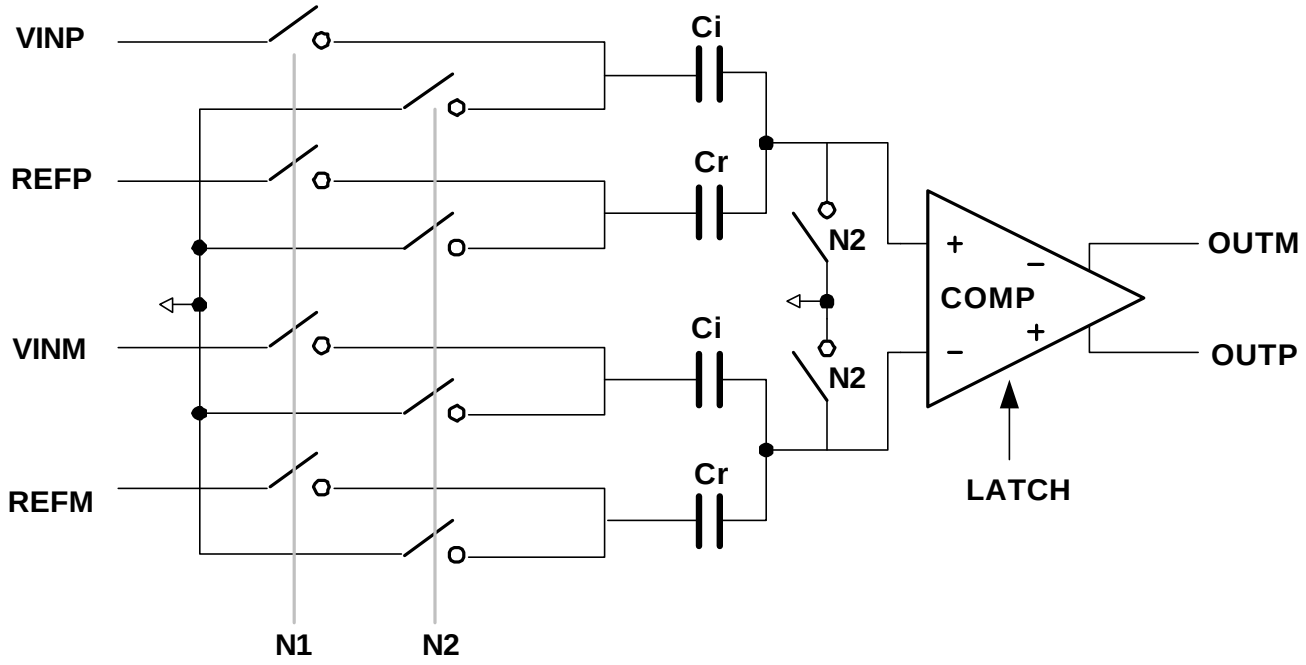
Comparator



- **Switched capacitor comparator is used to build 5 level quantizer.**
- **Capacitor ratio between C_i and C_r is chosen to have threshold voltage for each comparator.**
- **Capacitor size is optimized to be minimum considering decision speed, resolution (mismatch) and offset.**

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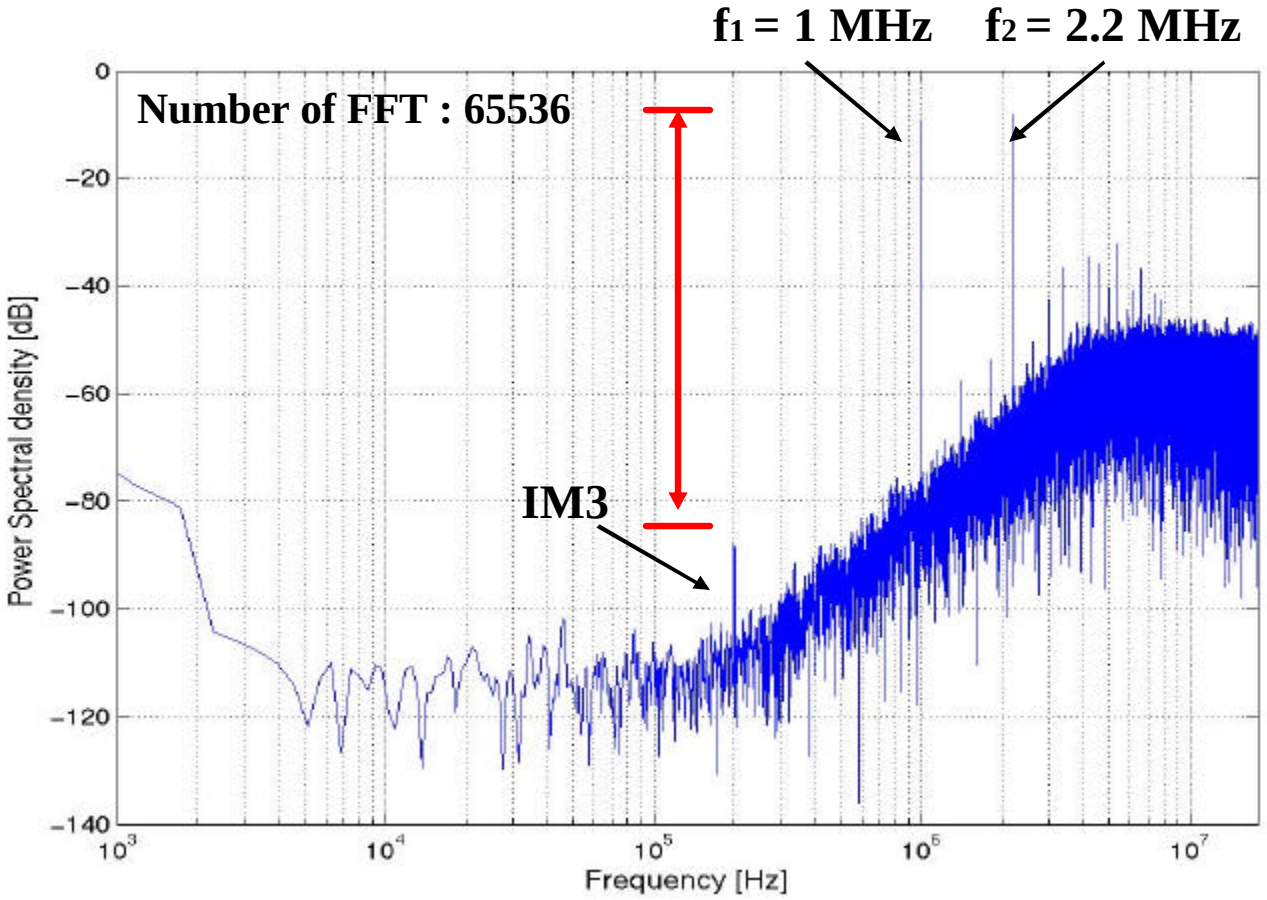
Two Tone Measurements



- -8 dBFS sine signals at 1 MHz (f1) and 2.2 MHz (f2) are applied.
- -80 dBc IM3 shows at 200 kHz.

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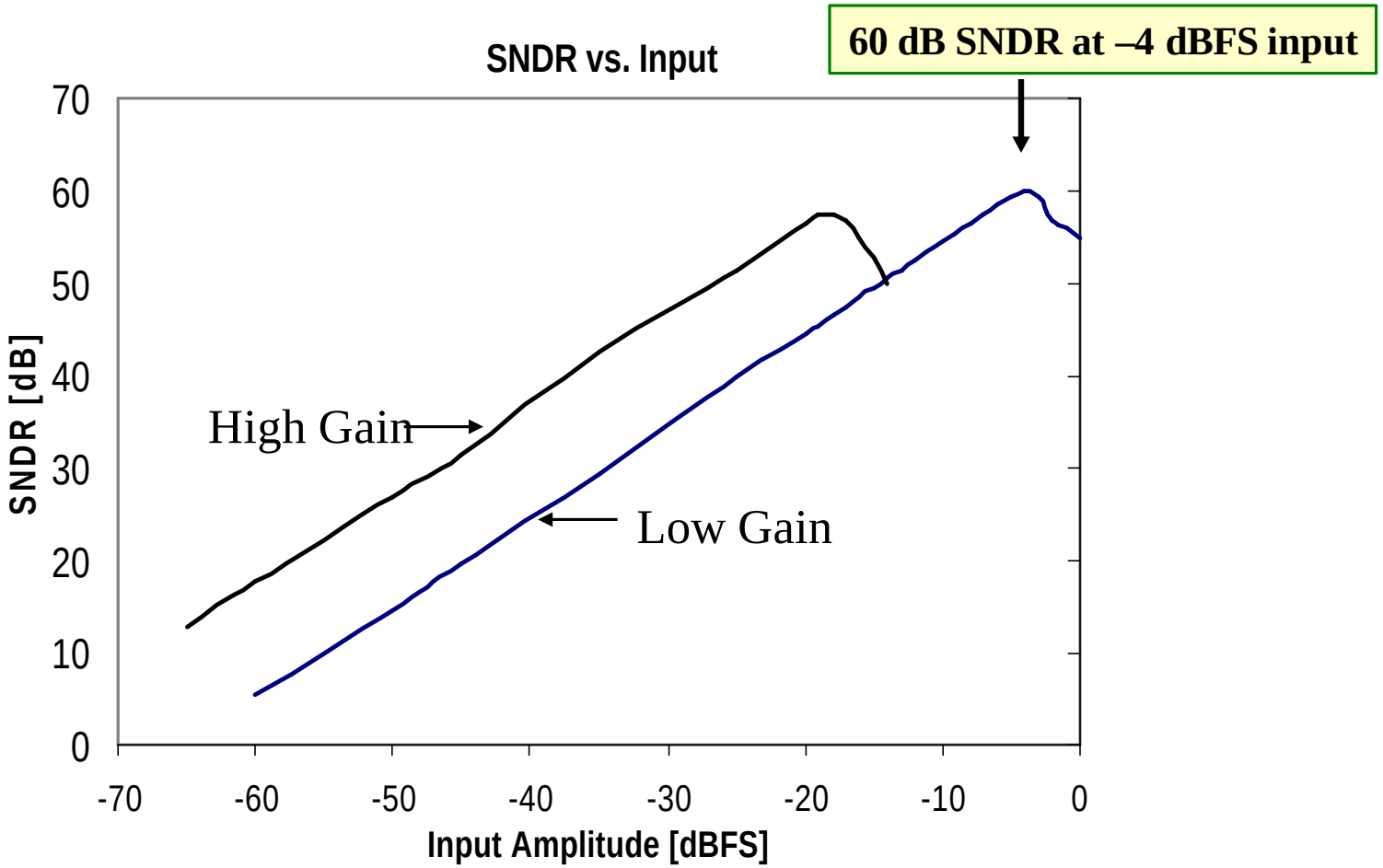
Measured SNDR



- **Peak SNDR for high gain mode is smaller since harmonics come earlier than low gain mode due to amplifier speed.**

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Performance summary

Technology	130nm Digital CMOS Process
Sampling Frequency	37.5 MHz
Signal Bandwidth	1 MHz
Peak SNDR1	60 dB
Peak SNDR2	57 dB
Dynamic Range	67 dB
Overall Dynamic Range	77 dB
Input Range	1.4 V_{pp} (differential)
Power Consumption	1.6 mW
Voltage Supply	1.58 V
Core Area	0.2 mm^2

- Sinusoidal signal at 360 kHz is used for performance measurements.
- Peak SNDR1 : when 0 dB gain option is selected.
- Peak SNDR2 : when 14 dB gain option is selected.

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Conclusion

- **Second order 5 level Sigma-Delta ADC with built-in anti-aliasing filter is realized.**
- **Decimation by two function relaxed settling and slew rate requirement.**
- **SC FIR filter for anti-aliasing is merged with sampling circuit.**
  - **Achieved power saving and cost reduction**
- **Two step gain control increases overall Dynamic Range.**
  - **Relax the automatic gain control burden in bluetooth system.**
- **Building block parameters are optimized based on noise analysis and realized low power consuming ADC.**

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66dB DR 1.2V 1.2mW Single-Amplifier Double-Sampling 2nd-order ?S ADC for WCDMA in 90nm CMOS

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Published in ISSCC2005

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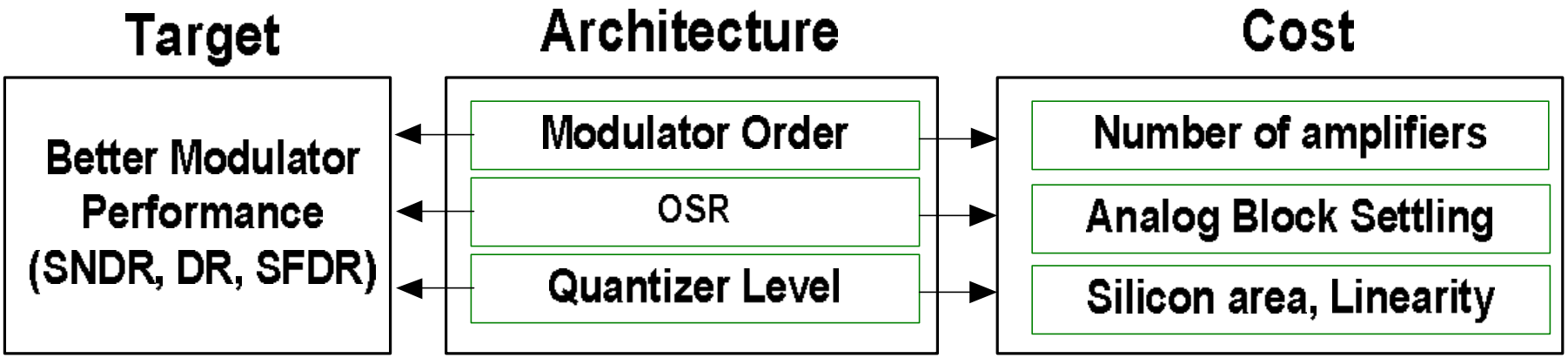
Objectives



- **For a given performance requirement, power consumption and area are optimized by:**
  - **Increasing sampling frequency → Double sampling technique**
  - **Increasing modulator order → Single Amplifier topology**
  - **Higher number of levels in Quantizer → 5-level quantizer with ILA**

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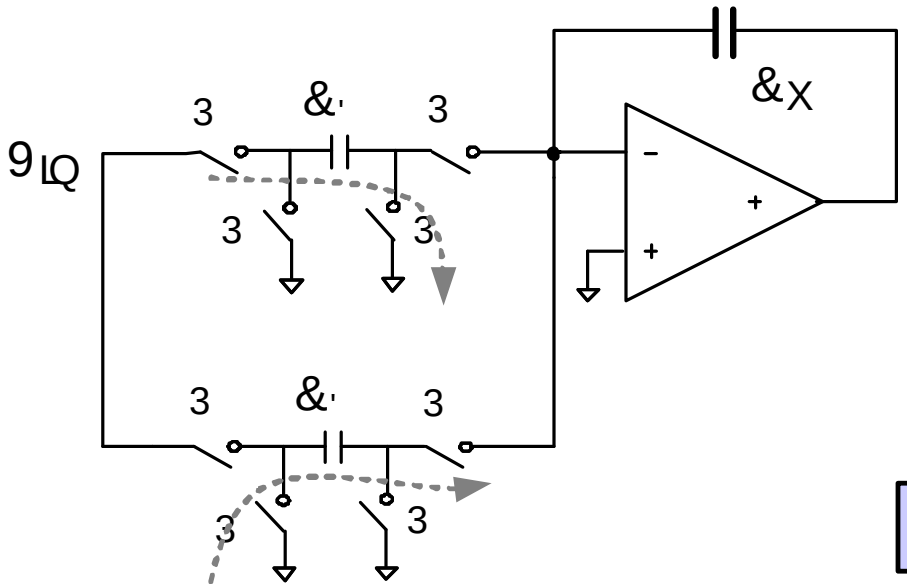
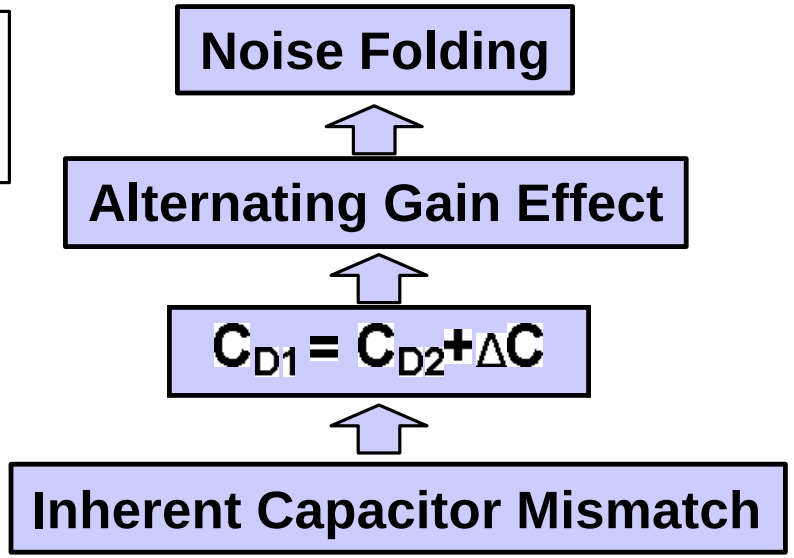
Double sampling

- **Advantages:**
  - **Efficient technique to double the OSR**
    - **Doesn't need faster op-amp settling**
    - **Provides improvement of SQNR by 6n+3 dB (n=order)**
- **Disadvantage:**
  - **Mismatch between capacitors creates noise folding**





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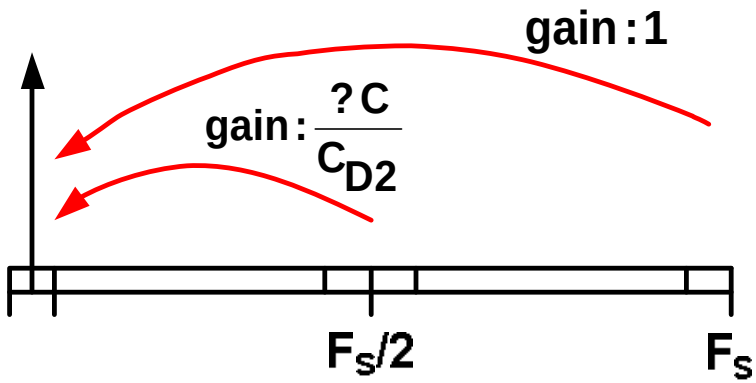
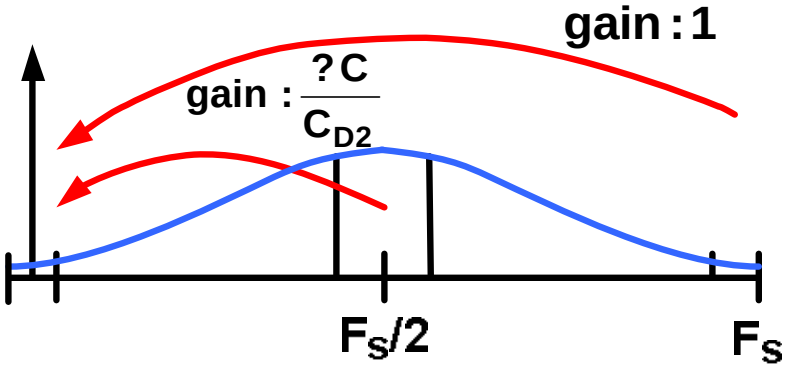
Noise Folding In Double Sampling

- **Alternating gain effect**

  → **Noise at $F_s/2$ is folded into Signal bandwidth**

Noise folding (Input sampling circuit)	Noise folding (DAC in feedback path)
	
• Noise at $F_s/2$ is suppressed by - Anti-aliasing filter - Pre-filtering	• No filtering on quantization noise

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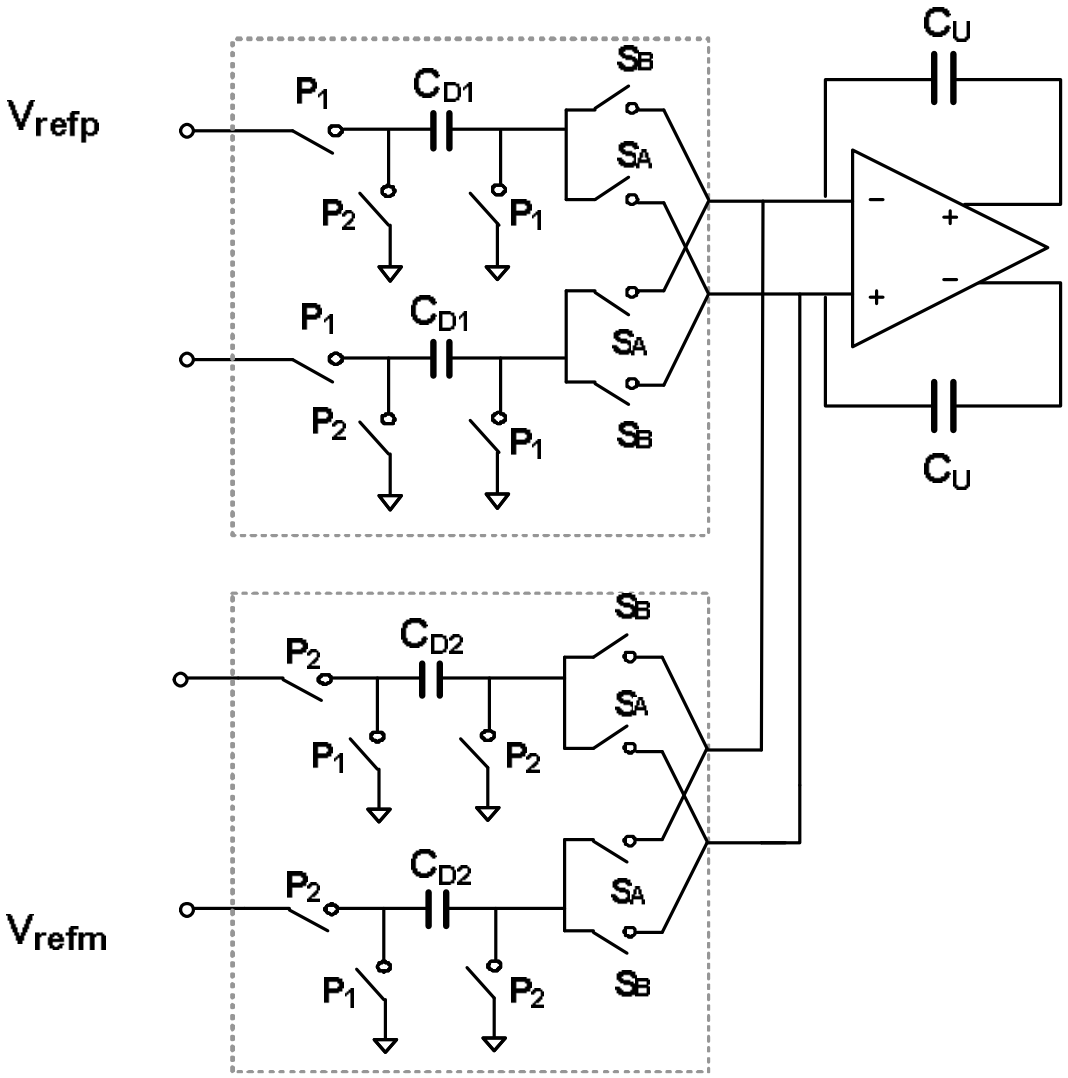

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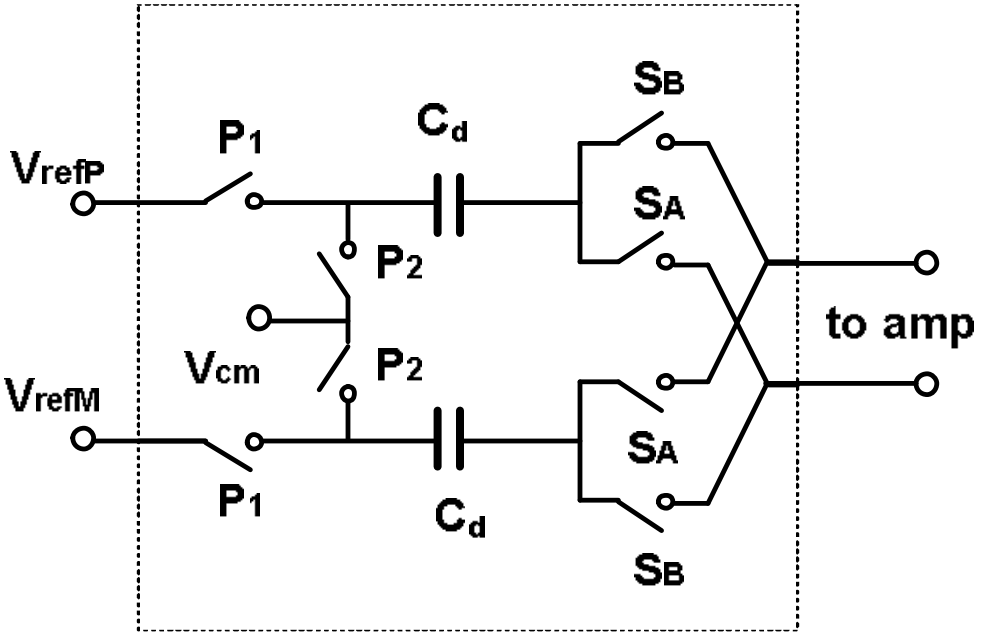
Proposed SC DAC element for double sampling

$B = b_0, b_1, b_2, b_3,$



	$b_i=1$		$b_i=0$	
P_1				
P_2				
S_A	ON	OFF	OFF	ON
S_B	OFF	ON	ON	OFF

- **Advantages of this approach vs. conventional approach:**
  - **Only one pair of capacitors needed**
  - **No “alternating-gain” effect**
  - **No additional circuitry needed for matching purposes**

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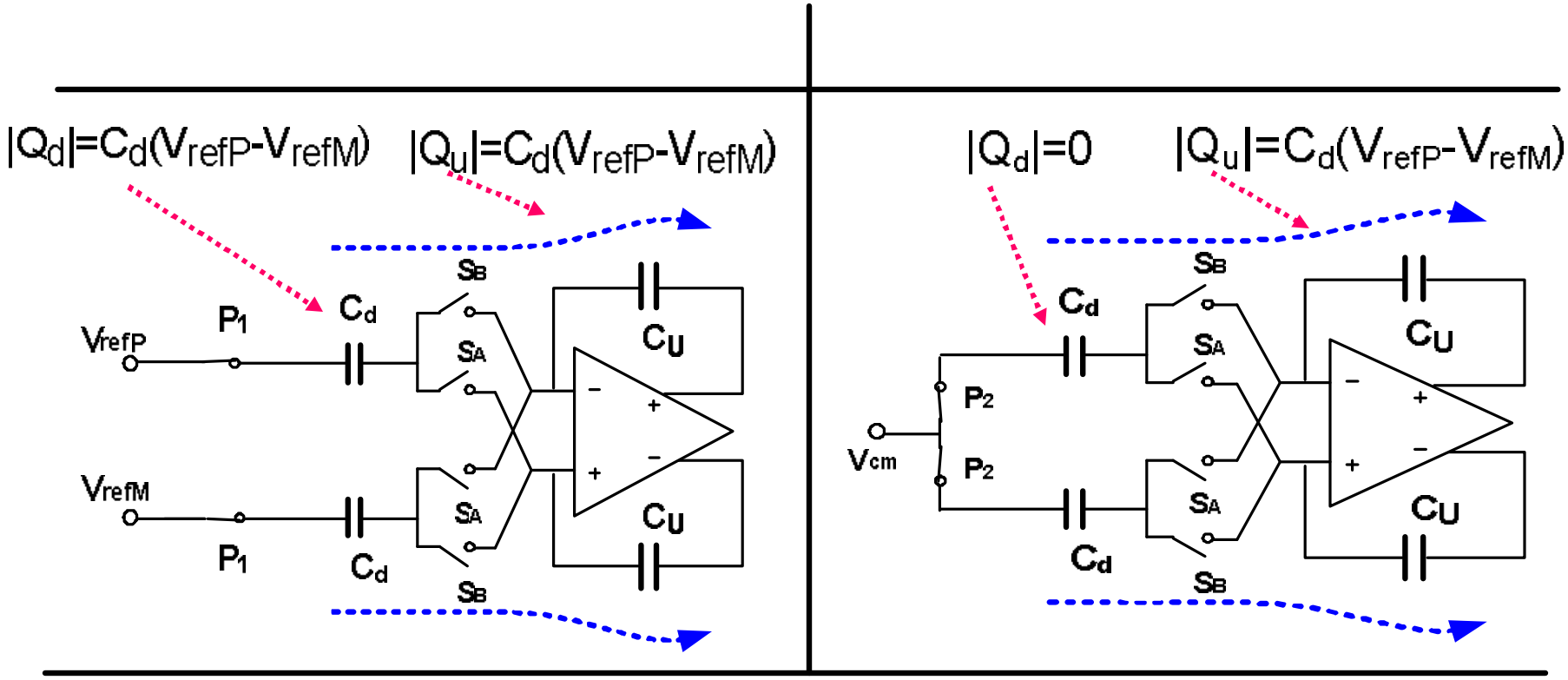
Operation of Proposed SC DAC element



- On phase P_1 the charge transferred to Integrating Capacitor is:
  - $Q_u = C_d(V_{refp}-V_{refm})$
  - Q_u is equal to the charge stored into C_d
  - This charge will be used during next integration phase

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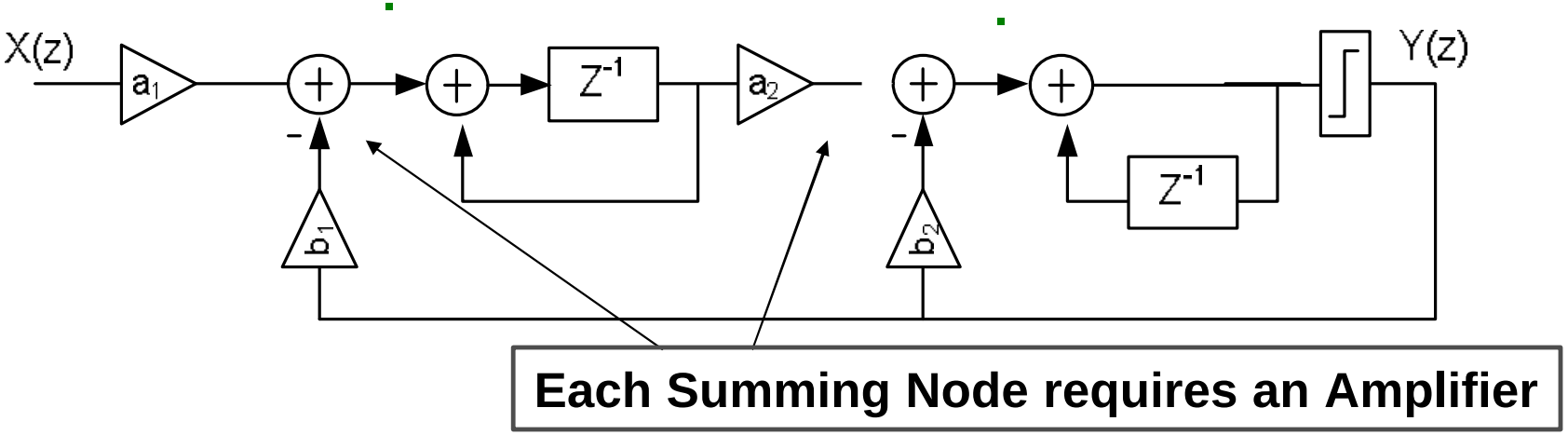
Conventional 2nd Order Sigma-Delta ADC



- **Conventional Sigma-delta ADC:**
  - **Needs an amplifier per summing node**
  - **Poles and zeros are chosen by a_i and b_i ,where i=1,2**

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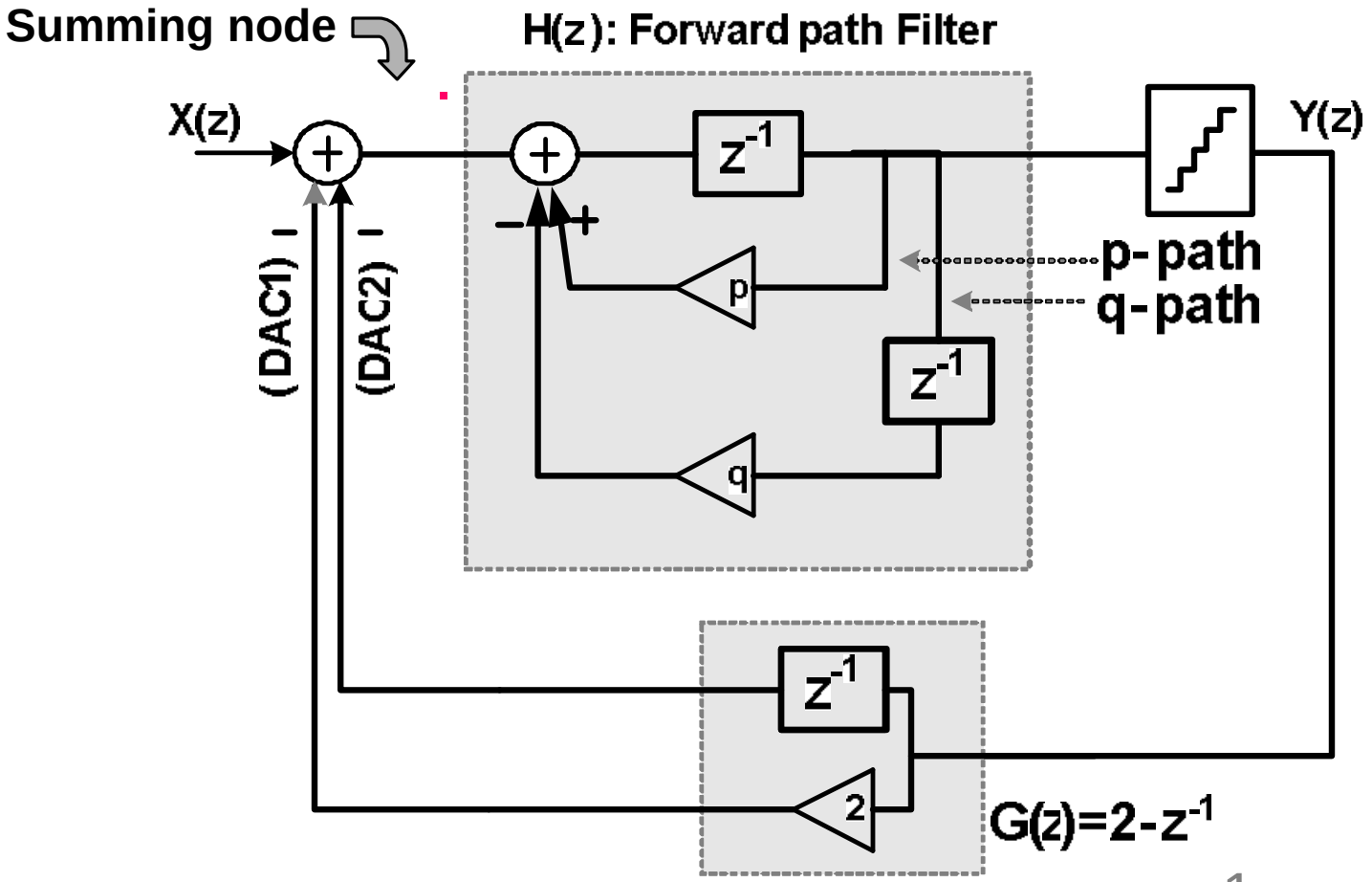
Single Amplifier 2nd Order Sigma-Delta ADC



$$STF = \frac{z^{-1}}{1 - p \cdot z^{-1} - q \cdot z^{-2} + z^{-1}G(z)} \qquad NTF = \frac{1 - p \cdot z^{-1} - q \cdot z^{-2}}{1 - p \cdot z^{-1} - q \cdot z^{-2} + z^{-1}G(z)}$$

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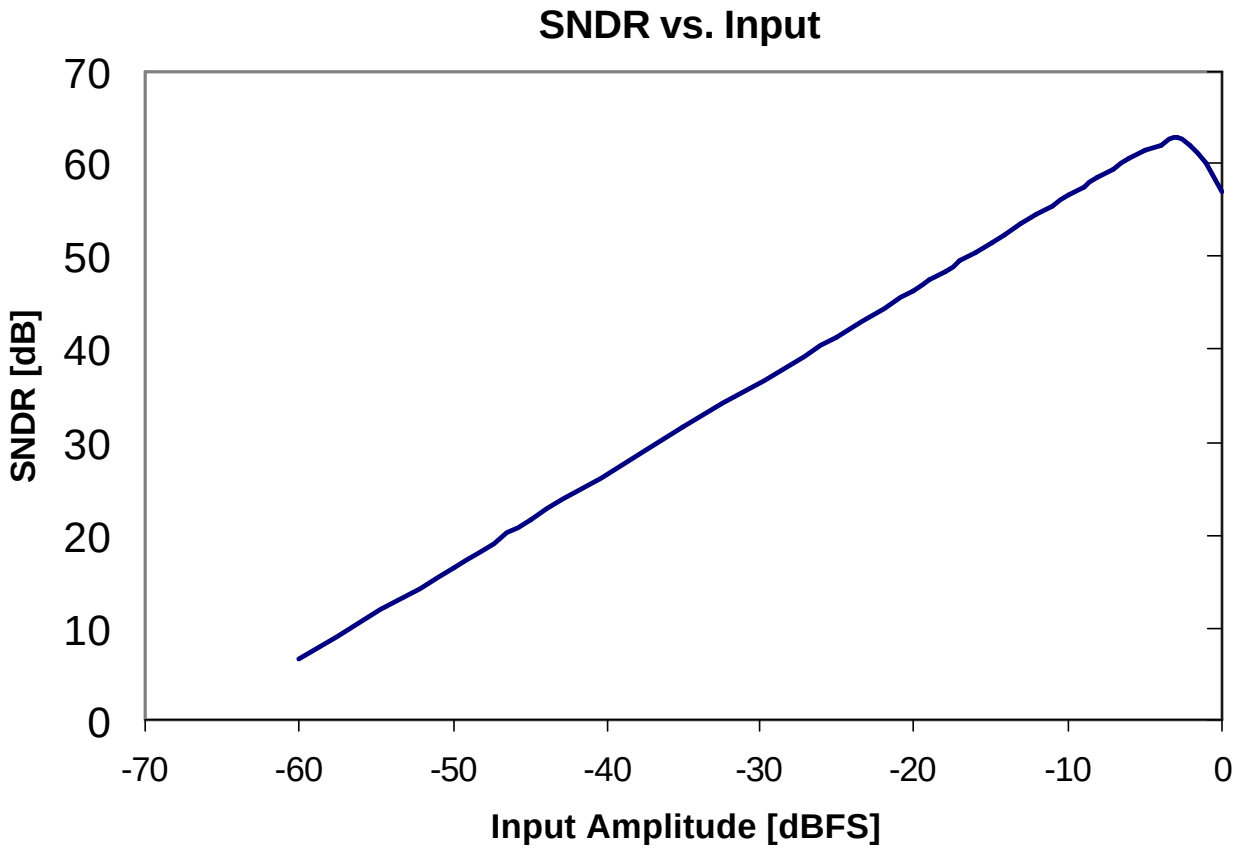
SNDR vs. Input power



- **63dB peak SNDR happens at -3dBFS input sinusoidal**

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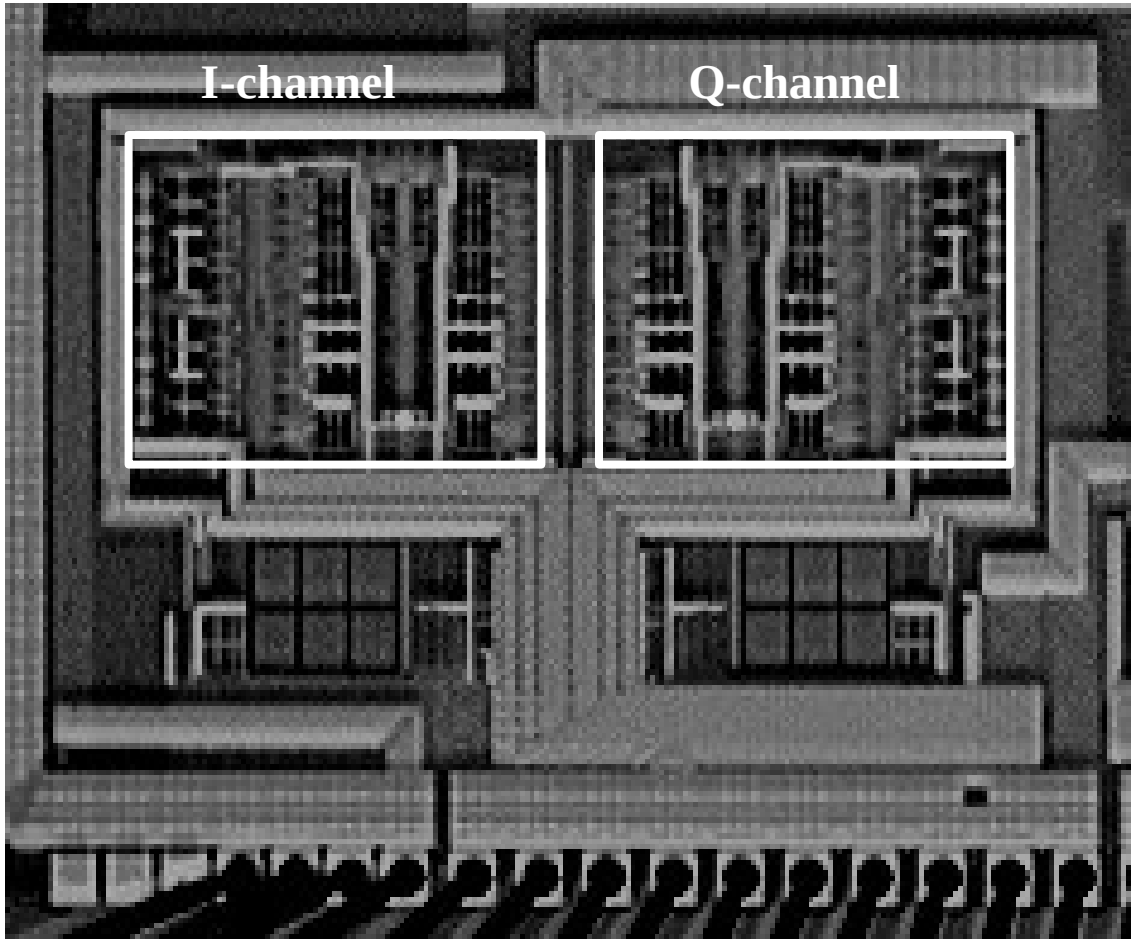
Die Photography for dual channel ADCs



- **Implemented in 90nm 5 metal digital CMOS process**

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Performance Summary

Technology	90 nm Digital CMOS
Signal Bandwidth	1.94 MHz
Clock Frequency	38.4 MHz
Sampling Frequency	76.8 MHz
Peak SNDR	63 dB
Dynamic Range	66 dB
Input Range	1.5 V_{pp} (differential)
Voltage Supply	1.2 V
Power Consumption	1.2 mW per ADC
Core Area	0.2 mm^2 per ADC

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Conclusions

- **Second order 5 level Single Amplifier Sigma-Delta ADC with double sampling technique was realized in 90 nm CMOS.**
- **By using double sampling technique, OSR is doubled with no increase of power consumption and silicon area.**
- **Single-capacitor double-sampling DAC solved “alternating-gain” error effect.**
- **2^{nd} order modulator is implemented using a Single-amplifier architecture. Higher order modulator is feasible.**
- **Low power consumption: 1.2mW for WCDMA, measured with a 1.2V power supply.**
- **66dB dynamic range was achieved in 1.94MHz bandwidth.**

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