Design of DC-DC Converters

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IEEE SSCS Dallas Chapter, October 2007
Design of DC-DC Converters

- DC-DC Converter Basics
  - Topology and Operation of DCDC Converters
  - Control Scheme for DCDC

- DC-DC Converter Design Techniques
  - System Level Modeling and Design
  - Building Block Design Considerations
DC-DC Converter Basics

- DC-DC Converter is a Voltage Regulator
  - Use Switches, Inductor and Capacitor for Power Conversion
  - Switched Mode Operation
- Why DC-DC Converters?
  - High Efficiency
  - Can Step-Down, Step-up, or Both, or Invert
  - Can Achieve Higher Output Power
DC-DC Converter Basics

- Why not DC-DC Converters?
  - Complex Control Loop
  - Higher Noise and Output Ripple
  - More External Components

- Basic DC-DC Converter Topologies
  - Majority of DC-DC uses PWM Control
    Operated in CCM Mode
**DC-DC Converter Basics**

- **Step-down (Buck)**

**Basic Relationships**

- **CCM Mode**
  - $I_L$ always supplies load
  - $I_C$ small, independent of load

\[
V_{OUT} = \frac{T_{ON}}{T} V_{IN} = D \cdot V_{IN}
\]

\[
I_{IN} = D \cdot I_{OUT}
\]

- **DCM Mode**

\[
V_{OUT} = \frac{T_{ON}^2}{T_{ON}^2 + \frac{2I_O \cdot L \cdot T}{V_{IN}}} V_{IN}
\]
DC-DC Converter Basics

- Step-up (Boost)

Basic Relationships

- **CCM Mode**
  - $I_L$ only supplies load during $T_{OFF}$ period
  - $I_C$ large and load dependent

$$V_{OUT} = \frac{T}{T_{OFF}} V_{IN} = \frac{1}{1-D} V_{IN}$$

$$I_{IN} = I_L = \frac{1}{1-D} I_{OUT}$$

- **DCM Mode**

$$V_{OUT} = \frac{T_{ON}^2 + 2I_O \cdot L \cdot T}{T_{ON}^2} \cdot V_{IN}$$
Common Control Architectures

- **Modulation Scheme**
  - **PFM (Pulse-Frequency-Modulation)**
    - Pulse Skipping, Hysteretic, Constant-on etc.
    - High Efficiency at Light Load
    - Inherently Higher Output Ripple
    - Unmanaged Spectrum Noise
  - **PWM (Pulse-Width-Modulation)**
    - Fixed Frequency with Variable Duty Cycle
    - Better Transient Response *(except Hysteretic?)*
    - Most Widely Used
Common Control Architectures

Control Method (for PWM)

- Voltage Mode
  - Regulates Output Voltage by Adjusting Duty Cycle
  - Constant Ramp for Modulation, Better Noise Immunity
  - LC Filter Contributes to Complex Conjugate Poles
  - Loop Has No Information on Inductor Current
  - Slower Response to Input Voltage Change
  - Bandwidth Varies with Input Voltage
  - Current Limit Done Separately
Common Control Architectures

Current Mode

- PCM (Peak-Current-Mode) Most Commonly Used
- Regulates Inductor Current to Satisfy Load Demand and Maintain Output Voltage
- Fast Current Loop makes Inductor to be a VCCS, eliminates Complex Conjugate Poles
- Easy Built-in Cycle-to-Cycle Current Limit
- Naturally Suitable for Multi-Phase Operation
- Current Sense Susceptible to Noise
- Need Slope Compensation for >50% Duty Cycle Operation
DC-DC Converter Design

- **Examples of Common DC-DC Converters**
  - **Voltage Mode Buck**
Voltage Mode Buck

Voltage Mode Buck Transfer Functions:

\[
\frac{v_Q}{d} \approx V_{IN} \frac{(1 + sCR_{ESR})}{s^2LC + s\left(\frac{L}{R_L} + CR_{ESR}\right) + 1} = V_{IN} \frac{(1 + sCR_{ESR})}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}
\]

\[
\omega_0 = \frac{1}{\sqrt{LC}}, Q = \frac{1}{\frac{1}{R_L}\sqrt{L} + R_{ESR}\sqrt{C}}
\]

and

\[
\frac{d}{V_{FB}} = \frac{1}{V_R} a(s)
\]

where \(a(s)\) is the transfer function of the error amplifier
Voltage Mode Buck

Control (Duty Cycle) to Output Transfer Function:

Example:
L = 2.2\,\mu\text{H}, \ C = 22\,\mu\text{F},
R_{\text{ESR}} = 10\,\text{m\,Ohm}
V_{\text{IN}} = 5\,\text{V}, \ V_{\text{OUT}} = 3.3\,\text{V}
R_L = 10 \,\text{Ohm}
F_{\text{SW}} = 1.5\,\text{MHz}
V_{\text{RAMP}} = 100\,\text{mV}

\omega_0 = 22.9\,\text{kHz}
Q \approx 15.8
\omega_Z = 700\,\text{kHz}
Voltage Mode Buck - Error Amp Ex. 1

Use low DC gain to set the bandwidth so that the phase margin is acceptable:

\[ V_{EA} = V_{REF} + \frac{R_2}{R_1} (V_{REF} - V_{FB}) \]

\[ v_{EA} = -\frac{R_2}{R_1} v_{FB} \]

\[ LG = -\frac{R_2}{R_1} \frac{V_{IN}}{V_R} \left(1 + sCR_{ESR}\right) \frac{1 + s/Q\omega_0 + s^2/\omega_0^2}{\omega_0^2} \]

Example: \( R_2 = 500k, R_1 = 100k, V_R = 100mV \)
Some Improvements Can Be Added:

- Make $V_{\text{RAMP}}$ proportional to $V_{\text{IN}}$ -> Constant Bandwidth
- Add Feed-forward Cap on Feedback Resistor String -> better phase margin

Limitations of Low DC Gain:

- Loose Output Regulation
- Need some ESR to Stabilize the Loop
- Small Modulation Ramp Sensitive to Noise
- DC Offset if Output Cap has large ESR
Voltage Mode Buck - Error Amp Ex. 2

Use Type-III Compensation Network to Re-Shape Loop Frequency Response:

Example Design Steps:
1. Set $R_1C_2=100\mu S$ for desired BW of $\sim300\text{kHz}$
2. Set 1st zero to be 1/5 of $\omega_0$:
   - $R_1=1\text{Meg}$, $C_1=30\text{pF}$, $\omega_{z1}=5.3\text{kHz}$
3. Set 2nd zero to be 4x of $\omega_0$:
   - $C_2=10\text{pF}$, $R_3=200\text{k}$, $\omega_{z2}=79.5\text{kHz}$
4. Mid-band DC gain of 5:
   - $R_3=200\text{k}$
5. Set 2nd and 3rd pole to near switching frequency for high frequency noise attenuation:
   - $C_3=0.2\text{pF}$, $\omega_{p2}=795\text{kHz}$; $R_2=10\text{k}$, $\omega_{p3}=1.5\text{MHz}$
- Modulation ramp $V_{\text{RAMP}}$ increased to 500mV for better noise immunity
- Blue: control to output transfer function
- Green: Type-III compensation error Amp transfer function
- Red: Complete loop transfer function
  bandwidth: $\sim$340kHz, PM: $\sim$65 degree

Compare to Error Amp Ex. 1:
- Step response has less overshoot due to better phase margin
- Settling is much slower due to 1st zero at low frequency
DC-DC Converter Design

- Current Mode Buck (Peak Current Control)
Current Mode Buck

Inductor Current Instability for Duty Cycle > 50%:

1. D=1/3: \( m_2/m_1 = 1/2 \)

\[ i_e[n+1] = i_e[n] \cdot \left( -\frac{m_2}{m_1} \right) = i_e[0] \cdot \left( -\frac{m_2}{m_1} \right)^n \]

\[ \left| \frac{m_2}{m_1} \right| < 1: \] \( i_e \) attenuates over cycles

\[ \left| \frac{m_2}{m_1} \right| > 1: \] \( i_e \) grows over cycles

Requires Slope Compensation:

\[ i_e[n+1] = i_e[n] \cdot \left( -\frac{m_2 - m_a}{m_1 + m_a} \right) \]

\( m_a \) is chosen so that \( \left| \frac{m_2 - m_a}{m_1 + m_a} \right| < 1 \)

ex: \( m_a = \frac{m_2}{2} \), guaranteed stable

\( m_a = m_2 \), 1 cycle correction
Current Mode Buck

- Fast current loop regulates inductor peak current, can be modeled as a VCCS with output impedance $R_x$
- Slower voltage loop provides reference for current loop

$$G_m = \frac{i_o}{V_{EA}} = \frac{1}{R_{SEN}} \frac{1}{1 + \frac{R_i T_s}{L} \left[1 + \frac{m_s}{m_i} \left(1 - D\right) - 0.5\right]} = \frac{1}{R_{SEN}} \frac{1}{1 + \frac{R_i}{R_x}}$$

where $R_x = \frac{L}{T_s \left[1 + \frac{m_s}{m_i} \left(1 - D\right) - 0.5\right]}$

Switched Operation results in delay and sampling effect:

$$H_s(s) = \frac{1 + \alpha}{1 + \alpha \cdot e^{-s T_0}} \frac{1 - e^{-s T_0}}{s T_0}$$

where $\alpha = \frac{m_s - m_u}{m_s + m_u}$

Complete VCCS transconductance including frequency response:

$$G_m(s) = \frac{1}{R_{SEN}} \frac{1}{1 + \frac{R_i T_s}{L} \left[1 + \frac{m_s}{m_i} \left(1 - D\right) - 0.5\right]} \frac{1 + \alpha}{1 + \alpha \cdot e^{-s T_0}} \frac{1 - e^{-s T_0}}{s T_0}$$

$$G_m(s) \approx \frac{1}{R_{SEN}} \frac{1}{1 + \frac{R_L}{R_x} \frac{s}{Q \omega_s} + \frac{s^2}{\omega_s^2}}$$

$$Q = \frac{2}{\pi} \frac{1}{\left(1 + \frac{m_s}{m_i} \left(1 - D\right) - 0.5\right)} = \frac{2}{\pi} \frac{1}{1 - 2D \left(1 - \frac{m_s}{m_z}\right)}$$
Current Mode Buck

Peak Current Mode Current Loop Transfer Function

Example:
L=2.2uH, $V_{IN}=5V$, $V_{OUT}=3.3V$, $R_L=10$ Ohm,
$R_{SEN} = 0.5$ Ohm,
$F_{SW} = 1.5$MHz

Blue: $m_a=0.5*m_2$
$R_X=19.4$ Ohm
$Gm=1.32$ A/V
$Q=1.87$

Green: $m_a=m_2$
$R_X=6.6$ Ohm
$Gm=0.80$ A/V
$Q=0.64$
Current Mode Buck

Control to Output Transfer Function
Equivalently Single-Pole System with Current Source Input

\[
\frac{v_o}{v_{EA}} = G_m \cdot Z_o = \frac{R_L}{1 + \frac{R_L}{R_{SEN}} \left(1 + \frac{s}{Q\omega_S} + \left(\frac{s}{\omega_S}\right)^2\right) \left[1 + sC\left(R_L \parallel R_X\right)\right]}\]

Example:
C=22uF, \(R_{ESR}=10\)m Ohm
\(R_{SEN} = 0.5\) Ohm
\(F_{SW} = 1.5\)MHz
\(R_X=19.4\) Ohm

\(R_L=10k, 1k, 100, 10, 1\) Ohm

\(R_L=10k, 1k, 100, 10, 1\) Ohm
Current Mode Buck – Error Amp

Error Amplifier Example:

\[ a(s) = \frac{V_{EA}}{V_{FB}} \approx -A_0 \frac{1 + sC_C R_Z}{[1 + sC_C(r_o + g_m R_1) R_Z + R_Z)(1 + sC_1 R_Z)} \]

\((C_C \gg C_1)\)

where: \(g_m\) is the transconductance of the error amp
\(r_o\) is the output impedance

- Bandwidth defined by \(R_1\) and \(C_1\)
- Much smaller \(C_C\), need large \(R_Z\)
- \(V_{FB}\) more error during transient

Example:
\(g_m = 100\mu S, r_o = 10\text{MOhm}, R_1 = 100\text{kOhm, } C_C = 25\text{pF}, R_Z = 1.5\text{MOhm, } C_1 = 0.3\text{pF}\)
Current Mode Buck – Error Amp

Complete Loop Transfer Function of Current Mode Buck:

\[ LG = - \frac{R_L}{R_{SEN}} \frac{1}{1 + \frac{R_L}{R_X}} \frac{1}{1 + \frac{s}{Q \omega_S} + \left(\frac{s}{\omega_S}\right)^2} \frac{1 + sC R_{ESR}}{\left[1 + sC \left(R_L \parallel R_X\right)\right]} \cdot A_0 \cdot \frac{1 + sC_c R_Z}{\left[1 + sC \left(r_o + g_m r_o R_1 + R_z\right)\right] \left(1 + sC_1 R_Z\right)} \]

- 1\text{st} zero of error amp placed near output filter pole
- ESR zero and 2\text{nd} pole of error amp are placed out of loop bandwidth

\[ BW \text{ obtained by setting } |LG| = 1: \]

\[ |LG(s_{BW})| \approx \frac{1}{R_{SEN}} \cdot \frac{1}{s_{BW} C} \cdot \frac{R_Z}{R_1} = 1 \]

\[ BW = \frac{1}{2\pi} \frac{R_Z}{R_1} \frac{1}{R_{SEN} C} \]
DC-DC Converter Design

- Voltage Mode Boost
Voltage Mode Boost

Voltage Mode Boost Transfer Functions:

\[
\frac{v_O}{d} \approx \frac{V_{IN}}{(1-D)^2} \left( 1 + s C R_{ESR} \right) \left( 1 - s \frac{L}{R_L (1-D)^2} \right) = \frac{V_{IN}}{(1-D)^2} \left( 1 + \frac{s}{\omega_z} \right) \left( 1 - \frac{s}{\omega_{RHP}} \right)
\]

\[
\omega_0 = \frac{(1-D)}{\sqrt{LC}}, \quad \omega_{RHP} = \frac{R_L (1-D)^2}{L}, \quad Q = \frac{1}{\frac{1}{(1-D)R_L \sqrt{L}} + \frac{1}{(1-D)R_{ESR}}} \sqrt{\frac{C}{L}}
\]

and

\[
\frac{d}{v_{FB}} = \frac{1}{V_R} a(s)
\]

where \( a(s) \) is the transfer function of the error amplifier.
Perturbation from Output to Inductor Current:

\[ L \frac{di_L}{dt} = V_{IN} - (1 - D)V_O \Rightarrow i_L = \frac{(1 - D)v_o}{sL} \]

and

\[ I_O = I_L(1 - D) \Rightarrow i_o = i_L(1 - D) \]

Impedance looking into the Inductor from Output:

\[ Z_o = \frac{v_o}{i_o} = \frac{sL}{(1 - D)^2} \]

Thus the Effective Inductance

\[ L_{eff} = \frac{L}{(1 - D)^2} \]

This makes the \( \omega_0 \) of the LC Filter to Move with D
Voltage Mode Boost - RHP Zero

Perturbation from Duty Cycle to Output Current:

\[ I_O = I_L (1 - D) \Rightarrow i_o = i_L (1 - D) - d \cdot I_L = i_L (1 - D) - d \cdot \frac{I_O}{1 - D} \]

\[ L \frac{di_L}{dt} = DV_{IN} + (1 - D)(V_{IN} - V_O) \Rightarrow i_L \approx \frac{d \cdot V_O}{sL} \]

Right-Half-Plan Zero forms at frequency where:

\[ \left| \frac{d \cdot V_O}{j \omega_{RHP} L} (1 - D) \right| = \left| d \cdot \frac{I_O}{1 - D} \right| \]

\[ \omega_{RHP} = \frac{R_L (1 - D)^2}{L} \]

Right-Half-Plan Zero exists for both Voltage Mode and Current Mode Boost
Voltage Mode Boost

Control (Duty Cycle) to Output Transfer Function:

Example:
$L=2.2\, \mu\text{H}$, $C=10\, \mu\text{F}$, $R_{\text{ESR}}=10\, \text{mOhm}$, $V_{\text{IN}}=2.5\, \text{V}$, $V_{\text{OUT}}=5\, \text{V}$, $10\, \text{V}$, $15\, \text{V}$, $I_{\text{OUT}}=100\, \text{mA}$, $F_{\text{SW}}=1.5\, \text{MHz}$

$\omega_0$ and $\omega_{\text{RHP}}$ moves lower with increased duty cycle
Voltage Mode Boost – Type-III Error Amp

Usually Type-III Compensation Network is Required:

Example Design Steps:
1. Estimate worst case
   \( \omega_{RHP} = 300\text{kHz} \)
2. Set BW < 100k:
   \( R_1C_2 < 2.75\mu\text{s} \)
3. Set both zeros near \( \omega_0 \):
   \( R_1 = 100k, \ C_1 = 100\text{pF}, \ R_3 = 300k, \ C_2 = 20\text{pF}, \)
   \( \omega_{z1} = 16.0\text{kHz}, \ \omega_{z2} = 26.5\text{kHz} \)
4. Bandwidth: \( f_{BW} = 80\text{kHz} \)
5. Mid-band DC gain of 1/3
6. Set 2\text{nd} and 3\text{rd} pole to beyond \( \omega_{RHP} \):
   \( R_2 = 10k, \ C_3 = 3\text{pF} \)
   \( \omega_{p2} = 530\text{kHz}, \ \omega_{p3} = 790\text{kHz} \)
Voltage Mode Boost – Type-III Error Amp

- Adjust $C_1$ to move 1$^{st}$ zero
- Adjust $R_3$ to move 2$^{nd}$ zero and mid-band gain
- 2$^{nd}$ pole and 3$^{rd}$ poles suppress high frequency noise
- Phase shift exceeds 180° at $\omega_0$ -> conditionally stable
- Move 1$^{st}$ zero lower to improve phase shift -> much larger $C_1$
DC-DC Converter Design

- Current Mode Boost

![Circuit Diagram of Current Mode Boost DC-DC Converter]

- Symbols and Labels:
  - $V_{IN}$, $V_{SW}$, $S2$, $V_{OUT}$
  - $D$, $D'$, $S1$
  - $R_{ESR}$, $C$, $R_L$
  - $S$, $Q$, $RST$
  - $L$, $E'A$
  - $V_{FB}$, $V_{REF}$
  - $V_{RAMP}$, $V_{EA}$
  - $CLK$, $RST$
  - $V_{SW}$, $V_{IN}$
  - $I_L$, $I_{OUT}$
Current Mode Boost

Transfer Function of the Current Loop:

\[
G_m = \frac{i_o}{v_{EA}} = \frac{1-D}{R_{SEN}} \frac{1}{1 + \frac{R_L}{2R_x}}
\]

where \( R_x = \frac{1}{(1-D)^2} \left( \frac{L}{T_s[(1+\frac{m_a}{m_1})(1-D) - 0.5]} || \frac{2L}{DT_s} \right) \)

Similar to Peak Current Mode Buck
Delay and sampling effect results in a 2 - pole system:

\[
G_m(s) \approx \frac{1-D}{R_{SEN}} \frac{1}{1 + \frac{R_L}{2R_x}} + \frac{s}{Q\omega_s} + \frac{s^2}{\omega_s^2}
\]

\[
\omega_s = \frac{\pi}{T_s}
\]

\[
Q = \frac{2}{\pi} \frac{1}{(1+\frac{m_a}{m_1})(1-D) - 0.5} = \frac{2}{\pi} \frac{1}{1 - 2D(1-\frac{m_a}{m_2})}
\]
Current Mode Boost

Control to Output Transfer Function:

\[
\frac{v_o}{v_{EA}} = G_m(s) \cdot Z_o = \frac{(1 - D)R_L}{2R_{SEN}} \left( \frac{1}{1 + \frac{R_L}{2R_x}} \right) \frac{1}{1 + \frac{s}{Q\omega_s} + \left(\frac{s}{\omega_s}\right)^2} \left(1 + sC\frac{R_L}{2 || R_x} \right)
\]

\[
\omega_{RHP} = \frac{R_L(1 - D)^2}{L}
\]

Example:

\(V_{IN} = 2.5V\)
\(V_{OUT} = 5V, 10V, 15V, 20V\)
\(L = 2.2\mu H, C = 10\mu F\)
\(R_{ESR} = 10m\ \text{Ohm}\)
\(I_{OUT} = 100mA\)
\(R_{SEN} = 0.5\ \text{Ohm}\)
\(F_{SW} = 1.5MHz\)
Use the same error amp structure as on page 22:

The Complete Loop Transfer Function:

\[
T(s) = \frac{1}{2R_{SEN}} \frac{(1 - D)R_L}{1 + \frac{R_L}{2R_x} + \frac{s}{Q\omega_s} + \left(\frac{s}{\omega_s}\right)^2} \cdot \frac{(1 + sC_{R_{ESR}})(1 - s - \frac{s}{\omega_{RHP}})}{[1 + sC\frac{R_L}{2} \| R_x]} \cdot \frac{1 + sC_{C_{R_Z}}}{[1 + sC_C(r_o + g_mR_1 + R_Z)](1 + sC_{C_{R_Z}})}
\]

Generally Guideline:

- To ensure loop stability, the unity-gain bandwidth is set to be 3-5x lower than the worst case RHP zero
- The ESR zero and 2\textsuperscript{nd} pole of the amplifier is placed higher than the RHP zero
- The current loop poles are usually much higher than RHP zero
Current Mode Boost – Error Amp Ex.

Loop Bandwidth can be estimated as:

\[ BW = \frac{1}{2\pi} \frac{(1 - D)}{R_{SEN} C} \cdot \frac{R_Z}{R_1} \leq \frac{\omega_{RHP}}{3} \]  
(RHP zero contributes <18° phase shift)

Since \( \omega_{RHP} \propto R_L (1 - D)^2 \) \( = R_L \left( \frac{V_{IN}}{V_O} \right)^2 = \frac{V_{IN}^2}{V_O \cdot I_O} \), \( BW \propto (1 - D) \)

Bandwidth should be set at max. duty cycle and load

Example:
\( V_{IN} = 2.5V, \ V_{OUT} = 5V, \ I_O = 500mA \)
\( L = 2.2\mu H, \ C = 10\mu F, \)
\( R_{SEN} = 0.5 \text{ Ohm}, \ R_Z = 1\text{M Ohm}, \)
\( \omega_{ZRHP} = 181\text{kHz}, \ BW \text{ chosen to be } \sim 60\text{kHz} \)
Calculate: \( R_1 : \sim 300k \text{ Ohm} \)
Current Mode Boost

Complete Loop Transfer Function of Current Mode Boost Converter:

Error Amplifier Example:
\( R_1 = 250k, \ R_Z = 1M \)
\( C_C = 25pF, \ C_1 = 0.3pF \)

Output Current:
1mA, 10mA, 100mA, 500mA

Loop BW: \(~60kHz\)
DC-DC Converter – Building Blocks

- **PWM Comparator**
  - Multi-Stage Gain -> Faster For Small Input Signal
  - But, High-Gain Stage Has Longer Recovery Time
  - So, Usually Low-Gain Amp(s) Followed by High-Gain Comparator
Building Blocks – PWM Comparator

OTA based comparator with pre-amps
Building Blocks – Error Amplifiers

- Error Amplifiers
  - Folded-Cascode Error Amplifier

Good:
- Input Common Mode Down to Ground
- Smaller Input Offset than OTA

But:
- Difficult to get large Gm
Building Blocks – Error Amplifiers

- Constant Gm Error Amplifier

Good:
- Constant Gm Defined by R
- Scalable Gm by Current Mirrors

But:
- Higher Input Offset due to Even More Current Mirrors
- Additional Gm Regulation Loop
DC-DC Converter Design

Acknowledgement:
Jian Zhou etc. for Review and Suggestions

Thank You For Your Attendance